

SEMICONDUCTOR DEVICE PACKAGES WITH ENHANCED THERMO-MECHANICAL RELIABILITY

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to semiconductor device packages and methods of forming the same. More specifically, embodiments described herein relate to structures of thin-form-factor semiconductor device packages and methods of forming the same.

Description of the Related Art

[0002] Ongoing trends in the development of semiconductor device technology have led to semiconductor components having reduced sizes and increased circuit densities. In accordance with demands for continued scaling of semiconductor devices while improving performance capabilities, these components and circuits are integrated into complex 3D semiconductor device packages that facilitate a significant reduction in device footprint and enable shorter and faster connections between components. Such packages may integrate, for example, semiconductor chips and a plurality of other electronic components for mounting onto a circuit board of an electronic device.

[0003] Conventionally, semiconductor device packages have been fabricated on organic package substrates due to the ease in forming features and connections therein, as well as the relatively low package manufacturing costs associated with organic composites. However, as circuit densities are increased and semiconductor devices are further miniaturized, the utilization of organic package substrates becomes impractical due to limitations with material structuring resolution to sustain device scaling and associated performance requirements.

[0004] More recently, 2.5D and/or 3D packages have been fabricated utilizing silicon-based substrates to compensate for some of the limitations associated with organic package substrates. Utilization of silicon-based materials for such packaging applications is driven by their excellent thermal properties, low coefficient of thermal expansion (CTE), smooth surfaces, and availability in large wafer and panel formats.

[0005] Yet, silicon-based materials substrates are not without their drawbacks. For example, the formation of features in silicon-based substrates, such as through-silicon vias (TSVs), is difficult and costly. In particular, high costs are imposed by high-aspect-ratio silicon via etching, chemical mechanical planarization, and semiconductor back end of line (BEOL) interconnection. Furthermore, silicon-based substrates often exhibit cracking and/or other defects when singulated from larger panels or wafers, and/or as caused by stresses induced by subsequently-formed insulation and/or redistribution layers (RDLs). In addition, such layers often debond or delaminate from silicon-based substrates due to weak adhesion therebetween.

[0006] Therefore, what is needed in the art are improved semiconductor device package structures for advanced packaging applications and methods of forming the same.

SUMMARY

[0007] Embodiments of the present disclosure relate to structures for thin-form-factor semiconductor device packages and methods of forming the same.

[0008] In certain embodiments, a package assembly is provided, the package assembly comprising: a frame having a first surface opposite a second surface, the frame further comprising: a frame material that comprises a first material that comprises silicon; at least one cavity with a semiconductor die disposed therein; a via comprising a via surface that defines an opening extending through the frame from the first surface to the second surface; and a coupling layer formed on the frame, the coupling layer comprising a silane coupling agent and contacting at least the first surface, and the second surface; an insulating layer disposed over the coupling layer on the first surface and the second surface of the frame, the insulating layer contacting at least a portion of each side of the semiconductor die; and an electrical interconnection disposed within the via, wherein the insulating layer and the coupling layer are disposed between the via surface and the electrical interconnection.

[0009] In certain embodiments, a package assembly is provided, the package assembly comprising: an embedded die assembly, comprising: a frame that comprises a first material that comprises silicon; a coupling layer disposed over the frame, the coupling layer comprising a silane coupling agent; one or more

semiconductor dies disposed within the frame, the one or more semiconductor dies having an integrated circuit formed thereon; and an insulating layer formed on the coupling layer, the insulating layer comprising an epoxy resin material having ceramic particles disposed therein; and one or more metal interconnections disposed within a portion of the embedded die assembly.

[0010] In certain embodiments, a package assembly is provided, the package assembly comprising: an embedded die assembly, comprising: a frame that comprises a first material that comprises silicon; a coupling layer formed over the frame and comprising a silane coupling agent; one or more semiconductor dies disposed within the frame; a first insulating layer formed on the frame, the first insulating layer comprising an epoxy resin material comprising ceramic particles; and one or more electrical interconnections disposed through the frame or the first insulating layer; and a redistribution layer formed on the embedded die assembly, the redistribution layer comprising: a second insulating layer formed on the first insulating layer; and one or more electrical redistribution connections disposed through the second insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

[0012] FIG. 1 illustrates a flow diagram of a process for forming a semiconductor device package, according to embodiments described herein.

[0013] FIG. 2 illustrates a flow diagram of a process for structuring and preparing a frame for forming a semiconductor device package, according to embodiments described herein.

[0014] FIGs. 3A-3D schematically illustrate cross-sectional views of a substrate at different stages of the frame structuring and preparation process depicted in FIG. 2, according to embodiments described herein.

[0015] FIGs. 4A-4F schematically illustrate cross-sectional views of a substrate at different stages of feature formation and subsequent damage removal, according to embodiments described herein.

[0016] FIGs. 5A-5F schematically illustrate cross-sectional views of a substrate at different stages of feature formation and subsequent damage removal, according to embodiments described herein.

[0017] FIGs. 6A-6E schematically illustrate cross-sectional views of a substrate at different stages of feature formation and subsequent damage removal, according to embodiments described herein.

[0018] FIGs. 7A-7D schematically illustrate cross-sectional views of a substrate at different stages of feature formation and subsequent damage removal, according to embodiments described herein.

[0019] FIG. 8 illustrates a schematic top view of a frame structured and prepared with the processes depicted in FIGs. 2, 3A-3D, 4A-4F, 5A-5F, 6A-6E, and 7A-7D according to embodiments described herein.

[0020] FIG. 9 illustrates a flow diagram of a process for forming an embedded die assembly having through-assembly vias and contact holes, according to embodiments described herein.

[0021] FIGs. 10A-10K schematically illustrate cross-sectional views of the embedded die assembly at different stages of the process depicted in FIG. 9, according to embodiments described herein.

[0022] FIG. 11 illustrates a flow diagram of a process for forming an embedded die assembly having through-assembly vias and contact holes, according to embodiments described herein.

[0023] FIGs. 12A-12G schematically illustrate cross-sectional views of the embedded die assembly at different stages of the process depicted in FIG. 11, according to embodiments described herein.

[0024] FIG. 13 illustrates a flow diagram of a process for forming interconnections in an embedded die assembly, according to embodiments described herein.

[0025] FIGs. 14A-14H schematically illustrate cross-sectional views of the embedded die assembly at different stages of the interconnection formation process depicted in FIG. 13, according to embodiments described herein.

[0026] FIG. 15 illustrates a flow diagram of a process for forming a redistribution layer on an embedded die assembly followed by package singulation, according to embodiments described herein.

[0027] FIGs. 16A-16L schematically illustrate cross-sectional views of an embedded die assembly at different stages of forming a redistribution layer followed by package singulation, as depicted in FIG. 15, according to embodiments described herein.

[0028] Fig. 17 schematically illustrate an exemplary apparatus for utilization with the processes of FIGs. 1-7D and 9-16L, according to embodiments described herein.

[0029] FIGs. 18A and 18B schematically illustrate cross-sectional views of dynamic random access memory (DRAM) stacks including a plurality of semiconductor device packages formed utilizing the processes depicted in FIGs. 1-7D and 9-16L, according to embodiments described herein.

[0030] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0031] The methods and apparatus disclosed herein include novel thin-form-factor semiconductor device packages intended to replace more conventional package structures utilizing organic substrates as frames, which are limited by material

structuring resolution, and further improve upon more recent package structures utilizing silicon-based or similar substrates as frames. Current package frames may provide low mechanical reliability, as they sometimes exhibit cracking and/or other defects caused by stresses induced by subsequently-formed insulation and/or redistribution layers (RDLs). In addition, during high temperature processing, the layers laminated directly onto the silicon-based substrate may debond or delaminate therefrom due to weak adhesion between silicon and dielectric materials. The methods and apparatus disclosed herein provide semiconductor device packages that overcome many of the disadvantages associated with conventional package architectures described above by utilizing frames coated with a layer of coupling agent, such as a silane coupling agent. The utilization of the coupling agent between the frame and subsequently formed layers enhances the thermo-mechanical reliability of the package frames by mitigating the stress induced by any subsequently formed insulation layers and/or RDLs, and by providing improved coupling between such layers and the relatively smooth surfaces of the frames.

[0032] As described in further detail below, FIG. 1 illustrates a flow diagram of a representative method 100 of forming a thin-form-factor semiconductor device package having a silane-coated frame. The method 100 has multiple operations 110, 120, 130, and 140. Each operation is described in greater detail with reference to FIGs. 2-16L. The method may include one or more additional operations which are carried out before any of the defined operations, between two of the defined operations, or after all of the defined operations (except where the context excludes the possibility).

[0033] In general, the method 100 includes structuring and preparing a substrate to be used as a package frame at operation 110, further described in greater detail with reference to FIGs. 2, 3A-3D, 4A-4F, 5A-5F, 6A-6E, 7A-7D, and 8. At operation 120, an embedded die assembly having one or more embedded dies and an insulating layer is formed, which is described in greater detail with reference to FIGs. 9 and 10A-10K and FIGs. 11 and 12A-12G. At operation 130, one or more interconnections are formed in and/or through the embedded die assembly for interconnection of embedded die-frame sets, which is described in greater detail with reference to FIGs. 13 and 14A-14H. At operation 140, a first redistribution layer is formed on the

embedded die assembly to relocate contact points of the interconnections to desired lateral locations on the embedded die assembly surface. In some embodiments, one or more additional redistribution layers may be formed in addition to the first redistribution layer before individual packages are singulated from the embedded die assembly, which is described in greater detail with reference to FIGs. 15 and 16A-16L.

[0034] FIG. 2 illustrates a flow diagram of a representative method 200 for structuring and preparing a substrate to be utilized as a package frame. FIGs. 3A-3D schematically illustrate cross-sectional views of a substrate 302 at different stages of the method 200 represented in FIG. 2. Therefore, FIG. 2 and FIGs. 3A-3D are herein described together for clarity.

[0035] The method 200 begins at operation 210 and corresponding FIG. 3A. The substrate 302 is formed of any suitable frame material including but not limited to a III-V compound semiconductor material, silicon, crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, silicon germanium, doped or undoped silicon, doped or undoped polysilicon, silicon nitride, quartz, borosilicate glass, glass, sapphire, alumina, and ceramic. In certain embodiments, the substrate 302 is a monocrystalline p-type or n-type silicon substrate. In certain embodiments, the substrate 302 is a polycrystalline p-type or n-type silicon substrate. In another embodiment, the substrate 302 is a p-type or n-type silicon solar substrate. The substrate 302 may further have a polygonal or circular shape. For example, the substrate 302 may include a substantially square silicon substrate having lateral dimensions between about 120 mm and about 180 mm, with or without chamfered edges. In another example, the substrate 302 may include a circular silicon-containing wafer having a diameter between about 20 mm and about 700 mm, such as between about 100 mm and about 500 mm, for example about 300 mm.

[0036] Unless otherwise noted, embodiments and examples described herein are conducted on substrates having a thickness between about 50 μm and about 1000 μm , such as between about 90 μm and about 780 μm . For example, the substrate 302 has a thickness between about 100 μm and about 300 μm , such as a thickness between about 110 μm and about 200 μm . In another example, the substrate 302

has a thickness between about 60 μm and about 160 μm , such as a thickness between about 80 μm and about 120 μm .

[0037] Prior to operation 210, the substrate 302 may be sliced and separated from a bulk material by wire sawing, scribing and breaking, mechanical abrasive sawing, or laser cutting. Slicing typically causes mechanical defects or deformities in substrate surfaces formed therefrom, such as scratches, micro-cracking, chipping, and other mechanical defects. Thus, the substrate 302 is exposed to a first damage removal process at operation 210 to smoothen and planarize surfaces thereof and remove any mechanical defects in preparation for later structuring and packaging operations. In some embodiments, the substrate 302 may further be thinned by adjusting the process parameters of the first damage removal process. For example, a thickness of the substrate 302 may be decreased with increased exposure to the first damage removal process.

[0038] The damage removal process at operation 210 includes exposing the substrate 302 to a substrate polishing process and/or an etch process followed by rinsing and drying processes. In some embodiments, operation 210 includes a chemical mechanical polishing (CMP) process. In certain embodiments, the etch process is a wet etch process including a buffered etch process that is selective for the removal of desired materials (e.g., contaminants and other undesirable compounds). In other embodiments, the etch process is a wet etch process utilizing an isotropic aqueous etch process. Any suitable wet etchant or combination of wet etchants may be used for the wet etch process. In certain embodiments, the substrate 302 is immersed in an aqueous HF etching solution for etching. In another embodiment, the substrate 302 is immersed in an aqueous KOH etching solution for etching.

[0039] In some embodiments, the etching solution is heated to a temperature between about 30 $^{\circ}\text{C}$ and about 100 $^{\circ}\text{C}$ during the etch process, such as between about 40 $^{\circ}\text{C}$ and about 90 $^{\circ}\text{C}$. For example, the etching solution is heated to a temperature of about 70 $^{\circ}\text{C}$. In still other embodiments, the etch process at operation 210 is a dry etch process. An example of a dry etch process includes a plasma-based dry etch process. The thickness of the substrate 302 is modulated by controlling the time of exposure of the substrate 302 to the etchants (e.g., the etching solution) used

during the etch process. For example, a final thickness of the substrate 302 is reduced with increased exposure to the etchants. Alternatively, the substrate 302 may have a greater final thickness with decreased exposure to the etchants.

[0040] At operations 220 and 230, the now planarized and substantially defect-free substrate 302 has one or more features, such as vias 303 and cavities 305, patterned therein and smoothened (one cavity 305 and four vias 303 are depicted in the lower cross-section of the substrate 302 in FIG. 3B). The vias 303 are utilized to form direct contact electrical interconnections through the substrate 302 and the cavities 305 are utilized to receive and enclose (i.e., embed) one or more semiconductor dies therein. FIGs. 4A-4C, 5A-5C, 6A-6C, and 7A-7B illustrate cross-sectional views of the substrate 302 at different stages of the feature formation and damage or defect removal (e.g., smoothening) processes according to embodiments described herein. Thus, operations 220 and 230 will now be described in greater detail with reference to FIGs. 4A-4C, 5A-5C, 6A-6C, and 7A-7B.

[0041] Turning now to FIGs. 4A-4C and 5A-5C, in certain embodiments, the substrate 302 may be patterned via a micro-blasting process. In such embodiments, if the substrate 302 has a thickness less than about 200 μm , such as a thickness of about 100 μm , or a thickness of about 50 μm , the substrate 302 may first be coupled to an optional carrier plate 406, as depicted in FIGs. 4A and 5A. The carrier plate 406 provides mechanical support for the substrate 302 during the substrate structuring process 200 and prevents the substrate 302 from breaking. The carrier plate 406 is formed of any suitable chemically and thermally stable rigid material including but not limited to glass, ceramic, metal, or the like. The carrier plate 406 has a thickness between about 1 mm and about 10 mm, such as between about 2 mm and about 5 mm. In certain embodiments, the carrier plate 406 has a textured surface. In other embodiments, the carrier plate 406 has a polished or smoothened surface.

[0042] In certain embodiments, the substrate 302 may be coupled to the carrier plate 406 via an adhesive layer 408. The adhesive layer 408 is formed of any suitable temporary bonding material, including but not limited to wax, glue, or similar bonding material. The adhesive layer 408 is applied onto the carrier plate 406 by mechanical rolling, pressing, lamination, spin coating, or doctor-blading. In certain embodiments, the adhesive layer 408 is a water-soluble or solvent-soluble adhesive layer. In other

embodiments, the adhesive layer 408 is a UV release adhesive layer. In still other embodiments, the adhesive layer 408 is a thermal release adhesive layer. In such embodiments, the bonding properties of the adhesive layer 408 degrade upon exposure to heat treatment, for example, by exposing the adhesive layer 408 to temperatures above 110 °C, such as above 150 °C. The adhesive layer 408 may further include one or more layers of additional films (not shown), such as a liner, a base film, a pressure-sensitive film, and other suitable layers.

[0043] In some embodiments, after bonding of the substrate 302 to the carrier plate 406, a resist film is applied to the substrate 302 to form a resist layer 404, as depicted in FIGs. 4A and 5A. In embodiments where the substrate 302 has a thickness of greater than about 200 μm, such as a thickness of about 250 μm, the resist layer 404 is formed on the substrate 302 without first coupling the substrate 302 to the carrier plate 406. The resist layer 404 is used to transfer a desired pattern to the substrate 302 upon which the resist layer 404 is formed during subsequent processing operations. After being patterned, the resist layer 404 protects selected regions of the underlying substrate 302 during later structuring operations.

[0044] The substrate 302 generally has a substantially planar surface upon which the resist layer 404 is formed. In some embodiments, such as those illustrated in FIG. 5A, the resist layer 404 is bonded to the substrate 302 via a resist adhesive layer 409. The resist adhesive layer 409 is formed of any suitable temporary bonding material, including but not limited to polyvinyl alcohol, triester with 2-ethyl-2-(hydroxymethyl)-1,3-propanediol, and other water- or solvent-soluble materials. In certain embodiments, the resist adhesive layer 409 is formed of a different material than the adhesive layer 408. In certain embodiments, the resist adhesive layer 409 is substantially similar in composition to the adhesive layer 408. The resist adhesive layer 409 is applied onto the substrate 302 by mechanical rolling, pressing, lamination, spin coating, or doctor-blading. In other embodiments, the resist layer 404 is formed of a temporary bonding material such as polyvinyl alcohol, thus enabling the resist layer 404 to be directly applied and bonded to the surface of the substrate 302. The resist layer 404 may include one or more layers, for example, a first resist layer and a second resist layer (not shown).

[0045] In certain embodiments, such as the embodiment illustrated in FIG. 4A, the resist layer 404 is a photosensitive layer (e.g., photoresist). The resist layer 404 may include a solvent, a photoresist resin, and a photoacid generator. The photoresist resin may be any positive photoresist resin or any negative photoresist resin. Representative photoresist resins include acrylates, novolak resins, poly(methylmethacrylates), and poly(olefin sulfones). Other photoresist resins may also be used. Upon exposure to electromagnetic radiation, the photoacid generator generates charged species, such as acid cations and anions. The photoacid generator may also generate polarized species. The photoacid generator sensitizes the resin to electromagnetic radiation. Representative photoacid generators include sulfonate compounds, such as, for example, sulfonated salts, sulfonated esters, and sulfonyloxy ketones. Other suitable photoacid generators include onium salts, such as aryl-diazonium salts, halonium salts, aromatic sulfonium salts and sulfoxonium salts or selenium salts. Other representative photoacid generators include nitrobenzyl esters, s-triazine derivatives, ionic iodonium sulfonates, perfluoroalkanesulfonates, aryl triflates and derivatives and analogs thereof, pyrogallol derivatives, and alkyl disulfones. Other photoacid generators may also be used. In certain embodiments, such as the embodiment illustrated in FIG. 5A, the resist layer 404 is a laser-sensitive resist.

[0046] After formation of the resist layer 404, the substrate 302 having the resist layer 404 formed thereon is exposed to electromagnetic radiation to pattern the resist layer 404, depicted in FIGs. 4B and 5B. In the embodiment illustrated by FIG. 4B, the substrate 302 having the resist layer 404 formed thereon is exposed to electromagnetic radiation in the ultraviolet (UV) range. Portions of the resist layer 404 are selectively exposed and portions of the resist layer 404 are selectively unexposed to the UV radiation. Upon exposure to the UV radiation, the selectively exposed portions of the resist layer 404 are structurally weakened (illustrated by hatching) while the selectively unexposed portions maintain their structural integrity. In certain embodiments, a mask 412 having a desired pattern is formed on or adjacent to the photosensitive resist layer 404 prior to UV radiation exposure. In other embodiments, the mask 412 is a reticle positioned between the resist layer 404 and the UV radiation source. The mask 412 is configured to transfer a desired pattern of UV radiation to

the resist layer 404. The mask 412 is formed of any suitable polymeric material, including but not limited to PTFE, PVDF, FEP, polyimide, or the like.

[0047] In the embodiment illustrated by FIG. 5B, the substrate 302 having the laser-sensitive resist layer 404 formed thereon is exposed to electromagnetic radiation generated by a laser source 307 instead of a UV radiation source. As such, patterning is accomplished by targeted laser ablation, without the use of a mask. The laser source 307 may be any suitable type of laser for patterning of the resist layer 404. In some examples, the laser source 307 is a femtosecond green laser. In other examples, the laser source 307 is a femtosecond UV laser. The laser source 307 generates a continuous or pulsed laser beam 310 for patterning of the resist layer 404. For example, the laser source 307 may generate a pulsed laser beam 310 having a frequency between 100 kHz and 1200 kHz, such as between about 200 kHz and about 1000 kHz. The laser source 307 is generally configured to form any desired pattern in the resist layer 404. It is further contemplated that the electromagnetic radiation at operation may alternatively include an electron beam or an ion beam instead of a laser beam.

[0048] In FIG. 4B, the resist layer 404 may be formed of any material having a suitable hardness after the resist layer 404 has been patterned, such as, for example, after exposing a negative photoresist to electromagnetic radiation to cause cross-linking of the material in the resist. In general, the resist layer 404 needs to have one or more desirable mechanical properties after the resist layer 404 has been patterned (e.g., deposited, exposed and developed). In certain embodiments, the resist layer 404 is formed of a material having a Shore A scale hardness value of between 40 and 90, such as between 60 and 70 after patterning. For example, the resist layer 404 is formed of a material having a Shore A scale hardness value of about 65 after patterning. In certain embodiments, the resist layer 404 is formed of a material having a tensile strength of between about 0.5 MPa and about 10 MPa, such as between about 1 MPa and about 8 MPa after patterning. For example, the resist layer 404 may be formed of a material having a tensile strength of about 7 MPa after patterning. In certain embodiments, the resist layer 404 is formed of a polydimethylsiloxane material. In other embodiments, the resist layer 404 is formed of polyvinyl alcohol, triester with 2-ethyl-2-(hydroxymethyl)-1, 3- propanediol, or the like.

[0049] Following patterning of the resist layer 404, the substrate 302 having the resist layer 404 formed thereon is micro-blasted to form a desired pattern in the substrate 302, as depicted in FIGs. 4C and 5C. During the micro-blasting process, a stream of powder particles 309 is propelled toward the substrate 302 by use of a high-pressure carrier gas to dislodge exposed portions of the substrate 302 and/or layers formed thereon. The micro-blasting process is performed using any suitable substrate abrading system.

[0050] The micro-blasting process is determined by the material properties of the powder particles 309, the momentum of the powder particles that strike the exposed surface of the substrate 302 and the material properties of the substrate 302 along with, when applicable, the selectively-exposed portions of the resist layer 404. To achieve desired substrate patterning characteristics, adjustments are made to the type and size of the powder particles 309, the size and distance of the abrading system's applicator nozzle to the substrate 302, the pressure, which correlates to the velocity and flow rate, of the carrier gas utilized to propel the powder particles 309, and the density of the powder particles 309 in the fluid stream. For example, a desired fluid pressure of the carrier gas used for propelling the powder particles 309 toward the substrate 302 for a desired fixed micro-blasting device nozzle orifice size is determined based on the materials of the substrate 302 and the powder particles 309. In certain embodiments, the fluid pressure utilized to micro-blast the substrate 302 ranges from between about 50 psi and about 150 psi, such as between about 75 psi and about 125 psi, to achieve a carrier gas and particle velocity of between about 300 and about 1000 meters per second (m/s) and/or a flow rate of between about 0.001 and about 0.002 cubic meters per second (m³/s). For example, the fluid pressure of an inert gas (e.g., nitrogen (N₂), CDA, argon) that is utilized to propel the powder particles 309 during micro-blasting is about 95 psi to achieve a carrier gas and particle velocity of about 2350 m/s. In certain embodiments, the applicator nozzle utilized to micro-blast the substrate 302 has an inner diameter of between about 0.1 and about 2.5 millimeters (mm) that is disposed at a distance between about 1 mm and about 5 mm from the substrate 302, such as between about 2 mm and about 4 mm. For example, the applicator nozzle is disposed at a distance of about 3 mm from the substrate 302 during micro-blasting.

[0051] Generally, the micro-blasting process is performed with powder particles 309 having a sufficient hardness and high melting point to prevent particle adhesion upon contact with the substrate 302 and/or any layers formed thereon. For example, the micro-blasting process is performed utilizing powder particles 309 formed of a ceramic material. In certain embodiments, the powder particles 309 utilized in the micro-blasting process are formed of aluminum oxide (Al_2O_3). In another embodiment, the powder particles 309 are formed of silicon carbide (SiC). Other suitable materials for the powder particles 309 are also contemplated. The powder particles 309 generally range in size between about 15 μm and about 60 μm in diameter, such as between about 20 μm and about 40 μm in diameter. For example, the powder particles 309 are an average particle size of about 27.5 μm in diameter. In another example, the powder particles 309 have an average particle size of about 23 μm in diameter.

[0052] The effectiveness of the micro-blasting process at operation 220 and depicted in FIGs. 4C and 5C further depends on the material characteristics of the resist layer 404. Utilizing a material having too high of a Shore A Scale hardness may cause unwanted ricocheting of the powder particles 309 between sidewalls of the resist layer 404, thus reducing the velocity upon which the powder particles 309 bombard the substrate 302, and ultimately reducing the effectiveness of the powder particles 309 in eroding or dislodging exposed regions of the substrate 302. Conversely, utilizing a material having too low of a Shore A Scale hardness may cause unwanted adhesion of the powder particles 309 to the resist layer 404. It is contemplated that a Shore A Scale hardness value of between about 40 and about 90 is utilized for the resist layer 404 material, as described above.

[0053] In embodiments where the resist layer 404 is a photoresist, such as the embodiment depicted in FIG. 4C, the substrate 302 remains unexposed at the start of the micro-blasting process. Thus, the powder particles 309 first bombard a surface of the photoresist, causing material from the UV-exposed and structurally weakened portions of the photoresist to be dislodged and removed. The powder particles 309 eventually penetrate through and remove the brittle UV-exposed portions to form voids in the resist layer 404, thus exposing desired regions of the substrate 302 while other regions remain shielded by the UV-unexposed portions of the photoresist.

Micro-blasting is then continued until the powder particles 309 dislodge and remove a desired amount or depth of material from the exposed regions of the substrate 302, thus forming a desired pattern in the substrate 302. In embodiments where the resist layer 404 is patterned by laser ablation, such as the embodiment depicted in FIG. 5C, desired regions of the substrate 302 are already exposed through voids in the resist layer 404 prior to the micro-blasting process. Thus, minimal to no removal of the resist layer 404 is contemplated during micro-blasting.

[0054] The processes described above for forming features in the substrate 302 at operation 220 may cause unwanted mechanical defects on the surfaces of the substrate 302, such as chipping and cracking. Therefore, after performing operation 220 to form desired features in the substrate 302, the substrate 302 is exposed to a second damage removal and cleaning process at operation 230 to smoothen the surfaces of the substrate 302 and remove unwanted debris, followed by a stripping of the resist layer 404 and optional debonding of the substrate 302 from the carrier plate 406. FIGs. 4D-4F and 5D-5F illustrate cross-sectional views of the substrate 302 at different stages of the second damage removal, cleaning, resist stripping, and substrate debonding processes according to embodiments described herein. Thus, operation 230 will now be described in greater detail with reference to FIGs. 4D-4F and 5D-5F.

[0055] The second damage removal process at operation 230 is substantially similar to the first damage removal process at operation 210 and includes exposing the substrate 302 to an etch process, followed by rinsing and drying. The etch process proceeds for a predetermined duration to smoothen the surfaces of the substrate 302, and in particular, the surfaces exposed to the micro-blasting process. In another aspect, the etch process is utilized to remove undesired debris remaining from the micro-blasting process. Leftover powder particles adhering to the substrate 302 may be removed during the etch process. FIGs. 4D and 5D illustrate the substrate 302 after removal of debris and surface smoothening.

[0056] In certain embodiments, the etch process is a wet etch process utilizing a buffered etch process preferentially etching the substrate surface versus the resist layer 404 material. For example, the buffered etch process is selective for polyvinyl alcohol. In other embodiments, the etch process is a wet etch process utilizing an

aqueous etch process. Any suitable wet etchant or combination of wet etchants may be used for the wet etch process. In certain embodiments, the substrate 302 is immersed in an aqueous HF etching solution for etching. In another embodiment, the substrate 302 is immersed in an aqueous KOH etching solution for etching. The etching solution may further be heated to a temperature between about 40 °C and about 80 °C during the etch process, such as between about 50 °C and about 70 °C. For example, the etching solution is heated to a temperature of about 60 °C. The etch process may be isotropic or anisotropic. In still other embodiments, the etch process at operation 230 is a dry etch process. An example of a dry etch process includes a plasma-based dry etch process.

[0057] After debris has been removed and the substrate surfaces have been smoothed, the substrate 302 is exposed to a resist stripping process. The stripping process is utilized to de-bond the resist layer 404 from the substrate 302, as depicted in FIGs. 4E and 5E. In certain embodiments, a wet process is used to de-bond the resist layer 404 from the substrate 302 by dissolving/solubilizing the resist adhesive layer 409. Other types of etch process are also contemplated for releasing the resist adhesive layer 409. In certain embodiments, a mechanical rolling process is used to physically peel off the resist layer 404 or the resist adhesive layer 409 from the substrate 302. In certain embodiments, an ashing process is used to remove the resist layer 404 from the substrate 302 by use of, for example, an oxygen plasma assisted process.

[0058] After the resist stripping process, the substrate 302 is exposed to an optional carrier de-bonding process as depicted in FIGs. 4F and 5F. The utilization of the carrier de-bonding process is dependent on whether the substrate 302 is coupled to the carrier plate 406 and the type of bonding material utilized to couple the substrate 302 and the carrier plate 406. As described above and depicted in FIGs. 4A-4F and 5A-5F, in embodiments where the substrate 302 has a thickness of less than about 200 μm , the substrate 302 is coupled to the carrier plate 406 for mechanical support during the formation of features at operation 220. The substrate 302 is coupled to the carrier plate 406 via the adhesive layer 408. Thus, after micro-blasting and subsequent substrate etch and resist stripping, the substrate 302 coupled to the

carrier plate 406 is exposed to the carrier de-bonding process to de-bond the substrate 302 from the carrier plate 406 by releasing the adhesive layer 408.

[0059] In certain embodiments, the adhesive layer 408 is released by exposing the substrate 302 to a bake process. The substrate 302 is exposed to temperatures of between about 50 °C and about 300 °C, such as temperatures between about 100 °C and about 250 °C. For example, the substrate 302 is exposed to a temperature of between about 150 °C and about 200 °C, such as about 160 °C for a desired period of time in order to release the adhesive layer 408. In other embodiments, the adhesive layer 408 is released by exposing the substrate 302 to UV radiation.

[0060] FIGs. 4F and 5F illustrate the substrate 302 after completion of operations 210-230. The cross-sections of the substrate 302 in FIGs. 4F and 5F depict a single cavity 305 formed therethrough and surrounded on either lateral side by two vias 303. A schematic top view of the substrate 302 upon completion of the operations described with reference to FIGs. 4A-4F and 5A-5F is depicted in FIG. 8, described in further detail below.

[0061] FIGs. 6A-6E illustrate schematic, cross-sectional views of a substrate 302 during an alternative micro-blasting process for operations 220 and 230 similar to those described above. The alternative process sequence depicted for operations 220 and 230 involves patterning the substrate 302 on two major opposing surfaces as compared to only one surface, thus enabling increased efficiency during structuring of the substrate 302. The embodiment depicted in FIGs. 6A-6E includes substantially all of the processes as described with reference to FIGs. 4A-4F and 5A-5F. For example, FIG. 6A corresponds with FIGs. 4A and 5A, FIG. 6B corresponds with FIGs. 4B and 5B, FIG. 6C corresponds with FIGs. 4C and 5C, FIG. 6D corresponds with FIGs. 4D and 5D, and FIG. 6E corresponds with FIGs. 4F and 5F. However, unlike the previous embodiments, the embodiment of operation 220 depicted in FIGs. 6A-6E includes a substrate 302 having two resist layers 404 formed on major opposing surfaces 606, 608 thereof, as opposed to one resist layer 404 formed on a single surface. Therefore, the processes performed during operations 210-230 will need to be performed at the same time (i.e., simultaneously) or one after the other (i.e., sequentially) on both sides of the substrate during each operation. While FIGs. 6A-

6E only illustrate the formation of vias 303, the processes described herein can also be used to form cavities 305, or cavities 305 and vias 303.

[0062] Accordingly, after exposing the resist layer 404 on one side of the substrate 302 to electromagnetic radiation for patterning, such as the side including the surface 608, the substrate 302 may be optionally flipped so that the resist layer 404 on the opposing surface 606 is also exposed to the electromagnetic radiation for patterning, as depicted in FIG. 6B. Similarly, after performing the micro-blasting process on the surface 608 of the substrate 302, the substrate 302 may be optionally flipped so that micro-blasting may be performed against the opposing surface 606 as depicted in FIG. 6C. Thereafter, the substrate 302 is exposed to a second damage removal and cleaning process and a resist stripping process, depicted in FIGs. 6D-6E. By utilizing two resist layers 404 on major opposing surfaces 606, 608 of the substrate 302 and performing the micro-blasting process against both surfaces 606 and 608, potential tapering of the features formed therein by the micro-blasting process may be reduced or eliminated and efficiency of the process used to structure the substrate 302 can be increased.

[0063] FIGs. 7A-7D illustrate schematic, cross-sectional views of a substrate 302 during another alternative process sequence for operations 220 and 230, wherein a desired pattern is formed in the substrate 302 by direct laser ablation. As depicted in FIG. 7A, the substrate 302, such as a solar substrate or even a semiconductor wafer, is placed on a stand 706 of a laser ablation system (not shown). The stand 706 may be any suitable rigid and planar or textured (e.g., structured) surface for providing mechanical support for the substrate 302 during laser ablation. In some embodiments, the stand 706 includes an electrostatic chuck for electrostatic chucking of the substrate 302 to the stand 706. In some embodiments, the stand 706 includes a vacuum chuck for vacuum chucking of the substrate 302 to the stand 706. After placing the substrate 302 on the stand 706, a desired pattern is formed in the substrate 302 by laser ablation, depicted in FIG. 7B.

[0064] The laser ablation system may include any suitable type of laser source 307 for patterning the substrate 302. In some examples, the laser source 307 is an infrared (IR) laser. In some examples the laser source 307 is a picosecond UV laser. In other examples, the laser source 307 is a femtosecond UV laser. In yet other

examples, the laser source 307 is a femtosecond green laser. The laser source 307 generates a continuous or pulsed laser beam 310 for patterning of the substrate 302. For example, the laser source 307 may generate a pulsed laser beam 310 having a frequency between 5 kHz and 500 kHz, such as between 10 kHz and about 200 kHz. In one example, the laser source 307 is configured to deliver a pulsed laser beam at a wavelength of between about 200 nm and about 1200 nm and at a pulse duration between about 10 ns and about 5000 ns with an output power of between about 10 Watts and about 100 Watts. The laser source 307 is configured to form any desired pattern and features in the substrate 302, including the cavities 305 and the vias 303.

[0065] Similar to micro-blasting, the process of direct laser patterning of the substrate 302 may cause unwanted mechanical defects on the surfaces of the substrate 302, including chipping and cracking. Thus, after forming desired features in the substrate 302 by direct laser patterning, the substrate 302 is exposed to a second damage removal and cleaning process substantially similar to embodiments described above. FIGs. 7C-7D illustrate the structured substrate 302 before and after performing the second damage removal and cleaning process, resulting in a smoothened substrate 302 having a cavity 305 and four vias 303 formed therein.

[0066] In certain embodiments, after removal of mechanical defects in the substrate 302 at operation 230, the substrate 302 may be exposed to an oxidation process to grow or deposit an insulating oxide film (i.e. layer) 314 on desired surfaces thereof, as shown in FIG. 3C. For example, the oxide film 314 may be formed on all surfaces of the substrate 302, such that it surrounds the substrate 302. The insulating oxide film 314 acts as a passivating layer on the substrate 302 and provides a protective outer barrier against corrosion and other forms of damage. In certain embodiments, the oxidation process is a thermal oxidation process. The thermal oxidation process is performed at a temperature of between about 800 °C and about 1200 °C, such as between about 850 °C and about 1150 °C. For example, the thermal oxidation process is performed at a temperature of between about 900 °C and about 1100 °C, such as a temperature of between about 950 °C and about 1050 °C. In certain embodiments, the thermal oxidation process is a wet oxidation process utilizing water vapor as an oxidant. In certain embodiments, the thermal oxidation process is a dry process utilizing molecular oxygen as the oxidant. It is contemplated

that the substrate 302 may be exposed to any suitable oxidation process at operation 240 to form the oxide film 314 thereon. The oxide film 314 generally has a thickness between about 100 nm and about 3 μm , such as between about 200 nm and about 2.5 μm . For example, the oxide film 314 has a thickness between about 300 nm and about 2 μm , such as about 1.5 μm .

[0067] At operation 240 and FIG. 3D, a coupling layer 316 is formed on desired surfaces of the substrate 302. For example, the coupling layer 316 may be formed on all surfaces of the substrate 302 as shown in FIG. 3D, or only some surfaces, such as major surfaces 606 and 608. In certain embodiments, the coupling layer 316 is formed over the oxide film 314.

[0068] The coupling layer 316 generally comprises a coating formed of one or more coupling agents to facilitate improved adhesion between the substrate 302 and any subsequently-formed insulation and/or redistribution layers thereon, such as the insulating layer 1018 described below with reference to FIG. 9 and FIGs. 10A-10K. Conventionally, insulation and/or redistribution layers, which are typically comprised of organic and/or dielectric materials, are formed directly over the frame of a semiconductor package device. However, when utilizing a silicon-based frame, poor adhesion between the frame and a subsequently-formed insulation and/or redistribution layer allows moisture to permeate therebetween. The moisture may thereafter expand when the package device is exposed to high heat conditions, e.g., during later processing, causing the insulation and/or redistribution layer to delaminate, or separate, from the frame, thus severely compromising the structural integrity and electrical performance of the semiconductor package device. By forming the coupling layer 316 between the substrate 302 and, e.g., the insulating layer 1018, adhesion of the insulating layer 1018 to the substrate 302 is improved, thereby enhancing the thermo-mechanical reliability of the final semiconductor package device. Additionally, the coupling layer 316 provides an additional protective barrier around the substrate 302, and mitigates any stresses thereon which may be caused by expansion and/or warping of the insulating layer 1018.

[0069] In certain embodiments, the coupling layer 316 comprises one or more silane coupling agents, which can generate a water-resistance interface between the organic polymer of an insulating layer, e.g., insulating layer 1018, and the inorganic

substrate, e.g., substrate 302, as they are able to react or interact with both the substrate and polymer. Silane coupling agents are organosilicon compounds that include both an organic functional group for reacting/interacting with organic materials, e.g., an insulation and/or redistribution layer, and a hydrolysable group for reacting/interacting with inorganic materials, e.g., a silicon-based frame. In certain embodiments, a silane coupling agent may have the general structure $X_3-Si-(CH_2)_n-Y$, where X is the hydrolysable group such as methoxy or ethoxy, Y is the functional group, and n equals 0-3. Examples of suitable functional groups include a vinyl group, an epoxy or epoxide group, a styryl group, an acryloyl group, a methacryl group, a methacryloyl group, an amino group, a phenyl group, a ureido group, an isocyanate group, an isocyanurate group, a mercapto group, and the like. In specific embodiments, the coupling layer 316 may include dodecyltrimethoxysilane, octadecyltrimethoxysilane, n-octyltriethoxysilane, methyltrimethoxysilane, methyltriethoxysilane, γ -methacryloxypropyltrimethoxysilane, vinyltriacetoxysilane, vinyltrimethoxysilane, vinyltriethoxysilane, dichloromethylvinylsilane, dimethoxymethylvinylsilane, diethoxymethylvinylsilane, chlorodimethylvinylsilane, vinyltrichlorosilane, vinyltri(2-methoxyethoxy)silane, 1,3,5,7-tetravinyl-1,3,5,7-tetramethylcyclotetrasiloxane, γ -isocyanatepropyltriethoxysilane, γ -glycidoxypropyltrimethoxysilane, β -(3,4-epoxycyclohexyl)ethyltrimethoxysilane, phenyltrichlorosilane, phenyltrimethoxysilane, phenyltriethoxysilane, dichlorodiphenylsilane, diphenyldimethoxysilane, diphenyldiethoxysilane, methylphenyldimethoxysilane, methylphenyldiethoxysilane, 3-aminopropyltriethoxysilane, n-2-(aminoethyl)-3-aminopropyltrimethoxysilane, n-2-(aminoethyl)-3-aminopropyltriethoxysilane, n-2-(aminoethyl)-3-aminopropylmethyltrimethoxysilane, 3-aminopropyltrimethoxysilane, 3-aminopropylmethyltrimethoxysilane, 3-aminopropylmethyltriethoxysilane, 3-ureidopropyltrimethoxysilane, 3-ureidopropyltriethoxysilane, 3-glycidoxypropyl trimethoxysilane, 3-glycidoxypropyl methyltrimethoxysilane, 3-glycidoxypropylmethyltriethoxysilane, 3-glycidoxypropylmethylmethyltrimethoxysilane, 3-glycidoxypropylmethylmethyltriethoxysilane, 2-(3,4-epoxycyclohexyl)ethyl trimethoxysilane, 2-(3,4-epoxycyclohexyl)ethyltriethoxysilane, 2-(3,4-epoxycyclohexyl)ethylmethyltrimethoxysilane, 2-(3,4-epoxycyclohexyl)ethylmethyltriethoxysilane, 3-methacryloxypropyltrimethoxysilane, 3-methacryloxypropylmethyltrimethoxysilane, 3-

methacryloxypropylmethyldiethoxysilane, 3-methacryloxypropyltriethoxysilane, bis[3-(triethoxysilyl)propyl]tetrasulfide, bis[3-(triethoxysilyl)propyl]sulfide, 3-mercaptopropyltrimethoxysilane, 3-mercaptopropyltriethoxysilane, 1,2-bis(trimethoxysilyl)ethane, 1,2-bis(triethoxysilyl)ethane, tetramethoxysilane, tetraethoxysilane, tetrapropoxysilane, trimethoxysilane, triethoxysilane, and the like.

[0070] Generally, the coupling layer 316 may be formed by any suitable methods, including any suitable chemical and/or deposition processes, as well as self-assembly. In certain embodiments, the coupling layer 316 is formed by sol-gel, or one or more other chemical processes. In certain embodiments, the coupling layer 316 is formed by chemical vapor deposition (CVD), or other deposition processes. In certain embodiments, organosilane self-assembled monolayers (SAMs) are formed over a surface of the substrate 302 via liquid phase deposition (LPD) or vapor phase deposition (VPD). In LPD, silane may be diluted in solvent and the substrate 302 may be immersed in the solution thereafter for a desired period of time. In VPD, silane may be evaporated by, e.g., application of heat, and the substrate 302 may thereafter be exposed to the vapor.

[0071] After formation of the coupling layer 316, the substrate 302 may proceed to method 900 or method 1100 described below, wherein an embedded die assembly 1002 is formed utilizing the substrate 302 as a frame.

[0072] FIG. 8 illustrates a schematic top view of an exemplary structured substrate 302 according to one embodiment. The substrate 302 may be structured during operations 210-240 as described above with reference to FIGs. 2, 3A-3D, 4A-4F, 5A-5F, 6A-6E, and 7A-7D. The substrate 302 is illustrated as having two quadrilateral cavities 305, and each cavity 305 is surrounded by a plurality of vias 303. In certain embodiments, each cavity 305 is surrounded by two rows 801, 802 of vias 303 arranged along each edge 306a-d of the quadrilateral cavity 305. Although ten vias 303 are depicted in each row 801, 802, it is contemplated that any desired number of vias 303 may be formed in a row. Further, any desired number and arrangement of cavities 305 and vias 303 may be formed in the substrate 302 during operation 220. For example, the substrate 302 may have more or less than two cavities 305 formed therein. In another example, the substrate 302 may have more or less than two rows of vias 303 formed along each edge 306a-d of the cavities 305. In another example,

the substrate 302 may have two or more rows of vias 303 wherein the vias 303 in each row are staggered and unaligned with vias 303 of another row.

[0073] In certain embodiments, the cavities 305 and vias 303 have a depth equal to the thickness of the substrate 302, thus forming holes on opposing surfaces of the substrate 302 (e.g., through the thickness of the substrate 302). For example, the cavities 305 and the vias 303 formed in the substrate 302 may have a depth of between about 50 μm and about 1 mm, such as between about 100 μm and about 200 μm , such as between about 110 μm and about 190 μm , depending on the thickness of the substrate 302. In other embodiments, the cavities 305 and/or the vias 303 may have a depth equal to or less than the thickness of the substrate 302, thus forming a hole in only one surface (e.g., side) of the substrate 302.

[0074] In certain embodiments, each cavity 305 has lateral dimensions ranging between about 3 mm and about 50 mm, such as between about 8 mm and about 12 mm, such as between about 9 mm and about 11 mm, depending on the size of one or more semiconductor dies 1026 (shown in FIG. 10B) to be embedded therein during package fabrication (described in greater detail below). Semiconductor dies generally include a plurality of integrated electronic circuits that are formed on and/or within a substrate material, such as a piece of semiconductor material. In certain embodiments, the cavities 305 are sized to have lateral dimensions substantially similar to that of the dies 1026 to be embedded therein. For example, each cavity 305 is formed having lateral dimensions exceeding those of the dies 1026 by less than about 150 μm , such as less than about 120 μm , such as less than 100 μm . Having a reduced variance in the size of the cavities 305 and the dies 1026 to be embedded therein reduces the amount of gap-fill material utilized thereafter.

[0075] In certain embodiments, each via 303 has a diameter ranging between about 50 μm and about 200 μm , such as between about 60 μm and about 130 μm , such as between about 80 μm and 110 μm . A minimum pitch 807 between the center of a via 303 in row 801 and a center of an adjacent via 303 in row 802 is between about 70 μm and about 200 μm , such as between about 85 μm and about 160 μm , such as between about 100 μm and 140 μm . Although embodiments are described with reference to FIG. 8, the substrate structuring processes described above with reference to operations 210-240 and FIGs. 2, 3A-3B, 4A-4C, 5A-5C, 6A-6C, and 7A-

7B may be utilized to form patterned features in the substrate 302 having any desired depth, lateral dimensions, and morphologies.

[0076] FIGs. 9 and 11 illustrate flow diagrams of representative methods 900 and 1100, respectively, for fabricating an intermediary embedded die assembly 1002 around the substrate 302 prior to final package formation. FIGs. 10A-10K schematically illustrate cross-sectional views of the substrate 302 at different stages of the method 900 depicted in FIG. 9, and FIGs. 12A-12G schematically illustrate cross-sectional views of the substrate 302 at different stages of the method 1100 depicted in FIG. 11. For clarity, FIG. 9 and FIGs. 10A-10K are herein described together and FIG. 11 and FIGs. 12A-12G are herein described together.

[0077] The method 900 begins at operation 902 and FIG. 10A wherein a first side 1075 of the substrate 302, now having desired features formed therein and a coupling layer 316 formed thereon, is placed on a first insulating film 1016a. In certain embodiments, the first insulating film 1016a includes one or more layers formed of polymer-based dielectric materials. For example, the first insulating film 1016a includes one or more layers formed of flowable build-up materials. In the embodiment depicted in FIG. 10A, the first insulating film 1016a includes a flowable layer 1018a. The flowable layer 1018a may be formed of a ceramic-filler-containing epoxy resin, such as an epoxy resin filled with (e.g., containing) silica (SiO_2) particles. Other examples of ceramic fillers or particles that may be utilized to form the flowable layer 1018a and other layers of the insulating film 1016a include aluminum nitride (AlN), aluminum oxide (Al_2O_3), silicon carbide (SiC), silicon nitride (Si_3N_4), $\text{Sr}_2\text{Ce}_2\text{Ti}_5\text{O}_{16}$, zirconium silicate (ZrSiO_4), wollastonite (CaSiO_3), beryllium oxide (BeO), cerium dioxide (CeO_2), boron nitride (BN), calcium copper titanium oxide ($\text{CaCu}_3\text{Ti}_4\text{O}_{12}$), magnesium oxide (MgO), titanium dioxide (TiO_2), zinc oxide (ZnO) and the like. In some examples, the ceramic fillers utilized to form the flowable layer 1018a have particles ranging in size between about 40 nm and about 1.5 μm , such as between about 80 nm and about 1 μm . For example, the ceramic fillers utilized to form the flowable layer 1018a have particles ranging in size between about 200 nm and about 800 nm, such as between about 300 nm and about 600 nm. In some embodiments, the ceramic fillers utilized to form the flowable layer 1018a include particles having a size less than about 25% of the desired feature (e.g., via, cavity, or through-assembly

via) width or diameter, such as less than about 15% of the desired feature width or diameter.

[0078] The flowable layer 1018a typically has a thickness less than about 60 μm , such as between about 5 μm and about 50 μm . For example, the flowable layer 1018a has a thickness between about 10 μm and about 25 μm . In certain embodiments, the insulating film 1016a further includes one or more support layers. For example, the insulating film 1016a includes a polyethylene terephthalate (PET) or similar lightweight plastic support layer 1022a. However, any suitable combination of layers and insulating materials is contemplated for the insulating film 1016a. In some embodiments, the entire insulating film 1016a has a thickness less than about 120 μm , such as a thickness less than about 90 μm .

[0079] The substrate 302, which is coupled to the insulating film 1016a on the first side 1075 thereof, and specifically to the flowable layer 1018a of the insulating film 1016a, may further be optionally placed on a carrier 1024 for mechanical support during later processing operations. The carrier is formed of any suitable mechanically and thermally stable material. For example, the carrier 1024 is formed of polytetrafluoroethylene (PTFE). In another example, the carrier 1024 is formed of PET.

[0080] At operation 904 and depicted in FIG. 10B, one or more semiconductor dies 1026 are placed within the cavities 305 formed in the substrate 302, so that the semiconductor dies 1026 are now bound by the insulating film 1016a on one side (a single semiconductor die 1026 is depicted in Figure 10B). In certain embodiments, the dies 1026 are multipurpose dies having integrated circuits formed on an active surface 1028 thereof. The dies 1026 are placed within the cavities 305 and positioned onto a surface of the insulating film 1016a exposed through the cavities 305. In certain embodiments, the dies 1026 are placed on an adhesive layer (not shown) disposed or formed on the insulating film 1016a.

[0081] After placement of the dies 1026 within the cavities 305, a first protective film 1060 is placed over a second side 1077 (e.g., over surface 608) of the substrate 302 at operation 906 and FIG. 10C. The protective film 1060 is coupled to the second side 1077 of the substrate 302 and opposite of the first insulating film 1016a such that

it contacts and covers the active surfaces 1028 of the dies 1026 disposed within the cavities 305. In certain embodiments, the protective film 1060 is formed of a similar material to that of the support layer 1022a. For example, the protective film 1060 is formed of PET, such as biaxial PET. However, the protective film 1060 may be formed of any suitable protective materials. In some embodiments, the protective film 1060 has a thickness between about 50 μm and about 150 μm .

[0082] The substrate 302, now affixed to the insulating film 1016a on the first side 1075 and the protective film 1060 on the second side 1077 and further having dies 1026 disposed therein, is exposed to a lamination process at operation 908 to adhere the insulating film 1016 to the substrate 302, and more particularly, the coupling layer 316 formed on the substrate 302. During the lamination process, the substrate 302 is exposed to elevated temperatures, causing the flowable layer 1018a of the insulating film 1016a to soften and flow into the open voids or volumes between the insulating film 1016a and the protective film 1060, such as into the vias 303 and gaps 1051 between the interior walls of the cavities 305 and the dies 1026. Accordingly, the semiconductor dies 1026 become at least partially embedded within the material of the insulating film 1016a and the substrate 302, as depicted in FIG. 10D.

[0083] In certain embodiments, the lamination process is a vacuum lamination process that may be performed in an autoclave or other suitable device. In certain embodiments, the lamination process is performed by use of a hot pressing process. In certain embodiments, the lamination process is performed at a temperature of between about 80 $^{\circ}\text{C}$ and about 140 $^{\circ}\text{C}$ and for a period between about 5 seconds and about 1.5 minutes, such as between about 30 seconds and about 1 minute. In some embodiments, the lamination process includes the application of a pressure of between about 1 psig and about 50 psig while a temperature of between about 80 $^{\circ}\text{C}$ and about 140 $^{\circ}\text{C}$ is applied to substrate 302 and insulating film 1016a for a period between about 5 seconds and about 1.5 minutes. For example, the lamination process is performed at a pressure of between about 5 psig and about 40 psig, a temperature of between about 100 $^{\circ}\text{C}$ and about 120 $^{\circ}\text{C}$ for a period between about 10 seconds and about 1 minute. For example, the lamination process is performed at a temperature of about 110 $^{\circ}\text{C}$ for a period of about 20 seconds.

[0084] At operation 910, the protective film 1060 is removed and the substrate 302, now having the laminated insulating material of the flowable layer 1018a at least partially surrounding the substrate 302 and the one or more dies 1026, is placed on a second protective film 1062. As depicted in FIG. 10E, the second protective film 1062 is coupled to the first side 1075 of the substrate 302 such that the second protective film 1062 is disposed against (e.g., adjacent) the support layer 1022a of the insulating film 1016a. In some embodiments, the substrate 302, now coupled to the protective film 1062, may be optionally placed on the carrier 1024 for additional mechanical support on the first side 1075. In some embodiments, the protective film 1062 is placed on the carrier 1024 prior to coupling the protective film 1062 with the substrate 302, now laminated with the insulating film 1016a. Generally, the protective film 1062 is substantially similar in composition to the protective film 1060. For example, the protective film 1062 may be formed of PET, such as biaxial PET. However, the protective film 1062 may be formed of any suitable protective materials. In some embodiments, the protective film 1062 has a thickness between about 50 μm and about 150 μm .

[0085] Upon coupling the substrate 302 to the second protective film 1062, a second insulating film 1016b substantially similar to the first insulating film 1016a is placed on the second side 1077 of the substrate 302 at operation 912 and FIG. 10F, thus replacing the protective film 1060. In certain embodiments, the second insulating film 1016b is positioned on the second side 1077 of the substrate 302 such that a flowable layer 1018b of the second insulating film 1016b contacts and covers the active surface 1028 of the dies 1026 within the cavities 305. In certain embodiments, the placement of the second insulating film 1016b on the substrate 302 may form one or more voids between the insulating film 1016b and the already-laminated insulating material of the flowable layer 1018a partially surrounding the one or more dies 1026. The second insulating film 1016b may include one or more layers formed of flowable, polymer-based dielectric materials. As depicted in FIG. 10F, the second insulating film 1016b includes a flowable layer 1018b which is similar to the flowable layer 1018a described above. The second insulating film 1016b may further include a support layer 1022b formed of similar materials to the support layer 1022a, such as PET or other lightweight plastic materials.

[0086] At operation 914, a third protective film 1064 is placed over the second insulating film 1016b, as depicted in FIG. 10G. Generally, the protective film 1064 is substantially similar in composition to the protective films 1060, 1062. For example, the protective film 1064 is formed of PET, such as biaxial PET. However, the protective film 1064 may be formed of any suitable protective materials. In some embodiments, the protective film 1064 has a thickness between about 50 μm and about 150 μm .

[0087] The substrate 302, now affixed to the insulating film 1016b and support layer 1064 on the second side 1077 and the protective film 1062 and optional carrier 1024 on the first side 1075, is exposed to a second lamination process at operation 916 and FIG. 10H. Similar to the lamination process at operation 908, the substrate 302 is exposed to elevated temperatures, causing the flowable layer 1018b of the insulating film 1016b to soften and flow into any open voids or volumes between the insulating film 1016b and the already-laminated insulating material of the flowable layer 1018a, thus integrating itself with the insulating material of the flowable layer 1018a. Accordingly, the cavities 305 and the vias 303 become filled (e.g. packed, sealed) with insulating material, and the semiconductor dies 1026 previously placed within the cavities 305 become entirely embedded within the insulating material of the flowable layers 1018a, 1018b.

[0088] In certain embodiments, the lamination process is a vacuum lamination process that may be performed in an autoclave or other suitable device. In certain embodiments, the lamination process is performed by use of a hot pressing process. In certain embodiments, the lamination process is performed at a temperature of between about 80 $^{\circ}\text{C}$ and about 140 $^{\circ}\text{C}$ and for a period between about 1 minute and about 30 minutes. In some embodiments, the lamination process includes the application of a pressure of between about 10 psig and about 150 psig while a temperature of between about 80 $^{\circ}\text{C}$ and about 140 $^{\circ}\text{C}$ is applied to substrate 302 and insulating film 1016 b for a period between about 1 minute and about 30 minutes. For example, the lamination process is performed at a pressure of between about 20 psig and about 100 psig, a temperature of between about 100 $^{\circ}\text{C}$ and about 120 $^{\circ}\text{C}$ for a period between about 2 minutes and 10 minutes. For example, the lamination process is performed at a temperature of about 110 $^{\circ}\text{C}$ for a period of about 5 minutes.

[0089] After lamination, the substrate 302 is disengaged from the carrier 1024 and the protective films 1062, 1064 are removed at operation 918, resulting in a laminated embedded die assembly 1002. As depicted in FIG. 10I, the embedded die assembly 1002 includes the substrate 302 having one or more cavities 305 and/or vias 303 formed therein and filled with the insulating dielectric material of the flowable layers 1018a, 1018b, as well as the embedded dies 1026 within the cavities 305. The insulating dielectric material of the flowable layers 1018a, 1018b encases the substrate 302 (and the coupling layer 316) such that the insulating material is disposed over at least two surfaces or sides of the substrate 302, such as the two major surfaces 606, 608, and covers all sides of the embedded semiconductor dies 1026. In some examples, the support layers 1022a, 1022b are also removed from the embedded die assembly 1002 at operation 918. Generally, the support layers 1022a and 1022b, the carrier 1024, and the protective films 1062 and 1064 are removed from the embedded die assembly 1002 by any suitable mechanical processes, such as peeling therefrom.

[0090] Upon removal of the support layers 1022a, 1022b and the protective films 1062, 1064, the embedded die assembly 1002 is exposed to a cure process to fully cure (i.e. harden through chemical reactions and cross-linking) the insulating dielectric material of the flowable layers 1018a, 1018b, thus forming a cured insulating layer 1018. The insulating layer 1018 substantially surrounds the substrate 302 and the semiconductor dies 1026 embedded therein. For example, the insulating layer 1018 contacts or encapsulates at least the sides 1075, 1077 of the substrate 302 (including surfaces 606, 608) and at least six sides or surfaces of each semiconductor die 1026, which has a rectangular prism shape as illustrated in Figure 10H (i.e., only four surfaces 1028 and 1029 shown in 2D view).

[0091] In certain embodiments, the cure process is performed at high temperatures to fully cure the embedded die assembly 1002. For example, the cure process is performed at a temperature of between about 140 °C and about 220 °C and for a period between about 15 minutes and about 45 minutes, such as a temperature of between about 160 °C and about 200 °C and for a period between about 25 minutes and about 35 minutes. For example, the cure process is performed at a temperature of about 180 °C for a period of about 30 minutes. In further embodiments, the cure

process at operation 916 is performed at or near ambient (e.g. atmospheric) pressure conditions.

[0092] After curing, one or more through-assembly vias 1003 are drilled through the embedded die assembly 1002 at operation 920, forming channels through the entire thickness of the embedded die assembly 1002 for subsequent interconnection formation. In some embodiments, the embedded die assembly 1002 may be placed on a carrier, such as the carrier 1024, for mechanical support during the formation of the through-assembly vias 1003 and subsequent contact holes 1032. The through-assembly vias 1003 are drilled through the vias 303 that were formed in the substrate 302 and subsequently filled with the insulating layer 1018. Thus, the through-assembly vias 1003 may be circumferentially surrounded by the insulating layer 1018 filled within the vias 303, as well as the coupling layer 316 and the substrate 302. By having the ceramic-filler-containing epoxy resin material of the insulating layer 1018 line the walls of the vias 303, capacitive coupling between the conductive silicon-based substrate 302 and interconnections 1444 (described with reference to FIG. 13 and FIGs. 14E – 14H), and thus capacitive coupling between adjacently positioned vias 303 and/or redistribution connections 1644 (described with reference to FIG. 15 and FIGs. 16H – 16L), in the completed package 1602 (described with reference to FIG. 15 and FIGs. 16K and 16L) is significantly reduced as compared to other conventional interconnecting structures that utilize conventional via insulating liners or films. Furthermore, the flowable nature of the epoxy resin material enables more consistent and reliable encapsulation and insulation, thus enhancing electrical performance by minimizing leakage current of the completed package 1602.

[0093] In certain embodiments, the through-assembly vias 1003 have a diameter less than about 100 μm , such as less than about 75 μm . For example, the through-assembly vias 1003 have a diameter less than about 60 μm , such as less than about 50 μm . In certain embodiments, the through-assembly vias 1003 have a diameter of between about 25 μm and about 50 μm , such as a diameter of between about 35 μm and about 40 μm . In certain embodiments, the through assembly vias 1003 are formed using any suitable mechanical process. For example, the through-assembly vias 1003 are formed using a mechanical drilling process. In certain embodiments, through-assembly vias 1003 are formed through the embedded die assembly 1002 by

laser ablation. For example, the through-assembly vias 1003 are formed using an ultraviolet laser. In certain embodiments, the laser source utilized for laser ablation has a frequency between about 5 kHz and about 500 kHz. In certain embodiments, the laser source is configured to deliver a pulsed laser beam at a pulse duration between about 10 ns and about 100 ns with a pulse energy of between about 50 microjoules (μJ) and about 500 μJ . Utilizing an epoxy resin material having small ceramic filler particles further promotes more precise and accurate laser patterning of small-diameter vias, such as the vias 1003, as the small ceramic filler particles therein exhibit reduced laser light reflection, scattering, diffraction and transmission of the laser light away from the area in which the via is to be formed during the laser ablation process.

[0094] At operation 922 and FIG. 10K, one or more contact holes 1032 are drilled through the insulating layer 1018 to expose one or more contacts 1030 formed on the active surface 1028 of each embedded die 1026. The contact holes 1032 are drilled through the insulating layer 1018 by laser ablation, leaving all external surfaces of the semiconductor dies 1026 covered and surrounded by the insulating layer 1018 and the contacts 1030 exposed. Thus, the contacts 1030 are exposed by the formation of the contact holes 1032. In certain embodiments, the laser source may generate a pulsed laser beam having a frequency between about 100 kHz and about 1000 kHz. In certain embodiments, the laser source is configured to deliver a pulsed laser beam at a wavelength of between about 100 nm and about 2000 nm, at a pulse duration between about $10\text{E-}4$ ns and about $10\text{E-}2$ ns, and with a pulse energy of between about 10 μJ and about 300 μJ . In certain embodiments, the contact holes 1032 are drilled using a CO_2 , green, or UV laser. In certain embodiments, the contact holes 1032 have a diameter of between about 5 μm and about 60 μm , such as a diameter of between about 20 μm and about 50 μm .

[0095] After formation of the contact holes 1032, the embedded die assembly 1002 is exposed to a de-smear process at operation 922 to remove any unwanted residues and/or debris caused by laser ablation during the formation of the through-assembly vias 1003 and the contact holes 1032. The de-smear process thus cleans the through-assembly vias 1003 and contact holes 1032 and fully exposes the contacts 1030 on the active surfaces 1028 of the embedded die 1026 for subsequent metallization. In

certain embodiments, the de-smear process is a wet de-smear process. Any suitable aqueous etchants, solvents, and/or combinations thereof may be utilized for the wet de-smear process. In one example, potassium permanganate (KMnO_4) solution may be utilized as an etchant. Depending on the residue thickness, exposure of the embedded die assembly 1002 to the wet de-smear process at operation 922 may be varied. In another embodiment, the de-smear process is a dry de-smear process. For example, the de-smear process may be a plasma de-smear process with an $\text{O}_2:\text{CF}_4$ mixture gas. The plasma de-smear process may include generating a plasma by applying a power of about 700W and flowing $\text{O}_2:\text{CF}_4$ at a ratio of about 10:1 (e.g., 100:10 sccm) for a time period between about 60 seconds and about 120 seconds. In further embodiments, the de-smear process is a combination of wet and dry processes.

[0096] Following the de-smear process at operation 922, the embedded die assembly 1002 is ready for formation of interconnection paths therein, described below with reference to FIG. 13 and FIGs. 14A-14H.

[0097] As discussed above, FIG. 9 and FIG. 10A – 10K illustrate a representative method 900 for forming the intermediary embedded die assembly 1002. FIG. 11 and FIGs. 12A – 12G illustrate an alternative method 1100 substantially similar to the method 900 but with fewer operations. The method 1100 generally includes eight operations 1110-1180. However, operations 1110, 1120, 1160, and 1190 of the method 1100 are substantially similar to the operations 902, 904, 920, and 922 of the method 900, respectively. Thus, only operations 1130, 1140, and 1150, depicted in FIGs. 12C, 12D, and 12E, respectively, are herein described for clarity.

[0098] After placement of the one or more semiconductor dies 1026 onto a surface of the insulating film 1016a exposed through the cavities 305, the second insulating film 1016b is positioned over the second side 1077 of the substrate 302 at operation 1130 and FIG. 12C, prior to lamination. In some embodiments, the second insulating film 1016b is positioned on the second side 1077 of the substrate 302 such that the flowable layer 1018b of the second insulating film 1016b contacts and covers the active surface 1028 of the dies 1026 within the cavities 305. In some embodiments, a second carrier 1025 is affixed to the support layer 1022b of the second insulating film 1016b for additional mechanical support during later processing operations. As

depicted in FIG. 12C, one or more voids 1050 are formed between the insulating films 1016a and 1016b through the vias 303 and gaps 1051 between the semiconductor dies 1026 and interior walls of the cavities 305.

[0099] At operation 1140 and FIG. 12D, the substrate 302, now affixed to the insulating films 1016a and 1016b and having dies 1026 disposed therein, is exposed to a single lamination process to adhere both insulating films 1016a and 1016b to the substrate 302, and more particularly, the coupling layer 316. During the single lamination process, the substrate 302 is exposed to elevated temperatures, causing the flowable layers 1018a and 1018b of both insulating films 1016a, 1016b to soften and flow into the open voids or volumes between the insulating films 1016a, 1016b, such as into the vias 303 and gaps 1051 between the interior walls of the cavities 305 and the dies 1026. Accordingly, the semiconductor dies 1026 become embedded within the material of the insulating films 1016a, 1016b and the vias 303 filled therewith.

[0100] Similar to the lamination processes described with reference to FIG. 9 and FIGs. 10A-10K, the lamination process at operation 1140 may be a vacuum lamination process that may be performed in an autoclave or other suitable device. In another embodiment, the lamination process is performed by use of a hot pressing process. In certain embodiments, the lamination process is performed at a temperature of between about 80 °C and about 140 °C and for a period between about 1 minute and about 30 minutes. In some embodiments, the lamination process includes the application of a pressure of between about 1 psig and about 150 psig while a temperature of between about 80 °C and about 140 °C is applied to substrate 302 and insulating film 1016a, 1016b layers for a period between about 1 minute and about 30 minutes. For example, the lamination process is performed at a pressure of between about 10 psig and about 100 psig, a temperature of between about 100 °C and about 120 °C for a period between about 2 minutes and 10 minutes. For example, the lamination process is performed at a temperature of about 110 °C for a period of about 5 minutes.

[0101] At operation 1150, the one or more support layers of the insulating films 1016a and 1016b are removed from the substrate 302, resulting in the laminated embedded die assembly 1002. As depicted in FIG. 12E, the embedded die assembly

1002 includes the substrate 302 having one or more cavities 305 and/or vias 303 formed therein and filled with the insulating dielectric material of the flowable layers 1018a, 1018b, as well as the embedded dies 1026 within the cavities 305. The insulating material encases the substrate 302 such that the insulating material covers at least two surfaces or sides of the substrate 302, for example surfaces 606, 608. In one example, the support layers 1022a, 1022b are removed from the embedded die assembly 1002, and thus the embedded die assembly 1002 is disengaged from the carriers 1024, 1025. Generally, the support layers 1022a, 1022b and the carriers 1024, 1025 are removed by any suitable mechanical processes, such as peeling therefrom.

[0102] Upon removal of the support layers 1022a, 1022b, the embedded die assembly 1002 is exposed to a cure process to fully cure the insulating dielectric material of the flowable layers 1018a, 1018b. Curing of the insulating material results in the formation of the cured insulating layer 1018. As depicted in FIG. 12E and similar to operation 918 corresponding with FIG. 10I, the insulating layer 1018 substantially surrounds the substrate 302 and the semiconductor dies 1026 embedded therein.

[0103] In certain embodiments, the cure process is performed at high temperatures to fully cure the embedded die assembly 1002. For example, the cure process is performed at a temperature of between about 140 °C and about 220 °C and for a period between about 15 minutes and about 45 minutes, such as a temperature of between about 160 °C and about 200 °C and for a period between about 25 minutes and about 35 minutes. For example, the cure process is performed at a temperature of about 180 °C for a period of about 30 minutes. In further embodiments, the cure process at operation 1150 is performed at or near ambient (e.g. atmospheric) pressure conditions.

[0104] After curing at operation 1150, the method 1100 is substantially similar to operations 920 and 922 of the method 900. For example, the embedded die assembly 1002 has one or more through-assembly vias 1003 and one or more contact holes 1032 drilled through the insulating layer 1018. Subsequently, the embedded die assembly 1002 is exposed to a de-smear process, after which the embedded die assembly 1002 is ready for formation of interconnection paths therein, as described below.

[0105] FIG. 13 illustrates a flow diagram of a representative method 1300 of forming electrical interconnections through the embedded die assembly 1002. FIGs. 14A-14H schematically illustrate cross-sectional views of the embedded die assembly 1002 at different stages of the process of the method 1300 depicted in FIG. 13. Thus, FIG. 13 and FIGs. 14A-14H are herein described together for clarity.

[0106] In certain embodiments, the electrical interconnections formed through the embedded die assembly 1002 are formed of copper. Thus, the method 1300 may optionally begin at operation 1310 and FIG. 14A wherein the embedded die assembly 1002, having through-assembly vias 1003 and contact holes 1032 formed therein, has an adhesion layer 1440 and/or a seed layer 1442 formed thereon. An enlarged partial view of the adhesion layer 1440 and the seed layer 1442 formed on the embedded die assembly 1002 is depicted in FIG. 14H for reference. The adhesion layer 1440 may be formed on desired surfaces of the insulating layer 1018, such as major surfaces 1005, 1007 of the embedded die assembly 1002, as well as on the active surfaces 1028 of the contact holes 1032 on each die 1026 and interior walls of the through-assembly vias 1003, to assist in promoting adhesion and blocking diffusion of the subsequently formed seed layer 1442 and copper interconnections 1444. Thus, in certain embodiments, the adhesion layer 1440 acts as an adhesion layer; in another embodiment, the adhesion layer 1440 acts as a barrier layer. In both embodiments, however, the adhesion layer 1440 will be hereinafter described as an "adhesion layer."

[0107] In certain embodiments, the optional adhesion layer 1440 is formed of titanium, titanium nitride, tantalum, tantalum nitride, manganese, manganese oxide, molybdenum, cobalt oxide, cobalt nitride, or any other suitable materials or combinations thereof. In certain embodiments, the adhesion layer 1440 has a thickness of between about 10 nm and about 300 nm, such as between about 50 nm and about 150 nm. For example, the adhesion layer 1440 has a thickness between about 75 nm and about 125 nm, such as about 100 nm. The adhesion layer 1440 is formed by any suitable deposition process, including but not limited to chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD), or the like.

[0108] The optional seed layer 1442 may be formed on the adhesion layer 1440 or directly on the insulating layer 1018 (e.g., without the formation of the adhesion

layer 1440). The seed layer 1442 is formed of a conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. In certain embodiments, the seed layer 1442 has a thickness between about 50 nm and about 500 nm, such as between about 100 nm and about 300 nm. For example, the seed layer 1442 has a thickness between about 150 nm and about 250 nm, such as about 200 nm. In certain embodiments, the seed layer 1442 has a thickness of between about 0.1 μm and about 1.5 μm . Similar to the adhesion layer 1440, the seed layer 1442 is formed by any suitable deposition process, such as CVD, PVD, PECVD, ALD dry processes, wet electroless plating processes, or the like. In certain embodiments, a molybdenum adhesion layer 1440 is formed on the embedded die assembly in combination with a copper seed layer 1442. The Mo-Cu adhesion and seed layer combination enables improved adhesion with the surfaces of the insulating layer 1018 and reduces undercut of conductive interconnect lines during a subsequent seed layer etch process at operation 1370.

[0109] At operations 1320 and 1330, corresponding to FIGs. 14B and 14C, respectively, a spin-on/spray-on or dry resist film 1450, such as a photoresist, is applied on both major surfaces 1005, 1007 of the embedded die assembly 1002 and is subsequently patterned. In certain embodiments, the resist film 1450 is patterned via selective exposure to UV radiation. In certain embodiments, an adhesion promoter (not shown) is applied to the embedded die assembly 1002 prior to formation of the resist film 1450. The adhesion promoter improves adhesion of the resist film 1450 to the embedded die assembly 1002 by producing an interfacial bonding layer for the resist film 1450 and by removing any moisture from the surface of the embedded die assembly 1002. In some embodiments, the adhesion promoter is formed of bis(trimethylsilyl)amine or hexamethyldisilazane (HMDS) and propylene glycol monomethyl ether acetate (PGMEA).

[0110] At operation 1340 and FIG. 14D, the embedded die assembly 1002 is exposed to a resist film development process. As depicted in Figure 14D, development of the resist film 1450 results in exposure of the through-assembly vias 1003 and contact holes 1032, now having an adhesion layer 1440 and a seed layer 1442 formed thereon. In certain embodiments, the film development process is a wet process, such as a wet process that includes exposing the resist to a solvent. In

certain embodiments, the film development process is a wet etch process utilizing an aqueous etch process. In other embodiments, the film development process is a wet etch process utilizing a buffered etch process selective for a desired material. Any suitable wet solvents or combination of wet etchants may be used for the resist film development process.

[0111] At operations 1350 and 1360, corresponding to FIGs. 14E and 14F respectively, interconnections 1444 are formed through the exposed through-assembly vias 1003 and contact holes 1032 and the resist film 1450 is thereafter removed. The interconnections 1444 are formed by any suitable methods including electroplating and electroless deposition. In certain embodiments, the resist film 1450 is removed via a wet process. As depicted in FIGs. 14E and 14F, the formed interconnections 1444 fill the through-assembly vias 1003 and contact holes 1032 and/or cover inner circumferential walls thereof and protrude from the surfaces 1005, 1007, and 1028 of the embedded die assembly 1002 upon removal of the resist film 1450. In certain embodiments, the interconnections 1444 are formed of copper. In other embodiments, the interconnections 1444 may be formed of any suitable conductive material including but not limited to aluminum, gold, nickel, silver, palladium, tin, or the like.

[0112] At operation 1370 and FIG. 14G, the embedded die assembly 1002 having interconnections 1444 formed therein is exposed to an adhesion and/or seed layer etch process to remove the adhesion layer 1440 and the seed layer 1442. In certain embodiments, the seed layer etch is a wet etch process including a rinse and drying of the embedded die assembly 1002. In certain embodiments, the seed layer etch process is a buffered etch process selective for a desired material such as copper, tungsten, aluminum, silver, or gold. In other embodiments, the etch process is an aqueous etch process. Any suitable wet etchant or combination of wet etchants may be used for the seed layer etch process.

[0113] Following the seed layer etch process at operation 1370, one or more electrically functioning packages may be singulated from the embedded die assembly 1002. Alternatively, the embedded die assembly 1002 may have one or more redistribution layers 1658 and/or 1660 (shown in FIGs. 16K-16L) formed thereon as needed to enable rerouting of contact points of the interconnections 1444 to desired

locations on the surfaces of the embedded die assembly 1002. FIG. 15 illustrates a flow diagram of a representative method 1500 of forming a redistribution layer 1658 on the embedded die assembly 1002. FIGs. 16A-16L schematically illustrate cross-sectional views of the embedded die assembly 1002 at different stages of the method 1500 depicted in FIG. 15. Thus, FIG. 15 and FIGs. 16A-16L are herein described together for clarity.

[0114] The method 1500 is substantially similar to the methods 900, 1100, and 1300 described above. Generally, the method 1500 begins at operation 1502 and FIG. 16A, wherein an insulating film 1616 is placed on the embedded die assembly 1002 and thereafter laminated. The insulating film 1616 may be substantially similar to the insulating film 1016 and includes one or more layers formed of polymer-based flowable dielectric materials. In certain embodiments, as depicted in FIG. 16A, the insulating film 1616 includes a flowable layer 1618 and one or more support layers 1622. In certain embodiments, the insulating film 1616 may include a ceramic-filler-containing epoxy resin flowable layer 1618 and one or more support layers 1622. In another example, the insulating film 1616 may include a photodefinable polyimide flowable layer 1618 and one or more support layers 1622. The material properties of photodefinable polyimide enable the formation of smaller (e.g., narrower) vias through the resulting interconnect layer formed therefrom. However, any suitable combination of layers and insulating materials is contemplated for the insulating film 1616. For example, the insulating film 1616 may include a non-photosensitive polyimide, polybenzoxazole (PBO), silicon dioxide, and/or silicon nitride flowable layer 1618. Examples of suitable materials for the one or more support layers 1622 include PET and polypropylene (PP).

[0115] In some examples, the flowable layer 1618 includes a different polymer-based flowable dielectric material than the flowable layers 1018a, 1018b described above. For example, the flowable layer 1018 may include a ceramic-filler-containing epoxy resin and the flowable layer 1618 may include a photodefinable polyimide. In another example, the flowable layer 1618 is formed from a different inorganic dielectric material from the flowable layers 1018a, 1018b. For example, the flowable layers 1018a, 1018b may include a ceramic-filler-containing epoxy resin and the flowable layer 1618 may include a silicon dioxide layer.

[0116] The insulating film 1616 has a thickness of less than about 200 μm , such as a thickness between about 10 μm and about 180 μm . For example, the insulating film 1616 including the flowable layer 1618 and the PET support layer 1622 has a total thickness of between about 50 μm and about 100 μm . In certain embodiments, the flowable layer 1618 has a thickness of less than about 60 μm , such as a thickness between about 5 μm and about 50 μm , such as a thickness of about 20 μm . The insulating film 1616 is placed on a surface of the embedded die assembly 1002 having exposed interconnections 1444 that are coupled to the contacts 1030 on the active surface 1028 of dies 1026 and/or coupled to the metallized through-assembly vias 1003, such as the major surface 1005.

[0117] After placement of the insulating film 1616, the embedded die assembly 1002 is exposed to a lamination process substantially similar to the lamination process described with reference to operations 908, 916, and 1140. The embedded die assembly 1002 is exposed to elevated temperatures to soften the flowable layer 1618, which subsequently bonds to the insulating layer 1018 already formed on the embedded die assembly 1002. Thus, in certain embodiments, the flowable layer 1618 becomes integrated with the insulating layer 1018 and forms an extension thereof. The integration of the flowable layer 1618 and the insulating layer 1018 results in an expanded and integrated insulating layer 1018 covering the previously exposed interconnections 1444. Accordingly, the bonded flowable layer 1618 and the insulating layer 1018 will herein be jointly described as the insulating layer 1018. In other embodiments, however, the lamination and subsequent curing of the flowable 1618 forms a second insulating layer (not shown) on the insulating layer 1018. In some examples, the second insulating layer is formed of a different material layer than the insulating layer 1018.

[0118] In certain embodiments, the lamination process is a vacuum lamination process that may be performed in an autoclave or other suitable device. In certain embodiments, the lamination process is performed by use of a hot pressing process. In certain embodiments, the lamination process is performed at a temperature of between about 80 $^{\circ}\text{C}$ and about 140 $^{\circ}\text{C}$ and for a period between about 1 minute and about 30 minutes. In some embodiments, the lamination process includes the application of a pressure of between 10 psig and about 100 psig while a temperature

of between about 80 °C and about 140 °C is applied to the substrate 302 and insulating film 1616 for a period between about 1 minute and about 30 minutes. For example, the lamination process is performed at a pressure of between about 30 psig and about 80 psig and a temperature of between about 100 °C and about 120 °C for a period between about 2 minutes and about 10 minutes. For example, the lamination process is performed at a temperature of about 110 °C for a period of about 5 minutes. In further examples, the lamination process is performed at a pressure between about 30 psig and about 70 psig, such as about 50 psig.

[0119] At operation 1504 and FIG. 16B, the support layer 1622 and the carrier 1624 are removed from the embedded die assembly 1002 by mechanical processes. After removal of the support layer 1622 and carrier 1624, the embedded die assembly 1002 is exposed to a cure process to fully cure the newly expanded insulating layer 1018. In certain embodiments, the cure process is substantially similar to the cure process described with reference to operations 918 and 1150. For example, the cure process is performed at a temperature of between about 140 °C and about 220 °C and for a period between about 15 minutes and about 45 minutes, such as a temperature of between about 160 °C and about 200 °C and for a period between about 25 minutes and about 35 minutes. For example, the cure process is performed at a temperature of about 180 °C for a period of about 30 minutes. In further embodiments, the cure process at operation 1504 is performed at or near ambient pressure conditions.

[0120] The embedded die assembly 1002 is then selectively patterned by laser ablation at operation 1506 and FIG. 16C. The laser ablation at operation 1506 forms redistribution vias 1603 through the newly expanded insulating layer 1018 and exposes desired interconnections 1444 for redistribution of contact points thereof. In certain embodiments, the redistribution vias 1603 have a diameter of between about 5 μm and about 60 μm , such as a diameter of between about 10 μm and about 50 μm , such as between about 20 μm and about 45 μm . In certain embodiments, the laser ablation process at operation 1506 is performed utilizing a CO₂ laser. In certain embodiments, the laser ablation process at operation 1506 is performed utilizing a UV laser. In certain embodiments, the laser ablation process at operation 1506 is performed utilizing a green laser. For example, the laser source may generate a

pulsed laser beam having a frequency between about 100 kHz and about 1000 kHz. In one example, the laser source is configured to deliver a pulsed laser beam at a wavelength of between about 100 nm and about 2000 nm, at a pulse duration between about $10\text{E-}4$ ns and about $10\text{E-}2$ ns, and with a pulse energy of between about 10 μJ and about 300 μJ .

[0121] Upon patterning of the embedded die assembly 1002, the embedded die assembly 1002 is exposed to a de-smear process substantially similar to the de-smear process at operation 922 and 1180. During the de-smear process at operation 1506, any unwanted residues and debris formed by laser ablation during the formation of the redistribution vias 1603 are removed from the redistribution vias 1603 to clear (e.g., clean) the surfaces thereof for subsequent metallization. In certain embodiments, the de-smear process is a wet process. Any suitable aqueous etchants, solvents, and/or combinations thereof may be utilized for the wet de-smear process. In one example, KMnO_4 solution may be utilized as an etchant. In another embodiment, the de-smear process is a dry de-smear process. For example, the de-smear process may be a plasma de-smear process with an O_2/CF_4 mixture gas. In further embodiments, the de-smear process is a combination of wet and dry processes.

[0122] At operation 1508 and FIG. 16D, an optional adhesion layer 1640 and/or seed layer 1642 are formed on the insulating layer 1018. In certain embodiments, the adhesion layer 1640 is formed from titanium, titanium nitride, tantalum, tantalum nitride, manganese, manganese oxide, molybdenum, cobalt oxide, cobalt nitride, or any other suitable materials or combinations thereof. In certain embodiments, the adhesion layer 1640 has a thickness of between about 10 nm and about 300 nm, such as between about 50 nm and about 150 nm. For example, the adhesion layer 1640 has a thickness between about 75 nm and about 125 nm, such as about 100 nm. The adhesion layer 1640 may be formed by any suitable deposition process, including but not limited to CVD, PVD, PECVD, ALD, or the like.

[0123] The optional seed layer 1642 is formed from a conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. In certain embodiments, the seed layer 1642 has a thickness between about 50 nm and about 500 nm, such as between about 100 nm and about

300 nm. For example, the seed layer 1642 has a thickness between about 150 nm and about 250 nm, such as about 200 nm. In certain embodiments, the seed layer 1642 has a thickness of between about 0.1 μm and about 1.5 μm . Similar to the adhesion layer 1640, the seed layer 1642 may be formed by any suitable deposition process, such as CVD, PVD, PECVD, ALD dry processes, wet electroless plating processes, or the like. In certain embodiments, a molybdenum adhesion layer 1640 and a copper seed layer 1642 are formed on the embedded die assembly 1002 to reduce undercut of conductive interconnect lines during a subsequent seed layer etch process at operation 1520.

[0124] At operations 1510, 1512, and 1514, corresponding to FIGs. 16E, 16F, and 16G respectively, a spin-on/spray-on or dry resist film 1650, such as a photoresist, is applied over the adhesion and/or seed surfaces of the embedded die assembly 1002 and subsequently patterned and developed. In certain embodiments, an adhesion promoter (not shown) is applied to the embedded die assembly 1002 prior to placement of the resist film 1650. The exposure and development of the resist film 1650 results in opening of the redistribution vias 1603. Thus, patterning of the resist film 1650 may be performed by selectively exposing portions of the resist film 1650 to UV radiation, and subsequent development of the resist film 1650 by a wet process, such as a wet etch process. In certain embodiments, the resist film development process is a wet etch process utilizing a buffered etch process selective for a desired material. In other embodiments, the resist film development process is a wet etch process utilizing an aqueous etch process. Any suitable wet etchant or combination of wet etchants may be used for the resist film development process.

[0125] At operations 1516 and 1518, corresponding to FIGs. 16H and 16I respectively, redistribution connections 1644 are formed through the exposed redistribution vias 1603 and the resist film 1650 is thereafter removed. The redistribution connections 1644 are formed by any suitable methods including electroplating and electroless deposition. In certain embodiments, the resist film 1650 is removed via a wet process. As depicted in FIGs. 16H and 16I, the redistribution connections 1644 fill the redistribution vias 1603 and protrude from the surfaces of the embedded die assembly 1002 upon removal of the resist film 1650. In certain embodiments, the redistribution connections 1644 are formed of copper. In other

embodiments, the redistribution connections 1644 may be formed of any suitable conductive material including but not limited to aluminum, gold, nickel, silver, palladium, tin, or the like.

[0126] At operation 1520 and FIG. 16J, the embedded die assembly 1002 having the redistribution connections 1644 formed thereon is exposed to a seed layer etch process substantially similar to that of operation 1370. In certain embodiments, the seed layer etch is a wet etch process including a rinse and drying of the embedded die assembly 1002. In certain embodiments, the seed layer etch process is a wet etch process utilizing a buffered etch process selective for a desired material of the seed layer 1642. In other embodiments, the etch process is a wet etch process utilizing an aqueous etch process. Any suitable wet etchant or combination of wet etchants may be used for the seed layer etch process.

[0127] At operation 1522 and depicted in FIGs. 16K and 16L, one or more completed packages 1602 are singulated from the embedded die assembly 1002. Prior to operation 1522, however, additional redistribution layers may be formed on the embedded die assembly 1002 utilizing the sequences and processes described above, as depicted in FIG. 16L (FIG. 16K depicts the completed package 1602 having one additional redistribution layer 1658). For example, one or more additional redistribution layers 1660 may be formed on a side or surface of the embedded die assembly 1002 opposite of the first additional redistribution layer 1658, such as the major surface 1007. Alternatively, one or more additional redistribution layers 1660 may be formed on the same side or surface of the first additional redistribution layer 1658 (not shown), such as major surface 1005. The completed package 1602 may then be singulated from the embedded die assembly 1002 after all desired redistribution layers are formed.

[0128] FIG. 17 schematically illustrates an exemplary package fabrication system 1700 for use with the methods described herein. Utilization of system 1700 enables performance of the operations described herein in an efficient and streamlined manner, thereby facilitating improved fabrication of semiconductor package devices. The system 1700 may include one or more processing stations 1702 each configured to perform one or more operations for fabricating a semiconductor package device, such as package 1602. The processing stations 1702 may be disposed in sequence

with one or more transfer robots 1704 or other transfer devices disposed therebetween, or the processing stations 1702 may be arranged around a centrally-disposed transfer robot 1704 or transfer device, e.g., such as on a platform-type device, as shown in FIG. 17. In the example of FIG. 17, the system 1700 is shown with four processing stations 1702a, 1702b, 1702c, and 1702d, which may each be utilized for performing one or more different operations. For example, processing station 1702a may comprise a laser ablation system for structuring a substrate to be used as a package frame; processing station 1702b may comprise a coupling layer station, such as a CVD chamber, for forming a coupling layer on the substrate; processing station 1702c may comprise a lamination/curing system, such as a processing chamber or oven, for performing lamination and/or curing of insulating layers; and processing station 1702d may comprise a metallization station for plating or interconnections. However, fewer or additional processing stations are also contemplated.

[0129] Turning now to FIG.s 18A and 18B, the package structures formed by the methods described herein, e.g., package 1602, may be utilized in any suitable packaging applications and in any suitable configurations. In one exemplary embodiment depicted in FIG. 18A, four packages 1602 are utilized to form a stacked DRAM structure 1800. Accordingly, each package 1602 includes a memory die 1826 (i.e., memory chip) embedded within the substrate 302 and encapsulated by the insulating layer 1018 (e.g., having a portion of each side in contact with the insulating layer 1018). One or more interconnections 1444 are formed through the entire thickness of each package 1602 and are directly in contact with one or more solder bumps 1846 disposed between major surfaces 1005 and 1007 of adjacent (i.e., stacked above or below) packages 1602. For example, as depicted in the stacked DRAM structure 1800, four or more solder bumps 1846 are disposed between adjacent packages 1602 to bridge (e.g., connect, couple) the interconnections 1444 of each package 1602 with the interconnections 1444 of an adjacent package 1602.

[0130] In certain embodiments, voids between adjacent packages 1602 connected by the solder bumps 1846 are filled with an encapsulation material 1848 to enhance the reliability of the solder bumps 1846. The encapsulation material 1848 may be any suitable type of encapsulant or underfill. In one example, the encapsulation material

1848 includes a pre-assembly underfill material, such as a no-flow underfill (NUF) material, a nonconductive paste (NCP) material, and a nonconductive film (NCF) material. In one example, the encapsulation material 1848 includes a post-assembly underfill material, such as a capillary underfill (CUF) material and a molded underfill (MUF) material. In certain embodiments, the encapsulation material 1848 includes a low-expansion-filler-containing resin, such as an epoxy resin filled with (e.g., containing) SiO_2 , AlN , Al_2O_3 , SiC , Si_3N_4 , $\text{Sr}_2\text{Ce}_2\text{Ti}_5\text{O}_{16}$, ZrSiO_4 , CaSiO_3 , BeO , CeO_2 , BN , $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$, MgO , TiO_2 , ZnO and the like.

[0131] In certain embodiments, the solder bumps 1846 are formed of one or more intermetallic compounds, such as a combination of tin (Sn) and lead (Pb), silver (Ag), Cu, or any other suitable metals thereof. For example, the solder bumps 1846 are formed of a solder alloy such as Sn-Pb, Sn-Ag, Sn-Cu, or any other suitable materials or combinations thereof. In certain embodiments, the solder bumps 1846 include C4 (controlled collapse chip connection) bumps. In certain embodiments, the solder bumps 1846 include C2 (chip connection, such as a Cu-pillar with a solder cap) bumps. Utilization of C2 solder bumps enables a smaller pitch between contact pads and improved thermal and/or electrical properties for the stacked DRAM structure 1800. In some embodiments, the solder bumps 1846 have a diameter between about 10 μm and about 150 μm , such as a diameter between about 50 μm and about 100 μm . The solder bumps 1846 may further be formed by any suitable wafer bumping processes, including but not limited to electrochemical deposition (ECD) and electroplating.

[0132] In another exemplary embodiment depicted in FIG. 18B, a stacked DRAM structure 1801 is formed by stacking four packages 1602 and directly bonding one or more interconnections 1444 of each package 1602 with the interconnections 1444 of one or more adjacent packages 1602. As depicted, the packages 1602 may be bonded by hybrid bonding, wherein major surfaces 1005 and 1007 of adjacent packages are planarized and in full contact with each other. Thus, one or more interconnections 1444 of each package 1602 are formed through the entire thickness of each package 1602 and are directly in contact with one or more interconnections 1444 of at least another adjacent package 1602.

[0133] The stacked DRAM structures 1800 and 1801 provide multiple advantages over conventional DRAM structures. Such benefits include thin form factor and high die-to-package volume ratio, which enable greater I/O scaling to meet the ever-increasing bandwidth and power efficiency demands of artificial intelligence (AI) and high performance computing (HPC). The utilization of a structured silicon frame provides optimal material stiffness and thermal conductivity for improved electrical performance, thermal management, and reliability of 3-dimensional integrated circuit (3D IC) architecture. Furthermore, the fabrication methods for through-assembly vias and via-in-via structures described herein provide high performance and flexibility for 3D integration with relatively low manufacturing costs as compared to conventional TSV technologies.

[0134] The embodiments described herein advantageously provide improved methods of substrate structuring and die assembling for fabricating advanced integrated circuit packages. By utilizing the methods described above, high aspect ratio features may be formed on glass and/or silicon substrates, thus enabling the economical formation of thinner and narrower semiconductor device packages. The thin and small-form-factor packages fabricated by utilizing the methods described above provide the benefits of not only high I/O density and improved bandwidth and power, but also greater thermo-mechanical reliability with improved stress distribution. Further merits of the methods described above include economical manufacturing with dual-sided metallization capability and high production yield by eliminating flip-chip attachment and over-molding steps, which are prone to feature damage in high-volume manufacturing of conventional and advanced packages.

[0135] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A package assembly, comprising:
 - a frame having a first surface opposite a second surface, the frame further comprising:
 - a frame material that comprises a first material that comprises silicon;
 - at least one cavity with a semiconductor die disposed therein;
 - a via comprising a via surface that defines an opening extending through the frame from the first surface to the second surface; and
 - a coupling layer formed on the frame, the coupling layer comprising a silane coupling agent, and contacting at least the first surface and the second surface;
 - an insulating layer disposed over the coupling layer on the first surface and the second surface of the frame, the insulating layer contacting at least a portion of each side of the semiconductor die; and
 - an electrical interconnection disposed within the via, wherein the insulating layer and the coupling layer are disposed between the via surface and the electrical interconnection.
2. The package assembly of claim 1, wherein the first material comprises silicon carbide or silicon nitride.
3. The package assembly of claim 1, wherein the at least one cavity extends from the first surface to the second surface.
4. The package assembly of claim 1, wherein the insulating layer extends from the first surface to the second surface through the via and the at least one cavity.
5. The package assembly of claim 1, wherein the insulating layer comprises an epoxy resin material.
6. The package assembly of claim 5, wherein the epoxy resin material further comprises ceramic particles ranging in size between about 40 nm and about 1.5 μm .

7. The package assembly of claim 6, wherein the ceramic particles comprise one or more of aluminum nitride (AlN), aluminum oxide (Al₂O₃), silicon carbide (SiC), silicon nitride (Si₃N₄), Sr₂Ce₂Ti₅O₁₆ ceramics, zirconium silicate (ZrSiO₄), wollastonite (CaSiO₃), beryllium oxide (BeO), cerium dioxide (CeO₂), boron nitride (BN), calcium copper titanium oxide (CaCu₃Ti₄O₁₂), magnesium oxide (MgO), titanium dioxide (TiO₂), and zinc oxide (ZnO).
8. The package assembly of claim 1, wherein the coupling layer further contacts one or more sidewalls of the at least one cavity and the via surface.
9. The package assembly of claim 1, wherein the silane coupling agent comprises include a vinyl functional group, an epoxy functional group, a styryl functional group, an acryloyl functional group, a methacryl functional group, a methacryloyl functional group, an amino functional group, a phenyl functional group, a ureido functional group, an isocyanate functional group, an isocyanurate functional group, or a mercapto functional group.
10. A package assembly, comprising:
an embedded die assembly, comprising:
a frame that comprises a first material that comprises silicon;
a coupling layer disposed over the frame, the coupling layer comprising a silane coupling agent;
one or more semiconductor dies disposed within the frame, the one or more semiconductor dies having an integrated circuit formed thereon; and
an insulating layer formed on the coupling layer, the insulating layer comprising an epoxy resin material having ceramic particles disposed therein; and
one or more metal interconnections disposed within a portion of the embedded die assembly.
11. The package assembly of claim 10, wherein the frame further comprises:

one or more cavities extending from a first surface of the frame to a second surface of the frame, the one or more cavities having the one or more semiconductor dies embedded therein; and

one or more vias formed therein, each of the one or more vias comprising a via surface that defines an opening extending through the frame from the first surface to the second surface, wherein the one or more metal interconnections are disposed through the one or more vias.

12. The package assembly of claim 11, wherein the coupling layer contacts at least the first surface and the second surface.

13. The package assembly of claim 12, wherein the coupling layer further contacts one or more sidewalls of the one or more cavities and the via surface.

14. The package assembly of claim 11, wherein the insulating layer extends from the first surface to the second surface through the one or more vias and the one or more cavities.

15. The package assembly of claim 10, wherein the ceramic particles comprise one or more of aluminum nitride (AlN), aluminum oxide (Al₂O₃), silicon carbide (SiC), silicon nitride (Si₃N₄), Sr₂Ce₂Ti₅O₁₆ ceramics, zirconium silicate (ZrSiO₄), wollastonite (CaSiO₃), beryllium oxide (BeO), cerium dioxide (CeO₂), boron nitride (BN), calcium copper titanium oxide (CaCu₃Ti₄O₁₂), magnesium oxide (MgO), titanium dioxide (TiO₂), and zinc oxide (ZnO).

16. The package assembly of claim 10, wherein the silane coupling agent comprises include a vinyl functional group, an epoxy functional group, a styryl functional group, an acryloyl functional group, a methacryl functional group, a methacryloyl functional group, an amino functional group, a phenyl functional group, a ureido functional group, an isocyanate functional group, an isocyanurate functional group, or a mercapto functional group.

17. A package assembly, comprising:

an embedded die assembly, comprising:

- a frame that comprises a first material that comprises silicon;
- a coupling layer formed over the frame and comprising a silane coupling agent;
- one or more semiconductor dies disposed within the frame;
- a first insulating layer formed on the frame, the first insulating layer comprising an epoxy resin material comprising ceramic particles;
- and
- one or more electrical interconnections disposed through the frame or the first insulating layer; and

a redistribution layer formed on the embedded die assembly, the redistribution layer comprising:

- a second insulating layer formed on the first insulating layer; and
- one or more electrical redistribution connections disposed through the second insulating layer.

18. The package assembly of claim 17, wherein the silane coupling agent comprises include a vinyl functional group, an epoxy functional group, a styryl functional group, an acryloyl functional group, a methacryl functional group, a methacryloyl functional group, an amino functional group, a phenyl functional group, a ureido functional group, an isocyanate functional group, an isocyanurate functional group, or a mercapto functional group.