1. A memory system comprising:

a first chip including a first plane and a first input/output circuit; and

a controller which is capable of issuing a command for controlling the first chip,

wherein the first plane includes:

a first memory cell array having a plurality of first memory cell transistors; and

a first latch circuit which is capable of storing first read data read from the first memory cell array,

the first input/output circuit includes a first FIFO circuit which is capable of fetching the first read data from the first latch circuit, and

the controller is capable of transmitting a read command for ordering execution of a read operation to the first plane, and thereafter transmitting to the first chip a first command for ordering fetching of the first read data from the first latch circuit to the first FIFO circuit during a period in which the read operation is executed on the first plane, the read command including address information indicating the first plane, the first command including the address information.

2. The memory system according to claim 1, wherein the first read data is fetched from the first latch circuit to the first FIFO circuit during the period in which the read operation is executed on the first plane.

3. The memory system according to claim 1, further comprising a second chip including a second plane and a second input/output circuit,

wherein the second plane includes:

a second memory cell array having a plurality of second memory cell transistors; and

a second latch circuit which is capable of storing second read data read from the second memory cell array,

the second input/output circuit includes a second FIFO circuit which is capable of fetching the second read data from the second latch circuit,

the controller is capable of issuing a command for controlling the second chip, and

the controller is capable of transmitting to the second chip a second command for ordering fetching of the second read data from the second latch circuit to the second FIFO circuit during a period in which a read operation is executed on the second plane after transmission of the first command to the first chip.

4. The memory system according to claim 3, wherein the second read data is fetched from the second latch circuit to the second FIFO circuit during a period in which the read operation is executed on the second plane.

5. The memory system according to claim 3, wherein the first

chip further includes a third plane,

the third plane includes:

a third memory cell array having a plurality of third memory transistors; and

a third latch circuit which is capable of storing third read data read from the third memory cell array,

the first FIFO circuit is capable of fetching the third read data from the third latch circuit, and

the controller transmits to the first chip a third command for ordering outputting of the first read data from the first FIFO circuit to the controller after transmission of the second command to the second chip, and transmits to the first chip a fourth command for ordering fetching of the third read data from the third latch circuit to the first FIFO circuit after outputting of the first read data from the first FIFO circuit to the controller based on the third command.

6. The memory system according to claim 1, wherein the first chip further includes a second plane,

the second plane includes:

a second memory cell array having a plurality of second memory cell transistors; and

a second latch circuit which is capable of storing second read data read from the second memory cell array,

the first input/output circuit further includes a second FIFO circuit which is capable of fetching the second read

data from the second latch circuit, and

the controller is capable of transmitting to the first chip a second command for ordering fetching of the second read data from the second latch circuit to the second FIFO circuit during a period in which a read operation is executed on the second plane.

7. The memory system according to claim 6, wherein the second read data is fetched from the second latch circuit to the second FIFO circuit during a period in which the read operation is executed on the second plane.

8. The memory system according to claim 6, wherein the first chip further includes a third plane,

the third plane includes:

a third memory cell array having a plurality of third memory transistors; and

a third latch circuit which is capable of storing third read data read from the third memory cell array,

the first FIFO circuit is capable of fetching the third read data from the third latch circuit, and

the controller transmits to the first chip a third command for ordering outputting of the first read data from the first FIFO circuit to the controller after transmission of the second command to the first chip, and transmits to the first chip a fourth command for ordering fetching of the third read data from the third latch circuit to the first

FIFO circuit after outputting of the first read data from the first FIFO circuit to the controller based on the third command.

9. The memory system according to claim 1, wherein the first chip further includes a second plane,

the second plane includes:

a second memory cell array having a plurality of second memory cell transistors; and

a second latch circuit which is capable of storing second read data read from the second memory cell array,

the first FIFO circuit is capable of fetching the second read data from the second latch circuit, and

the controller transmits to the first chip a second command for ordering outputting of the first read data from the first FIFO circuit to the controller after transmission of the first command to the first chip, and the second read data is fetched from the second latch circuit to the first FIFO circuit during a period in which the first read data is output from the first FIFO circuit to the controller based on the second command.

10. The memory system according to claim 9, further comprising a switch configured to switch between coupling of the first FIFO circuit to the first latch circuit and coupling of the first FIFO circuit to the second latch circuit,

wherein after transferring of the first read data from the first latch circuit to the first FIFO circuit, the switch is switched from the coupling of the first FIFO circuit to the first latch circuit to the coupling of the first FIFO circuit to the second latch circuit.

11. The memory system according to claim 9, wherein the controller is capable of transmitting the first command to the first chip during a period in which the read operation is executed on the first plane and the second plane.

12. A memory system comprising:

a chip including a first plane, a second plane, and an input/output circuit; and

a controller which is capable of issuing a command for controlling the chip,

wherein the first plane includes:

a first memory cell array having a plurality of first memory cell transistors; and

a first latch circuit which is capable of storing first read data read from the first memory cell array,

the second plane includes:

a second memory cell array having a plurality of second memory cell transistors; and

a second latch circuit which is capable of storing second read data read from the second memory cell array,

the input/output circuit includes a FIFO circuit which

is capable of fetching the first read data from the first latch circuit and fetching the second read data from the second latch circuit,

the controller transmits to the chip a first command for ordering fetching of the second read data from the second latch circuit to the FIFO circuit, and

the controller issues, with respect to the first plane, a second command for executing a read of the first read data from the first memory cell array to the first latch circuit, after transmission of the first command to the chip and before initiation of outputting of the second read data from the FIFO circuit to the controller.