BODY-TIED SOI TRANSISTOR AND METHOD FOR FABRICATION THEREOF

BACKGROUND

FIELD OF THE INVENTION

The present disclosure relates generally to semiconductor fabrication, and more particularly to ion implantation processes during semiconductor fabrication.

Description of the Related Art

Semiconductor-on-insulator (SOI) structures have advantages over conventional bulk substrates such as elimination of latch-up, reduced short-channel effects, improved radiation hardness, and dynamic coupling, among others. Because of these advantages, semiconductor device manufacturers commonly form metal-oxide semiconductor field effect transistors (MOSFETs) on SOI structures.

In a typical MOSFET, a source and a drain are formed in an active semiconductor region by implanting N-type or P-type impurities in the layer of semiconductor material. Between the source and the drain is a channel (or body) region, above which is a gate electrode. Unfortunately, MOSFETs formed on SOI structures often experienced a floating body effect (FBE), which lead to the development of tied-body construction techniques, particularly in the manufacture of partially-depleted SOI devices such as the t-type or "hammer head" gate electrode seen in FIG. 1.

FIG. 1 illustrates a top view of a typical t-type gate transistor 100 according to the prior art. This t-type gate transistor is also known as a "hammerhead" transistor, because the shape of the block of the polysilicon portion 10 between the gate 9 and the contact 3 in region 4 resembles a hammerhead. Transistor 100 is formed in an active area having a first region 2, having a first width, and a second region 4, having a second width. Contacts 3 are located in the region 2 and contact 5 is formed in region 4. Another view of t-type gate transistor 100 is shown in FIG. 2.

FIG. 2 illustrates a cross-sectional view of t-type transistor 100 Line A of FIG. 1, while FIG. 3 illustrates a more detailed plan view of a portion of transistor 100. Line A is a cross-section just inside the gate 9 sidewall. This cross-section results in the source/drain (S/D) extensions 8 and halo implants 6 underlying the edge of the gate 9 being shown. From FIG. 2, it is seen that transistor 100 utilizes partially depleted SOI manufacturing technology. Components in FIG. 2 not illustrated in FIG. 1 include isolation structures 18, insulator layer 11, substrate 12, dielectric layer 17, source/drain (S/D) extension 8 underlying the gate 9, and halo implant 6, underlying the gate 9.

While tied-body transistors such as t-type transistor 100 avoid FBE problems by tying the transistor body to a contact CMOS scaling, has resulted in increased resistance due to attendant reductions in the cross-sectional dimensions of certain conductive structures, as well as other factors. In t-type transistor 100, there are several components of body resistance: a) contact 5 resistance, b) resistance along the width of the

transistor 100 under the gate structure 9, and c) pinch off resistance under the hammer head 10 along the boundary of the body tie implant from transistor S/D implant.

Of the three resistance components named above, the contact resistance is generally the smallest portion of the total resistance. The resistance along the width of the gate structure 9 is decreased somewhat by the halo implant 6, also known as pocket implants, which normally receives a dopant dose level about one order of magnitude greater than the well implant dose level. Well implant doses are trending downward in current manufacturing technology, which has led to an increase in resistance under the polysilicon hammer head 10 such that this resistance component has begun to dominate the body resistance.

In addition, resistance problems can be exacerbated by depletion phenomena, such as when source/drain extension depletion areas create a "pinch off" under the hammerhead 10, as shown in FIG. 3. FIG. 3 is an enlargement of a portion of the t-type transistor 100 of FIG. 1 near the hammer head 10. From FIG. 3, the depletion areas 13 near the hammer head 10 of S/D extensions have created a pinch off region 14 in the channel under the hammerhead 10, which results in increased resistance. This phenomenon is illustrated from another perspective in FIG. 4.

FIG. 4 illustrates a cross-sectional view of a portion 100 of a t-type transistor along the point indicated by Line B in FIGs 1. The pinch off region 14 as created by the overlapping depletion areas 13 is plainly seen. The gate width 7 is indicated by the dashed lines appearing in the hammerhead 10 cross section. Note that the two depletion areas do not need to overlap, as illustrated, to result in an increased resistance due to pinch off.

Therefore, a method which overcomes these problems and limitations would be useful.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Other advantages, features and characteristics of the present disclosure, as well as methods, operation and functions of related elements of structure, and the combinations of parts and economies of manufacture, will become apparent upon consideration of the following description and claims with reference to the accompanying drawings, all of which form a part of the specification, wherein like reference numerals designate corresponding parts in the various figures, and wherein:

FIG. 1 is a top view of a t-type gate transistor according to the prior art;

FIG. 2 is a prior art, cross-sectional view of t-type transistor along the area indicated by Line A in FIG. 1;

FIG. 3 is an enlargement of the top view of a portion of the prior art t-type transistor of FIG. 1;

FIG. 4 illustrates a cross-sectional view of a prior art, t-type transistor along the point indicated by Line B in FIG. 1;

FIG. 5 illustrates a top view of a portion of a t-type transistor showing the source/drain extension implants created in a fabrication process according to one embodiment of the present disclosure;

FIG. 6 illustrates a top view of the creation of halo regions in a transistor device according to at least one embodiment of the present disclosure;

FIG. 7 illustrates a cross-sectional view of a portion of a t-type transistor device fabricated according to at least one embodiment of the present disclosure; and

FIG. 8 illustrates a cross-sectional view of a portion of a t-type transistor device fabricated according to at least one embodiment of the present disclosure.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

The present disclosure provides a method for ion implantation for producing transistors such as a t-type transistor with reduced body resistance. The method comprises the steps of placing a semiconductor wafer comprising a gate edge in an ion implantation device. The semiconductor wafer is then oriented to a first position relative to a beam path of the ion implantation device in order to obtain a substantially non-orthogonal twist orientation between the beam path and the gate edge. Following this orientation to the first position, at least one ion species, for example an n-type or p-type dopant, is implanted into a first implantation region of the wafer. The wafer is then rotated to a second substantially non-orthogonal twist orientation, where another ion implantation is conducted. This process continues in the same manner, such that further substantially non-orthogonal twists and ion implantations are conducted, until the desired number of implantation areas is created.

The method overcomes the limitations of previous implantation methods by preventing an increase in resistance caused by depletion regions associated with S/D extensions overlapping in the region between the contact and gate channel in body-tied SOI transistors. The method thus reduces the total body resistance in a transistor, which increases the overall performance characteristics of the device. In addition, the present method is appropriate for integration into existing manufacturing process lines for advanced sub-micron integrated circuit semiconductor devices without the requirement for additional capital expenditures.

The present disclosure is best understood with a reference to the specific embodiments illustrated in FIGs 5 through 8. It should be noted, however, that the examples described are not intended to impose a limitation on the types of devices or process flows to which the teachings of the present disclosure may be applied. Various devices and fabrication processes utilizing ion implantation of dopants are known in the art, and many would benefit from a cost-effective process in which the suppression or reduction of resistance in

the path between the contact (such as contact in FIG. 5) and the gate channel created by the overlap of depletion regions associated with S/D diffusion areas as disclosed herein.

FIG. 5 illustrates a top view of a portion 200 of a t-type transistor on a semiconductor wafer having a gate portion 29 and a hammerhead portion 20, and source/drain portions 22 and 24. Also shown in FIG. 5 is a mask layer 21 overlying the active region 24 that is analogous to region 4 of FIG. 1. The S/D extension 28 implantation is generally accomplished according to techniques known in the art, with doses ranging from 10^{12} cm^{-2} to 10^{16} cm^{-2}. A typical S/D extension dose is on the order of a 10^{14} cm^{-2} to 10^{15} cm^{-2} range. As seen in FIG. 5, the source/drain extensions 28 extend to the edge of the hammerhead 20. Following the S/D extension 28 implantation indicated in FIG. 5, the halo implantation occurs, as shown in FIG. 6, with the results further illustrated by FIGs 7 and 8.

FIG. 6 illustrates a top view of the creation of the halo regions 26 in portion 200. In an embodiment, the semiconductor wafer is oriented to a first position relative to an ion beam path, as indicated by arrow number 31. The purpose of this orientation is to obtain a substantially non-orthogonal twist orientation between the beam path 31 and the gate structure 29 edge. The term twist or twist orientation as used herein may be thought of as analogous to the horizontal yaw axis of an aircraft, that is demonstrated by suspending a model aircraft in a level condition by a wire located at the center of gravity. Left or right movement of the nose of the aircraft occurs along the horizontal yaw axis.

Following twist orientation to the first position, an n-type or p-type dopant is implanted into a first implantation region of transistor portion 200 of the wafer. This implantation results in the creation of an initial portion of a halo or pocket implant region 26 located in the active region under hammerhead 20 of the transistor device portion 200 beyond that of the S/D extension. Additional rotations of portion 200 to beam paths indicated by the arrows numbered 32, 33, and 34 in FIG. 6, are then carried out, with respective halo implantations occurring at each of the non-orthogonal twist orientations. In this manner, an overlap between regions of halo regions 26 under the hammerhead 20 can be obtained. For example, the second implantation region may overlap the first implantation region; the third may overlap the fourth, and so on. Photoresist block 21 can be removed following completion of pocket implantation, extension implantation, and deep source implantation, or when no longer required.

In an embodiment, the ion species utilized during halo region 26 implantation is a n-type dopant such as elements located in group 15 (VA) of the periodic table, e.g., phosphorus (P). In another embodiment, the ion species implanted is a p-type dopant, e.g., elements found in group 13 (IIIA) of the periodic table, such as boron (B). These pocket implantations occur at medium beam currents and energies. For example, for boron (B), the beam energy ranges from 7 keV to 15 keV, while the beam energy ranges for arsenic (As) are from 40 keV to 90 keV. The halo or pocket implantation dose can range from 10^{13} cm^{-2} to10^{15} cm^{-2}, with 10^{13} cm^{-2} being a typical delivered dose.

The substantially non-orthogonal twist orientation can be 45 degrees relative to the gate 29 edge, as seen in FIG. 6. In one embodiment, the substantially non-orthogonal twist orientation can range between 30

degrees and 60 degrees. In a further embodiment, the substantially non-orthogonal twist orientation can be between 15 degrees and 75 degrees. The substantially non-orthogonal twist orientation is chosen based upon the desired result, which involves consideration of the geometry of the features for which implants such as halo implantation region 26 are needed.

FIG. 7 illustrates a cross-sectional view of portion 200 of a t-type transistor device according to an embodiment of the present disclosure. The cross-sectional view of FIG. 7 is similar to that which would be obtained by dissection across the area indicated by Line A in FIG. 1. The example presented in FIG. 7 is that of an SOI transistor employing partially depleted SOI manufacturing technology. Components in FIG. 7, which were not illustrated in FIG. 6, include isolation structures 38, insulator layer 31, substrate 32, and active regions 22 and 24. The beam paths are illustrated for reference purposes, even though the masking layer 21 has been removed.

As seen in FIG. 7, the halo region 26 extends under a portion of the hammerhead 20 of gate structure 29. This has the effect of constraining the depletion 53 of S/D depletion region and suppressing pinch-off, as seen in FIG. 8.

FIG. 8 illustrates a cross-sectional view of a portion of a t-type transistor device fabricated according to an embodiment of the present disclosure. The cross-sectional view of FIG. 8 is similar to that which would be obtained by dissection across the area indicated by Line B in FIG. 1. The S/D depletion region 53 is pulled back such that a depletion pinch off condition in the channel 40 under the hammerhead 20 is not manifested. This will result in decreased total body resistance because the resistance increase manifested by the manufacturing methods of the prior art which created a pinch off region (14, FIG. 4) are not manifested when practicing the manufacturing techniques taught herein.

The method and apparatus described herein provides for a flexible implementation. Although the invention has been described using certain specific examples, it will be apparent to those skilled in the art that the invention is not limited to these few examples. For example, the disclosure could be used to create other features not specifically illustrated. In addition, the invention can be employed with other device technologies to realize reduced resistance characteristics in implantation processes during device manufacture. Additionally, various types of ion implantation devices are currently available which could be suitable for use in employing the method as taught herein. Note also, that although an embodiment of the present invention has been shown and described in detail herein, along with certain variants thereof, many other varied embodiments that incorporate the teachings of the invention may be easily constructed by those skilled in the art. For example, specific novel embodiments of the present disclosure are identified by the items listed below:

Item 1. A method comprising placing a semiconductor wafer comprising a gate edge in an ion implantation device; orienting the semiconductor wafer to a first position relative to a beam path of the ion implantation device to obtain a substantially non-orthogonal twist orientation between the beam path and the

gate edge; and implanting at least one ion species into a first implantation region of the semiconductor wafer while the semiconductor wafer is in the first position.

Item 2. The method of item 1, further comprising rotating the semiconductor wafer to a second substantially non-orthogonal twist orientation; and implanting at least one ion species into a second implantation region of the semiconductor wafer while the semiconductor wafer is in the second position.

Item 3. The method of item 2, wherein the first implantation region and the second implantation region are located under a hammer head portion of a transistor device, and wherein the second implantation region overlaps the first implantation region.

Item 4. The method of items 1, 10 and 17 wherein the substantially non-orthogonal twist orientation is 45 degrees.

Item 5. The method of items 1, 10 and 17 wherein the substantially non-orthogonal twist orientation is between 30 degrees and 60 degrees.

Item 6. The method of items 1, 10 and 17 wherein the substantially non-orthogonal twist orientation is between 15 degrees and 75 degrees.

Item 7. The method of item 1, wherein the ion species is an n-type dopant.

Item 8. The method of item 1, wherein the ion species is a p-type dopant.

Item 9. A method comprising forming a transistor device having a gate portion and a hammer-head portion, the gate portion comprising a first gate edge and a second gate edge, wherein a distance between the first gate edge and second gate edge is the gate's width; and implanting a dopant, after forming the transistor device, underlying the hammerhead portion to form a continuously doped region extending from a first point under the hammerhead portion that is closest to the first gate edge to a second location under the hammerhead portion that is closest to the second edge.

Item 10. The method of item 9, wherein the step of implanting further comprises rotating the transistor device to a first substantially non-orthogonal twist orientation; implanting at least one ion species into a first implantation region of the transistor device; rotating the transistor device to a second substantially non-orthogonal twist orientation; and implanting at least one ion species into a second implantation region of the transistor device.

Item 11. The method of item 10, wherein the substantially non-orthogonal twist orientation is 45 degrees.

Item 12. The method of item 10, wherein the substantially non-orthogonal twist orientation is between 30 degrees and 60 degrees.

Item 13. The method of item 10, wherein the substantially non-orthogonal twist orientation is between 15 degrees and 75 degrees.

Item 14. The method of item 9, wherein the dopant is an n-type dopant.

Item 15. The method of item 9, wherein the dopant is a p-type dopant.

Item 16. A semiconductor device comprising a transistor device having a gate portion and a hammerhead portion, the gate portion comprising a first gate edge and a second gate edge, wherein a distance between the first gate edge and the second gate edge is the gate's width; a continuously-doped region extending from a first point under the hammer-head portion that is closest to the first gate edge to a second location under the hammer-head portion that is closest to the second edge; a dopant underlying the hammer-head portion forming a continuously-doped region extending from a first point under the hammer-head portion that is closest to the first gate edge to a second location under the hammer-head portion that is closest to the second gate edge.

Item 17. The device of item 16, wherein the dopant underlying the hammer-head portion comprises at least one ion species implanted while the transistor device was oriented to at least one substantially non-orthogonal twist orientation.

Item 18. The device of item 17, wherein the substantially non-orthogonal twist orientation is 45 degrees.

Item 19. The device of item 17, wherein the substantially non-orthogonal twist orientation is between 30 degrees and 60 degrees.

Item 20. The device of item 17, wherein the substantially non-orthogonal twist orientation is between 15 degrees and 75 degrees.

Item 21. The device of item 16, wherein the dopant is an n-type dopant.

Item 22. The device of item 16, wherein the dopant is a p-type dopant.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. Accordingly, the present invention is

not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A method comprising:

placing a semiconductor wafer comprising a gate edge in an ion implantation device;

orienting the semiconductor wafer to a first position relative to a beam path of the ion implantation device to obtain a substantially non-orthogonal twist orientation between the beam path and the gate edge; and

implanting at least one ion species into a first implantation region of the semiconductor wafer while the semiconductor wafer is in the first position.

2. The method of claim 1, further comprising:

rotating the semiconductor wafer to a second substantially non-orthogonal twist orientation; and

implanting at least one ion species into a second implantation region of the semiconductor wafer while the semiconductor wafer is in the second position.

3. The method of claim 2, wherein the first implantation region and the second implantation region are located under a hammer head portion of a transistor device, and wherein the second implantation region overlaps the first implantation region.

4. The method of claims 1, 8 and 10 wherein the substantially non-orthogonal twist orientation is 45 degrees.

5. The method of claims 1, 8 and 10 wherein the substantially non-orthogonal twist orientation is between 30 degrees and 60 degrees.

6. The method of claims 1, 8 and 10 wherein the substantially non-orthogonal twist orientation is between 15 degrees and 75 degrees.

7. A method comprising:

forming a transistor device having a gate portion and a hammer-head portion, the gate portion comprising a first gate edge and a second gate edge, wherein a distance between the first gate edge and second gate edge is the gate's width; and

implanting a dopant, after forming the transistor device, underlying the hammerhead portion to form a continuously doped region extending from a first point under the hammerhead portion that is closest to the first gate edge to a second location under the hammerhead portion that is closest to the second edge.

8. The method of claim 7, wherein the step of implanting further comprises:

rotating the transistor device to a first substantially non-orthogonal twist orientation;

implanting at least one ion species into a first implantation region of the transistor device;

rotating the transistor device to a second substantially non-orthogonal twist orientation; and

implanting at least one ion species into a second implantation region of the transistor device.

9. A semiconductor device comprising:

a transistor device having a gate portion and a hammerhead portion, the gate portion comprising a first gate edge and a second gate edge, wherein a distance between the first gate edge and the second gate edge is the gate's width;

a continuously-doped region extending from a first point under the hammer-head portion that is closest to the first gate edge to a second location under the hammer-head portion that is closest to the second edge;

a dopant underlying the hammer-head portion forming a continuously-doped region extending from a first point under the hammer-head portion that is closest to the first gate edge to a second location under the hammer-head portion that is closest to the second gate edge.

10. The device of claim 9, wherein the dopant underlying the hammer-head portion comprises at least one ion species implanted while the transistor device was oriented to at least one substantially non-orthogonal twist orientation.