

LOW-VOLTAGE SENSE AMPLIFIER AND METHOD

TECHNICAL FIELD

The invention relates to memory devices, and more particularly, to sense amplifiers used to sense differential voltages produced by memory cells in memory devices, such as dynamic random access memory ("DRAM") devices.

BACKGROUND OF THE INVENTION

Memory devices, such as static random access memory ("SRAM") devices and dynamic random access memory ("DRAM") devices are in common use in a wide variety of electronic systems, such as personal computers. Memory devices include one or more arrays of memory cells, which, in DRAM devices, are small capacitors that are arranged in rows and columns. A portion of a conventional DRAM memory array 10 is shown in Figure 1. The array 10 includes a pair of complementary digit lines DL, DL* for each column of the array 10, only one pair of which is shown in Figure 1. A large number of memory cells 12 are coupled to the digit lines DL, DL*.

Each of the memory cells 12 includes an access transistor 16 and a memory cell capacitor 18 coupled between the transistor 16 and a cell plate 20, which is generally biased at one-half the supply voltage, *i.e.*, $V_{CC}/2$. The capacitor 18 generally stores a voltage equal to either the supply voltage V_{CC} or ground. A gate of each access transistor 16 is coupled to a respective word line WL_0 , WL_1 , although only two of these word lines are shown in Figure 1. For a "folded digit line" architecture, the even-numbered word lines, *e.g.*, WL_0 , are coupled to the digit lines DL, and the odd-numbered word lines, *e.g.*, WL_1 , are coupled to the complementary digit lines DL*. Thus, one word line WL is provided for each row of memory cells 12 in the array 10.

Each pair of digit lines DL, DL* is coupled to a respective sense amplifier 30 that performs two functions; first, "equilibrating" the digit lines and, second, sensing a differential voltage developed between the digit lines DL, DL* and then driving the digit lines to corresponding logic levels. Equilibrating the digit lines DL, DL*, which causes them to be at the same voltage, is accomplished using an equilibration circuit 34. The equilibration circuit 34 includes an equilibration transistor

36 coupled between the digit lines DL, DL*, and a pair of equilibration bias transistors 40, 42 coupled between one-half the supply voltage, *i.e.*, $V_{CC}/2$, and respective digit lines DL, DL*.

In operation, in response to an active high equilibration EQ signal, the equilibration transistor 36 turns ON to couple the digit lines DL, DL* to each other, and the equilibration bias transistors 40, 42 turn ON to couple the digit lines DL, DL* to $V_{CC}/2$. As a result, after an equilibration period, the voltage on both of the digit lines DL, DL* is $V_{CC}/2$, and the differential voltage between the digit lines is therefore zero.

As mentioned above, the sense amplifier 30 also performs the function of sensing a differential voltage developed between the digit lines DL, DL* and then driving the digit lines to corresponding logic levels. This second function is accomplished by an NSENSE amplifier 50 and a PSENSE amplifier 52. The NSENSE amplifier 50 includes a pair of cross-coupled NMOS transistors 56, 58, and the PSENSE amplifier 52 similarly includes a pair of cross-coupled PMOS transistors 60, 62.

In operation, the digit lines DL, DL* are initially equilibrated by driving the EQ signal active high for the equilibration period. After the differential voltage between the digit lines DL, DL* has reached substantially zero volts, the EQ signal transitions inactive low to turn OFF the transistors 36, 40, 42. One of the word lines is then driven active high to turn ON the access transistor 16 to which it is coupled. The ON access transistor 16 then couples a memory cell capacitor 18 to the digit line DL or DL* to which the access transistor 16 is coupled. This voltage from the capacitor 18 causes the voltage on the digit line DL or DL* to either increase slightly (if the capacitor 18 was at V_{CC}) or decrease slightly (if the capacitor 18 was at ground).

A SENSE ENABLE line is then driven to a relatively low voltage, such as ground or a slight negative voltage, and an ACT line is driven to a relatively high voltage, such as V_{CC} or a voltage elevated slightly above V_{CC} . Assuming, for example, the voltage on the digit line DL has increased, the NMOS transistor 58 will turn ON to an extent that is greater than the amount the NMOS transistor 56 turns ON because the gate-to-source voltage of the transistor 58 will be greater. The complementary digit line DL* is therefore pulled toward the low voltage on the SENSE ENABLE line to a

greater extent than the DL is pulled toward zero voltage. In a manner similar to the operation of the NSENSE amplifier 50, when the ACT line is driven high, the PMOS transistor 60 in the PSENSE amplifier 52 turns ON to an extent that is greater than the extent that the PMOS transistor 62 is turned ON because the gate-to-source voltage of the transistor 60 is larger. Therefore, the transistor 60 more strongly drives the digit line DL to V_{CC} . Thereafter, the voltage on the digit line DL further increases and the voltage on the complementary digit line DL* further decreases, thereby causing the transistor 60 to drive the digit line DL more strongly, and the transistor 62 to drive the complementary digit line less strongly, to the relatively high ACT voltage. At the same time, the increased voltage on the digit line DL and the decreased voltage on the complementary digit line DL* causes the transistor 58 to drive the complementary digit line DL* more strongly, and the transistor 56 to drive the digit line DL less strongly, to the relatively low SENSE ENABLE voltage. At the end of a sensing period, the NSENSE amplifier 50 has driven the complementary digit line DL* to the relatively low SENSE ENABLE voltage, and the PSENSE amplifier 52 has driven in the digit line DL to the relatively high ACT voltage. A COLUMN SELECT signal then transitions high to turn ON input/output ("I/O") transistors 70, 72, thereby coupling the digit lines DL, DL* to respective complementary I/O lines 76, 78 in order to read a data bit from the array 10.

The sense amplifier 30 shown in Figure 1 can also be used to read data bits from a memory array (not shown) having an open digit line architecture in essentially the same manner as explained above with reference to the folded digit line architecture shown in Figure 1.

Although the sense amplifier 30 shown in Figure 1 has performed well in the past, it is less able to quickly sense a differential voltage between the digit lines DL, DL* as the magnitude of the supply voltage V_{CC} continues to decrease and transistor threshold voltages V_T continues to decrease less rapidly, which is the trend for newer memory designs. Although the sense amplifier 30 may still correctly sense the voltage differential between the digit lines DL, DL*, the time required for the sense amplifier 30 to do so can increase to unacceptable levels.

There is therefore a need for a sense amplifier that can quickly sense a voltage differential between complementary digit lines even for a supply voltage having a relatively small magnitude.

SUMMARY OF THE INVENTION

5 A sense amplifier and method in accordance with the present invention includes a first sense amplifier section driving a second sense amplifier section. During a memory read operation, the first sense amplifier section is initially coupled to the digit lines for only a short period of time so that the voltage differential is applied to the first sense amplifier section. Thereafter, the first sense amplifier section is isolated from the
10 digit lines so that the sense amplifier can respond to the differential voltage without the need to drive the relatively high capacitance digit lines. As a result, the differential voltage generated by the first sense amplifier section can increase at a relatively fast rate. While the first sense amplifier section is responding to the differential voltage, the first sense amplifier section drives the second sense amplifier section, which is coupled
15 to the digit lines. As a result, the second sense amplifier is driven by a voltage that increases at a rate that is faster than the rate that the voltage between the digit lines increases. The sense amplifier can be used with any type of memory device that uses complementary digit lines, including a wide variety of DRAM devices as well as static random access memory ("SRAM") devices and FLASH memory devices.

20 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic of a portion of a conventional memory array coupled to a conventional sense amplifier.

Figure 2 is a schematic of a sense amplifier according to one embodiment of the present invention.

25 Figure 3 is a flow chart showing the operation of the sense amplifier embodiment of Figure 2.

Figure 4 is a waveform diagram showing various signals present in the sense amplifier of Figure 2 as a function of time.

Figure 5 is a block diagram of a memory device using the sense amplifier of Figure 2 or some other embodiment of a sense amplifier accordance with the present invention.

Figure 6 is a block diagram of a computer system using the memory device of Figure 5.

DETAILED DESCRIPTION OF THE INVENTION

A sense amplifier 100 according to one embodiment of the invention is shown in Figure 2. The sense amplifier 100 includes an inner sense amplifier section 110 and an outer sense amplifier section 120. The inner sense amplifier 110 has the same typography as the sense amplifier 10 shown in Figure 1 except that it is coupled between a pair of complementary sense lines S, S* rather than between complementary digit lines DL, DL*. Thus, the inner sense amplifier section 110 includes a pair of cross-coupled PMOS sense transistors 130, 132 that couple respective sense lines S, S* to a supply voltage V_{CC} through a PMOS positive supply transistor 136. The conductive state of the transistor 136 is controlled by an active low early PSENSE* signal. Similarly, a pair of cross-coupled NMOS sense transistors 140, 142 couple the sense lines S, S* to a relatively low supply voltage, which is preferably a negative voltage V_{BB} , through an NMOS negative supply transistor 146. The conductive state of the transistor 146 is controlled by an active high early NSENSE signal.

In operation, when the early PSENSE* and early NSENSE signals are active, the first sense amplifier section 110 operates in the same manner described above for the sense amplifier 10 to sense a voltage differential between the sense lines S, S* and then drive the sense lines S, S* to corresponding logic levels.

The first sense amplifier section 110 is selectively isolated from the second sense amplifier section 120 through a pair of NMOS coupling transistors 150, 152, which are controlled by an active high connect "CON" signal. The second sense amplifier section 120, like the first sense amplifier section 110, includes a pair of PMOS sense transistors 154, 156 coupled to V_{CC} through a PMOS positive supply transistor 158. The conductive state of the transistor 158 is controlled by an active low late PSENSE* signal. In a similar manner, a pair of NMOS sense transistors 160, 162

are coupled to ground through an NMOS negative supply transistor 164. The conductive state of the transistor 164 is controlled by a signal that will be described below.

The second sense amplifier section 120 differs from the first sense amplifier section 110: (1) by being coupled between the digit lines DL, DL* rather than between the sense lines S, S*, and (2) by having the gates of its sense transistors 154, 156, 160, 162 coupled to the sense lines S, S* rather than to the digit lines DL, DL*. As a result, the sense transistors 154, 156, 160, 162 are not cross-coupled. The switching of the sense transistors 154, 156, 160, 162 is controlled by the voltage differential between the sense lines S, S* rather than by the voltage differential between the digit lines DL, DL* as is done with prior art sense amplifiers. Since the voltage between the sense lines S, S* can change much more rapidly than the voltage between the digit lines because of the lower capacitance of the sense lines S, S*, the sense transistors 154, 156, 160, 162 are switched at a much more rapid rate than in prior art sense amplifiers, such as the amplifier 10 shown in Figure 1.

The CON signal used to control the conductive state of the coupling transistors 150, 152 is generated by a NAND gate 170, which receives the early NSENSE signal and the compliment of an active high WRITE signal through an inverter 172. The CON signal will therefore be active high to couple the inner sense amplifier section 110 to the outer sense amplifier section 120 if either the early NSENSE signal is inactive or the WRITE signal is active high. The WRITE signal coupled through the inverter 172 is also applied to a NAND gate 176, which also receives an active high late NSENSE signal. The NAND gate 176 will output a low to turn ON the negative supply transistor 164 through an inverter 178 if the late NSENSE signal is active and the WRITE signal is inactive low.

The operation of the sense amplifier 100 for a read memory access will now be explained with reference to flow chart of Figure 3 and the waveform diagram of Figure 4. As shown in Figure 4, the WRITE signal is initially low and all of the other signals mentioned above are inactive. As a result, no power is applied to the sense amplifier sections 110, 120 and the CON signal is high to cause the coupling transistors 150, 152 to connect the sense amplifier sections 110, 120 to each other, which is shown

at step 180. At time t_0 , a memory cell capacitor is coupled to the digit line DL (although it could alternatively be coupled to the complementary digit line DL*), thereby causing the voltage on the digit line DL to increase slightly relative to the voltage on the complementary digit line DL* as shown at step 184. The voltage
5 differential between the digit lines DL, DL* is also coupled to the sense lines S, S* because the coupling transistors 150, 152 are still ON.

At t_1 , the early NSENSE and early PSENSE* signals transition to an active state at step 188, thereby applying power to the inner sense amplifier section 110. The active high early NSENSE signal also causes the NAND gate 170 to make the CON
10 signal inactive low, which turns OFF the coupling transistors 150, 152 to isolate the inner sense amplifier section 110 from the outer sense amplifier section 120. As shown in Figure 4, the inner sense amplifier section 110 is able to respond to the voltage differential between the sense lines S, S* much faster than the outer sense amplifier section 120 is able to respond to the voltage differential between the digit lines DL, DL*
15 because of the much lower capacitance of the sense lines S, S* (the S signal is shown by the solid line, and the S* signal is shown by the dotted line). The voltages applied to the gates of the sense transistors 154, 156, 160, 162 in the outer sense amplifier section 120 therefore transition much faster than voltages that could be applied to the gates from the digit lines DL, DL* as in conventional sense amplifiers.

20 Power is subsequently applied to the outer sense amplifier section 120 at time t_2 in step 190 by transitioning the late NSENSE and PSENSE* signals to an active state, as shown in Figure 4. The sense transistors 154, 156, 160, 162 then drive the digit lines DL, DL* to complementary logic levels corresponding to the data bit read from the memory cell capacitor in step 184 (the DL signal is shown by the solid line, and the
25 DL* signal is shown by the dotted line). The voltages on the digit lines DL, DL* transition at a relatively fast rate compared to digit lines driven by conventional sense amplifiers because the voltages on the gates of the sense transistors 154, 156, 160, 162 are already at voltages that strongly turn ON the sense transistors 154, 156, 160, 162 before the voltages on the digit lines DL, DL* have changed appreciably. In contrast, if
30 the gates of the sense transistors 154, 156, 160, 162 were coupled to the digit lines DL, DL*, the sense transistors 154, 156, 160, 162 may not have the drive strength needed to

discern the slight voltage difference or they would switch at the relatively slow rate commensurate with the speed at which the differential voltage between the digit lines DL, DL* increases. The voltages on the digit lines DL, DL* reach complementary logic levels corresponding to the read data bit at time t_3 to refresh the memory cell capacitor coupled to the digit line DL at step 194, thereby completing the read memory access.

The initial operation of the sense amplifier 100 for a write memory access is similar to the above-described operation for a read memory access since a write memory access always starts out as a read memory access and does not transition to a write memory access until the WRITE signal transitions active high when the memory device receives a column address and a column address strobe signal. The transitioning of the WRITE signal causes the write memory access to differ from the read memory access because NAND gate 170 outputs a high to turn ON the coupling transistors 150, 152 after the early NSENSE signal has transitioned active high. As a result, the inner sense amplifier section 110 continues to be connected to the outer sense amplifier section 120. Furthermore, the active high WRITE signal causes the NAND gate to output a high even when the late NSENSE signal is active to maintain the negative supply transistor 164 OFF.

The high speed operation of the first sense amplifier section 110 is further enhanced by coupling the sense transistors 140, 142 to a negative voltage V_{BB} rather than to ground. However, this negative voltage V_{BB} can easily be supplied by conventional sources, such as a charge pump (not shown), because it is only necessary to drive the sense lines S, S*. If it was also necessary to drive the digit lines DL, DL*, substantially more current at the negative voltage V_{BB} would be required.

Figure 5 is a block diagram of a conventional synchronous dynamic random access memory ("SDRAM") 200 that utilizes the sense amplifier 100 (Figure 2) or some other embodiment of the invention. Of course, the sense amplifier 100 and other embodiments of the invention can also be used in other DRAM devices and other memory devices, such as SRAM devices, FLASH memory devices, etc.

The operation of the SDRAM 200 is controlled by a command decoder 204 responsive to high-level command signals received on a control bus 206. These high level command signals, which are typically generated by a memory controller (not

shown in Figure 5), are a clock enable signal CKE*, a clock signal CLK, a chip select signal CS*, a write enable signal WE*, a row address strobe signal RAS*, a column address strobe signal CAS*, and a data mask signal DQM, in which the "*" designates the signal as active low. The command decoder 204 generates a sequence of command signals responsive to the high level command signals to carry out the function (e.g., a read or a write) designated by each of the high level command signals. These command signals, and the manner in which they accomplish their respective functions, are conventional. Therefore, in the interest of brevity, a further explanation of these command signals will be omitted.

10 The SDRAM 200 includes an address register 212 that receives row addresses and column addresses through an address bus 214. The address bus 214 is generally coupled to a memory controller (not shown in Figure 5). A row address is generally first received by the address register 212 and applied to a row address multiplexer 218. The row address multiplexer 218 couples the row address to a number of components associated with either of two memory banks 220, 222 depending upon the state of a bank address bit forming part of the row address. Associated with each of the memory banks 220, 222 is a respective row address latch 226, which stores the row address, and a row decoder 228, which decodes the row address and applies corresponding signals to one of the arrays 220 or 222. The row address multiplexer 218 also couples row addresses to the row address latches 226 for the purpose of refreshing the memory cells in the arrays 220, 222. The row addresses are generated for refresh purposes by a refresh counter 230, which is controlled by a refresh controller 232. The refresh controller 232 is, in turn, controlled by the command decoder 204.

25 After the row address has been applied to the address register 212 and stored in one of the row address latches 226, a column address is applied to the address register 212. The address register 212 couples the column address to a column address latch 240. Depending on the operating mode of the SDRAM 200, the column address is either coupled through a burst counter 242 to a column address buffer 244, or to the burst counter 242, which applies a sequence of column addresses to the column address buffer 244 starting at the column address output by the address register 212. In either case, the column address buffer 244 applies a column address to a column decoder 248.

Data to be read from one of the arrays 220, 222 is coupled to column circuitry 250, 252 (*i.e.*, sense amplifiers, I/O gating, DQM & WPB mask logic, block write col./byte mask logic) for one of the arrays 220, 222, respectively. The column circuitry 250, 252 may include for each column of memory cells in the arrays 220, 222 the equilibration circuit 34 (Figure 1) and the sense amplifier 100 or a sense amplifier according to some other embodiment of the invention. The data bits developed by the sense amplifier 100 are then coupled to a data output register 256. Data to be written to one of the arrays 220, 222 are coupled from the data bus 258 through a data input register 260. The write data are coupled to the column circuitry 250, 252 where they are transferred to one of the arrays 220, 222, respectively. A mask register 264 responds to a data mask DM signal to selectively alter the flow of data into and out of the column circuitry 250, 252, such as by selectively masking data to be read from the arrays 220, 222.

Figure 6 shows an embodiment of a computer system 300 that may use the SDRAM 200 or some other memory device that uses the sense amplifier 100 or some other embodiment of the invention. The computer system 300 includes a processor 302 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 302 includes a processor bus 304 that normally includes an address bus, a control bus, and a data bus. In addition, the computer system 300 includes one or more input devices 314, such as a keyboard or a mouse, coupled to the processor 302 to allow an operator to interface with the computer system 300. Typically, the computer system 300 also includes one or more output devices 316 coupled to the processor 302, such output devices typically being a printer or a video terminal. One or more data storage devices 318 are also typically coupled to the processor 302 to store data or retrieve data from external storage media (not shown). Examples of typical storage devices 318 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs). The processor 302 is also typically coupled to a cache memory 326, which is usually static random access memory ("SRAM") and to the SDRAM 200 through a memory controller 330. The memory controller 330 includes an address bus 214 (Figure 5) to couple row addresses and column addresses to the DRAM 200. The memory controller

330 also includes a control bus that couples command signals to a control bus 206 of the SDRAM 200. The external data bus 258 of the SDRAM 200 is coupled to the data bus of the processor 302, either directly or through the memory controller 330.

From the foregoing it will be appreciated that, although specific
5 embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A sense amplifier, comprising:
 - a first sense amplifier section comprising:
 - first and second complementary sense lines;
 - first switch coupled between the first sense line and a first power supply node, the first switch having a control terminal coupled to the second sense line;
 - a second switch coupled between the second sense line and the first power supply node, the second switch having a control terminal coupled to the first sense line;
 - a third switch coupled between the first sense line and a second power supply node, the third switch having a control terminal coupled to the second sense line;
 - a fourth switch coupled between the second sense line and the second power supply node, the fourth switch having a control terminal coupled to the first sense line;
 - a second sense amplifier section comprising:
 - a pair of complementary digit lines;
 - a first switch coupled between the first digit line and a third power supply node, the first switch having a control terminal coupled to the second sense line;
 - a second switch coupled between the second digit line and the third power supply node, the second switch having a control terminal coupled to the first sense line;
 - a third switch coupled between the first digit line and a fourth power supply node, the third switch having a control terminal coupled to the second sense line;

a fourth switch coupled between the second digit line and the fourth power supply node, the fourth switch having a control terminal coupled to the first sense line;

a sixth switch coupled between the first sense line and the first digit line the, the sixth switch having a control terminal; and

a seventh switch coupled between the second sense line and the second digit line, the seventh switch having a control terminal.

2. The sense amplifier of claim 1 wherein each of the switches comprises respective FET transistors.

3. The sense amplifier of claim 2 wherein each of the switches comprises respective MOSFET transistors.

4. The sense amplifier of claim 1 wherein the first power supply voltage and the third power supply voltage are equal to each other.

5. The sense amplifier of claim 4 wherein the first and third power supply voltage comprise a positive voltage.

6. The sense amplifier of claim 1 wherein the second power supply voltage and the fourth power supply voltage are different from each other.

7. The sense amplifier of claim 6 wherein the second power supply voltage comprises a negative voltage and the fourth power supply voltage comprises zero volts.

8. The sense amplifier of claim 1, further comprising a control circuit coupled to the control terminals of the sixth and seventh switches.

9. The sense amplifier of claim 8, further comprising an eighth switch coupled between the fourth power supply node and a power supply terminal, the eighth switch having a control terminal, and wherein the control circuit is further coupled to the control terminals of the eighth switch.

10. The sense amplifier of claim 1, further comprising
an eighth switch coupled between the first power supply node and a first power supply terminal, the eighth switch having a control terminal; and
a ninth switch coupled between the third power supply node and a second power supply terminal, the ninth switch having a control terminal.

11. An amplifier for sensing a differential voltage, comprising:
a first sense amplifier having complementary first and second output terminals and complementary first and second input terminals, the first input terminal being coupled to the second output terminal, and the second input terminal being coupled to the first output terminal;

a second sense amplifier having complementary first and second output terminals and complementary first and second input terminals, the first input terminal being coupled to the second output terminal of the first sense amplifier, and the second input terminal being coupled to the first output terminal of the first sense amplifier; and

a coupling circuit configured to couple the first output terminal of the first sense amplifier to the first output terminal of the second sense amplifier, and to couple the second output terminal of the first sense amplifier to the second output terminal of the second sense amplifier.

12. The sense amplifier of claim 11 wherein the coupling circuit comprises:

a first switch coupling the first output terminal of the first sense amplifier to the first output terminal of the second sense amplifier, the first switch having a control terminal; and

a second switch coupling the second output terminal of the first sense amplifier to the second output terminal of the second sense amplifier, the second switch having a control terminal.

13. The sense amplifier of claim 12 wherein the first and second switches comprise respective FET transistors.

14. The sense amplifier of claim 11, further comprises a first switch through which a first power supply voltage is coupled to the first sense amplifier, a second switch through which a second power supply voltage is coupled to the first sense amplifier, a third switch through which a third power supply voltage is coupled to the second sense amplifier, and a fourth switch through which a fourth power supply voltage is coupled to the second sense amplifier.

15. The sense amplifier of claim 14 wherein the first, second, third and fourth switches comprise respective FET transistors.

16. The sense amplifier of claim 14 wherein the first power supply voltage is the same as the third power supply voltage, and the second power supply voltage is different from the fourth power supply voltage.

17. The sense amplifier of claim 16 wherein the first and second power supply voltages are positive, the second power supply voltage is negative, and the fourth power supply voltage is zero volts.

18. A sense amplifier, comprising:

a first sense amplifier section comprising:

first and second complementary sense lines;

a first p-channel sense transistor having its source and drain coupled between the first sense line and a first voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second sense line and the first voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first sense line and a second voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second sense line and the second voltage, and its gate coupled to the first sense line;

a second sense amplifier section comprising:

a pair of complementary digit lines;

a first p-channel sense transistor having its source and drain coupled between the first digit line and a third voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second digit line and the third voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first digit line and a fourth voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second digit line and the fourth voltage, and its gate coupled to the first sense line;

a first coupling transistor having its source and drain coupled between the first sense line and the first digit line; and

a second coupling transistor having its source and drain coupled between the second sense line and the second digit line.

19. The sense amplifier of claim 18 wherein the first voltage and the third voltage are equal to each other.

20. The sense amplifier of claim 19 wherein the first and third voltage comprise a positive voltage.

21. The sense amplifier of claim 18 wherein the second voltage and the fourth voltage are different from each other.

22. The sense amplifier of claim 21 wherein the second voltage comprises a negative voltage and the fourth voltage comprises zero volts.

23. The sense amplifier of claim 18, further comprising a control circuit coupled to a gate of the first coupling transistor and to a gate of the second coupling transistor.

24. The sense amplifier of claim 18 wherein the coupling transistors comprise respective n-channel transistors.

25. A memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

at least one array of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a plurality of sense amplifiers provided for respective columns of memory cells in the at least one array, each of the sense amplifiers comprising:

a first sense amplifier section comprising:

first and second complementary sense lines;

a first p-channel sense transistor having its source and drain coupled between the first sense line and a first voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second sense line and the first voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first sense line and a second voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second sense line and the second voltage, and its gate coupled to the first sense line;

a second sense amplifier section comprising:

a pair of complementary digit lines;

a first p-channel sense transistor having its source and drain coupled between the first digit line and a third voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second digit line and the third voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first digit line and a fourth voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second digit line and the fourth voltage, and its gate coupled to the first sense line;

a first coupling transistor having its source and drain coupled between the first sense line and the first digit line; and

a second coupling transistor having its source and drain coupled between the second sense line and the second digit line;

a data path circuit operable to couple data signals corresponding to the data bits between the sense amplifiers and external data terminals of the memory device; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

26. The memory device of claim 25 wherein the first voltage and the third voltage are equal to each other.

27. The memory device of claim 26 wherein the first and third voltage comprise a positive voltage.

28. The memory device of claim 25 wherein the second voltage and the fourth voltage are different from each other.

29. The memory device of claim 28 wherein the second voltage comprises a negative voltage and the fourth voltage comprises zero volts.

30. The memory device of claim 25, further comprising a control circuit coupled to a gate of the first coupling transistor and to a gate of the second coupling transistor.

31. The memory device of claim 30 wherein the coupling transistors comprise respective n-channel transistors.

32. The memory device of claim 25 wherein the memory device comprises a dynamic random access memory device.

33. The memory device of claim 32 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

34. A memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

at least one array of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a plurality of sense amplifiers provided for respective columns of memory cells in the at least one array, each of the sense amplifiers comprising:

a first sense amplifier section having complementary first and second output terminals and complementary first and second input terminals, the first input terminal being coupled to the second output terminal, and the second input terminal being coupled to the first output terminal;

a second sense amplifier section having complementary first and second output terminals and complementary first and second input terminals, the first input terminal being coupled to the second output terminal of the first sense amplifier section, and the second input terminal being coupled to the first output terminal of the first sense amplifier section; and

a coupling circuit configured to couple the first output terminal of the first sense amplifier section to the first output terminal of the second sense amplifier section, and to couple the second output terminal of the first sense amplifier section to the second output terminal of the second sense amplifier section;

a data path circuit operable to couple data signals corresponding to the data bits between the sense amplifiers and external data terminals of the memory device; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

35. The memory device of claim 34 wherein the coupling circuit comprises:

a first switch coupling the first output terminal of the first sense amplifier section to the first output terminal of the second sense amplifier section, the first switch having a control terminal; and

a second switch coupling the second output terminal of the first sense amplifier section to the second output terminal of the second sense amplifier section, the second switch having a control terminal.

36. The memory device of claim 35 wherein the first and second switches comprise respective FET transistors.

37. The memory device of claim 34, further comprises a first switch through which a first power supply voltage is coupled to the first sense amplifier section, a second switch through which a second power supply voltage is coupled to the first sense amplifier section, a third switch through which a third power supply voltage is coupled to the second sense amplifier section, and a fourth switch through which a fourth power supply voltage is coupled to the second sense amplifier section.

38. The memory device of claim 37 wherein the first, second, third and fourth switches comprise respective FET transistors.

39. The memory device of claim 37 wherein the first power supply voltage is the same as the third power supply voltage, and the second power supply voltage is different from the fourth power supply voltage.

40. The memory device of claim 39 wherein the first and second power supply voltages are positive, the second power supply voltage is negative, and the fourth power supply voltage is zero volts.

41. The memory device of claim 34 wherein the memory device comprises a dynamic random access memory device.

42. The memory device of claim 41 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

43. A computer system, comprising:
a processor having a processor bus;
an input device coupled to the processor through the processor bus to allow data to be entered into the computer system;
an output device coupled to the processor through the processor bus to allow data to be output from the computer system;
a data storage device coupled to the processor through the processor bus to allow data to be read from a mass storage device;
a memory controller coupled to the processor through the processor bus; and
a memory device coupled to the memory controller, the memory device comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

at least one array of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a plurality of sense amplifiers provided for respective columns of memory cells in the at least one array, each of the sense amplifiers comprising:

a first sense amplifier section comprising:

first and second complementary sense lines;

a first p-channel sense transistor having its source and drain coupled between the first sense line and a first voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second sense line and the first voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first sense line and a second voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second sense line and the second voltage, and its gate coupled to the first sense line;

a second sense amplifier section comprising:

a pair of complementary digit lines;

a first p-channel sense transistor having its source and drain coupled between the first digit line and a third voltage, and its gate coupled to the second sense line;

a second p-channel sense transistor having its source and drain coupled between the second digit line and the third voltage, and its gate coupled to the first sense line;

a first n-channel sense transistor having its source and drain coupled between the first digit line and a fourth voltage, and its gate coupled to the second sense line;

a second n-channel sense transistor having its source and drain coupled between the second digit line and the fourth voltage, and its gate coupled to the first sense line;

a first coupling transistor having its source and drain coupled between the first sense line and the first digit line; and

a second coupling transistor having its source and drain coupled between the second sense line and the second digit line;

a data path circuit operable to couple data signals corresponding to the data bits between the sense amplifiers and external data terminals of the memory device; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

44. The computer system of claim 43 wherein the first voltage and the third voltage are equal to each other.

45. The computer system of claim 44 wherein the first and third voltage comprise a positive voltage.

46. The computer system of claim 43 wherein the second voltage and the fourth voltage are different from each other.

47. The computer system of claim 46 wherein the second voltage comprises a negative voltage and the fourth voltage comprises zero volts.

48. The computer system of claim 43, further comprising a control circuit coupled to a gate of the first coupling transistor and to a gate of the second coupling transistor.

49. The computer system of claim 48 wherein the coupling transistors comprise respective n-channel transistors.

50. The computer system of claim 43 wherein the memory device comprises a dynamic random access memory device.

51. The computer system of claim 50 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

52. A computer system, comprising:

- a processor having a processor bus;
- an input device coupled to the processor through the processor bus to allow data to be entered into the computer system;
- an output device coupled to the processor through the processor bus to allow data to be output from the computer system;
- a data storage device coupled to the processor through the processor bus to allow data to be read from a mass storage device;
- a memory controller coupled to the processor through the processor bus; and
- a memory device coupled to the memory controller, the memory device comprising:
 - a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;
 - a column address circuit operable to receive and decode column address signals applied to the external address terminals;
 - at least one array of memory cells arranged in rows and columns, each of the memory cells being operable to store a data bit written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;
 - a plurality of sense amplifiers provided for respective columns of memory cells in the at least one array, each of the sense amplifiers comprising:
 - a first sense amplifier section having complementary first and second output terminals and complementary first and second input terminals,

the first input terminal being coupled to the second output terminal, and the second input terminal being coupled to the first output terminal;

a second sense amplifier section having complementary first and second output terminals and complementary first and second input terminals, the first input terminal being coupled to the second output terminal of the first sense amplifier section, and the second input terminal being coupled to the first output terminal of the first sense amplifier section; and

a coupling circuit configured to couple the first output terminal of the first sense amplifier section to the first output terminal of the second sense amplifier section, and to couple the second output terminal of the first sense amplifier section to the second output terminal of the second sense amplifier section;

a data path circuit operable to couple data signals corresponding to the data bits between the sense amplifiers and external data terminals of the memory device; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

53. The computer system of claim 52 wherein the coupling circuit comprises:

a first switch coupling the first output terminal of the first sense amplifier section to the first output terminal of the second sense amplifier section, the first switch having a control terminal; and

a second switch coupling the second output terminal of the first sense amplifier section to the second output terminal of the second sense amplifier section, the second switch having a control terminal.

54. The computer system of claim 53 wherein the first and second switches comprise respective FET transistors.

55. The computer system of claim 52, further comprises a first switch through which a first power supply voltage is coupled to the first sense amplifier section, a second switch through which a second power supply voltage is coupled to the first sense amplifier section, a third switch through which a third power supply voltage is coupled to the second sense amplifier section, and a fourth switch through which a fourth power supply voltage is coupled to the second sense amplifier section.

56. The computer system of claim 55 wherein the first, second, third and fourth switches comprise respective FET transistors.

57. The computer system of claim 55 wherein the first power supply voltage is the same as the third power supply voltage, and the second power supply voltage is different from the fourth power supply voltage.

58. The computer system of claim 57 wherein the first and third power supply voltages are positive, the second power supply voltage is negative, and the fourth power supply voltage is zero volts.

59. The computer system of claim 52 wherein the memory device comprises a dynamic random access memory device.

60. The computer system of claim 59 wherein the dynamic random access memory device comprises a synchronous dynamic random access memory device.

61. A method of sensing a differential voltage between a pair of complementary digit lines, comprising:

providing a first sense amplifier having a pair of complementary inputs and a pair of complementary outputs, the complementary inputs complementary outputs of the first sense amplifier being cross-coupled to each other;

providing a second sense amplifier having a pair of complementary inputs and a pair of complementary outputs, the complementary inputs of the second sense amplifier being coupled to the corresponding complementary outputs of the first sense amplifier, and the complementary outputs of the second sense amplifier being coupled to respective ones of the complementary digit lines;

coupling the complementary outputs of the first sense amplifier to the corresponding complementary outputs of the second sense amplifier during an initial sensing period; and

after the initial sensing period, isolating the complementary outputs of the first sense amplifier from the corresponding complementary outputs of the second sense amplifier.

62. The method of claim 61, further comprising:

applying power to the first sense amplifier during the initial sensing period and thereafter; and

applying power to the second sense amplifier after the initial sensing period, but leaving the second sense amplifier unpowered during the initial sensing period.

63. The method of claim 62 wherein the act of applying power to the first sense amplifier comprising applying a positive supply voltage and a negative supply voltage to the first sense amplifier.

64. The method of claim 63 wherein the act of applying power to the second sense amplifier comprising applying a positive supply voltage and ground to the second sense amplifier.

65. A method of sensing a differential voltage between a pair of complementary digit lines, comprising:

providing a first sense amplifier having a pair of complementary inputs and a pair of complementary outputs;

coupling the differential voltage to the complementary inputs of the first sense amplifier;

allowing the first sense amplifier to respond to the differential amplifier;

using the first sense amplifier to drive a pair of complementary inputs of a second sense amplifier, the second sense amplifier having and a pair of complementary outputs coupled to respective ones of the complementary digit lines.

66. The method of claim 65 wherein the act of coupling the differential voltage to the complementary inputs of the first sense amplifier comprises coupling the complementary digit lines to respective ones of the complementary inputs of the first sense amplifier.

67. The method of claim 66 wherein the act of coupling the complementary digit lines to respective ones of the complementary inputs of the first sense amplifier comprises:

coupling the digit lines to the complementary inputs of the first sense amplifier for an initial sensing period that is significantly shorter than a period of time that the first sense amplifier needs to fully respond to the differential voltage; and

isolating the digit lines from the complementary inputs of the first sense amplifier after the initial sensing period.

68. The method of claim 65 wherein the act of using the first sense amplifier to drive a pair of complementary inputs of a second sense amplifier comprises coupling the complementary outputs of the first sense amplifier to respective ones of the complementary inputs of the second sense amplifier.

69. A method of reading a data bit from a memory cell, comprising:

providing a first sense amplifier having a pair of complementary inputs and a pair of complementary outputs;

providing a second sense amplifier having a pair of complementary inputs and a pair of complementary outputs, the complementary inputs being coupled to the corresponding complementary outputs of the first sense amplifier, and the complementary outputs being coupled to respective complementary digit lines;

coupling a memory cell to one of the complimentary digit lines;

coupling the complementary inputs of the first sense amplifier to respective ones of the digit lines during an initial sensing period after coupling the memory cell to one of the complimentary digit lines;

isolating the first sense amplifier from the digit lines and applying power to the first sense amplifier to allow the first sense amplifier to respond to the a voltage imparted to one of the complimentary digit lines by the memory cell;

after applying power to the first sense amplifier, applying power to the second sense amplifier to allow the second sense amplifier to drive the complimentary digit line to logic levels corresponding to a voltage stored in the memory cell; and

coupling the digit lines through respective input/output lines.

70. The method of claim 69 wherein the act of applying power to the first sense amplifier comprises applying a positive supply voltage and a negative supply voltage to the first sense amplifier.

71. The method of claim 70 wherein the act of applying power to the second sense amplifier comprises applying a positive supply voltage and ground to the second sense amplifier.

72. The method of claim 69 wherein the act of coupling the complementary inputs of the first sense amplifier to respective ones of the digit lines during an initial sensing period comprises coupling the complementary inputs of the first sense

amplifier to respective ones of the digit lines before and after coupling the memory cell to one of the complimentary digit lines.