

LEAKAGE COMPENSATION DYNAMIC REGISTER, DATA OPERATION UNIT, CHIP, HASH BOARD, AND COMPUTING APPARATUS

ABSTRACT

The invention provides a leakage compensation dynamic register, a data operation unit, a chip, a hash board, and a computing apparatus. The leakage compensation dynamic register comprises: an input terminal, an output terminal, a clock signal terminal, and an analog switch unit; a data latch unit for latching the data under control of the clock signal; and an output drive unit for inverting and outputting the data received from the data latch unit, the analog switch unit, the data latch unit, and the output drive unit being sequentially connected in series between the input terminal and the output terminal, and the analog switch unit and the data latch unit having a node therebetween, wherein the leakage compensation dynamic register further comprises a leakage compensation unit electrically connected between the node and the output terminal. The invention can effectively compensate for a dynamic leakage current of the node, thereby improving data security and accuracy.

(FIG. 2)