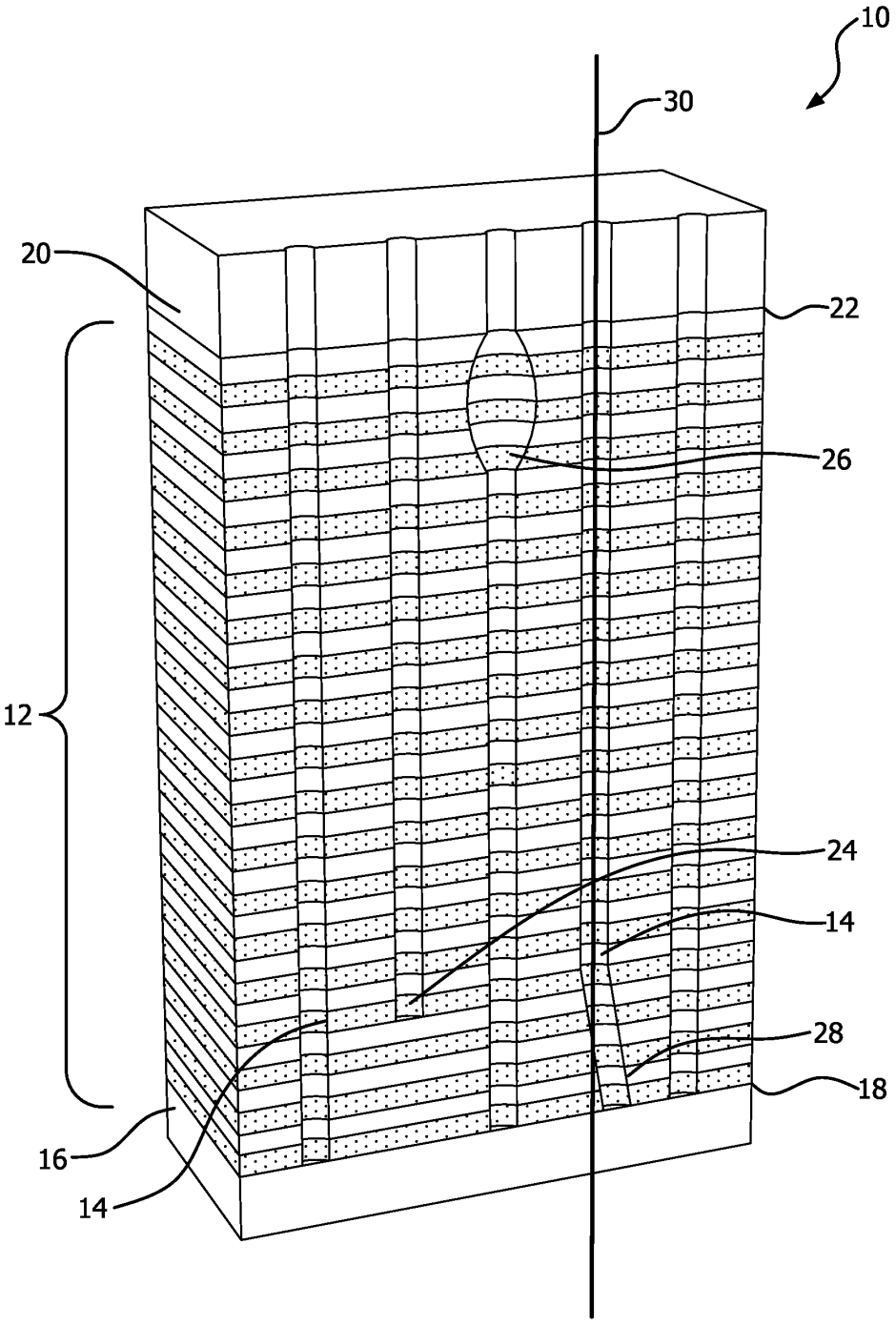


FIG. 1

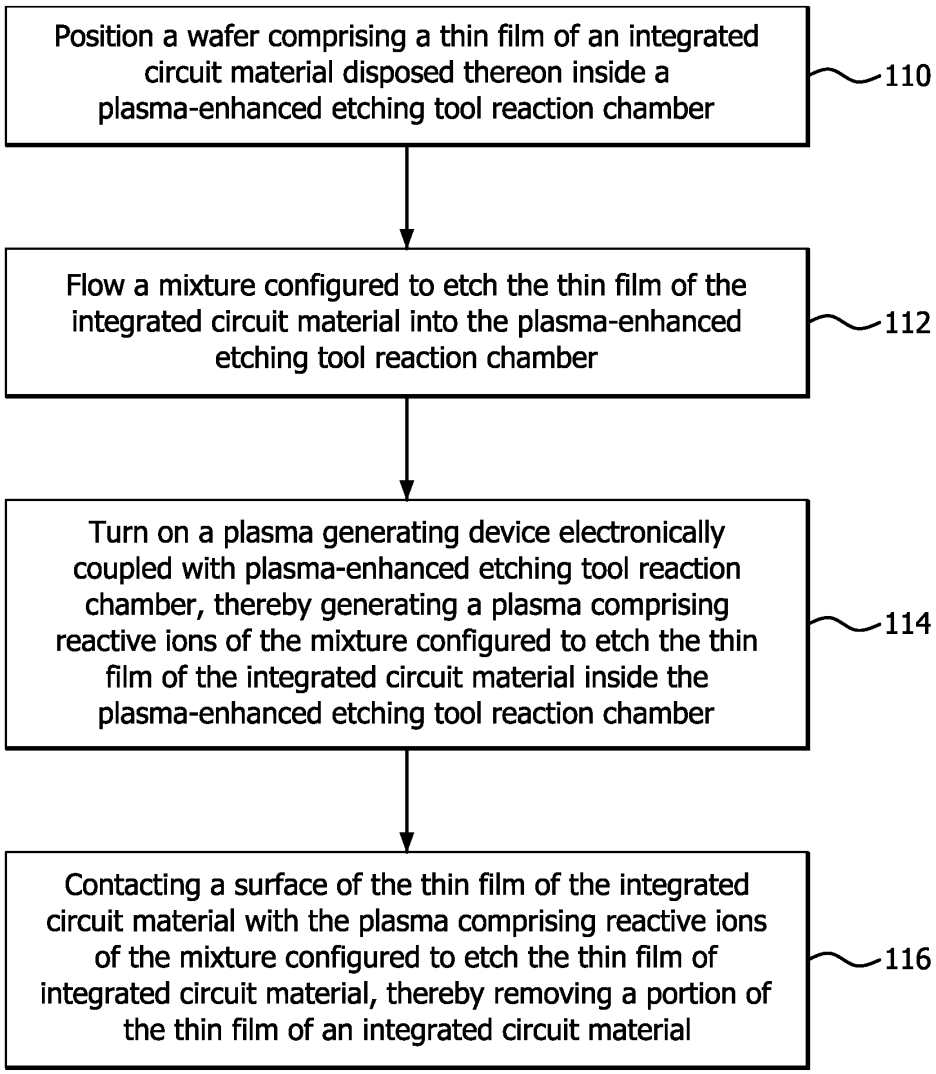

Position a wafer comprising a thin film of an integrated circuit material disposed thereon inside a plasma-enhanced etching tool reaction chamber
110
Flow a mixture configured to etch the thin film of the integrated circuit material into the plasma-enhanced etching tool reaction chamber
112
Turn on a plasma generating device electronically coupled with plasma-enhanced etching tool reaction chamber, thereby generating a plasma comprising reactive ions of the mixture configured to etch the thin film of the integrated circuit material inside the plasma-enhanced etching tool reaction chamber
114
Contacting a surface of the thin film of the integrated circuit material with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material, thereby removing a portion of the thin film of an integrated circuit material
116

FIG. 2

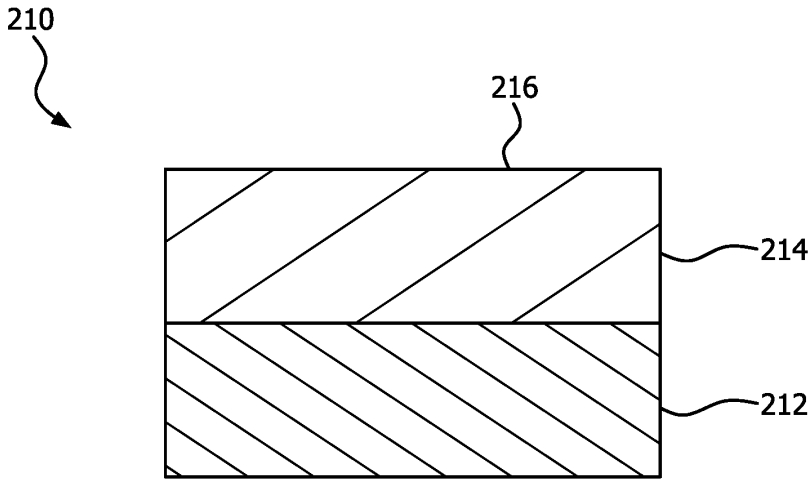


FIG. 3

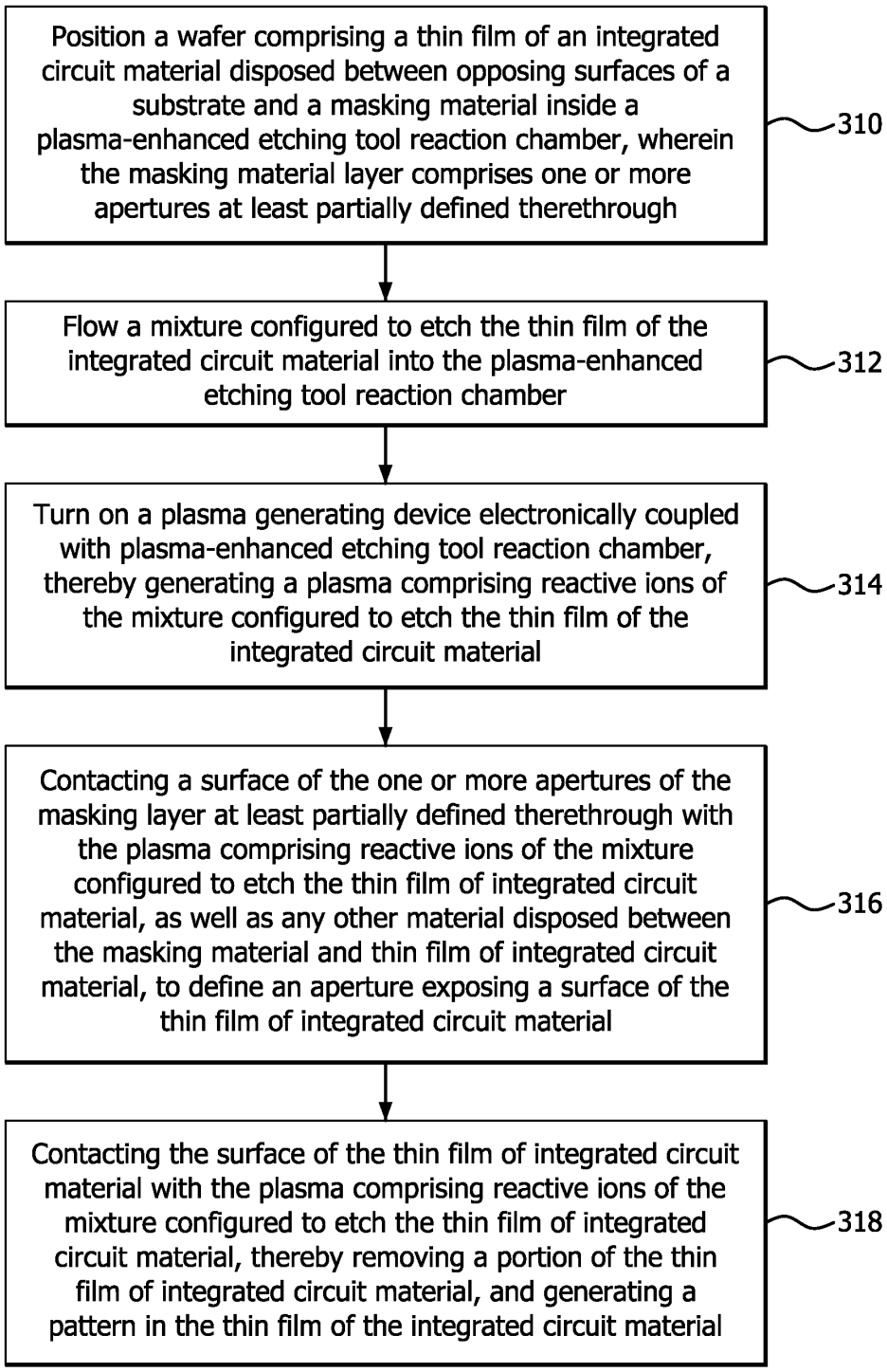

Position a wafer comprising a thin film of an integrated circuit material disposed between opposing surfaces of a substrate and a masking material inside a plasma-enhanced etching tool reaction chamber, wherein the masking material layer comprises one or more apertures at least partially defined therethrough
310
Flow a mixture configured to etch the thin film of the integrated circuit material into the plasma-enhanced etching tool reaction chamber
312
Turn on a plasma generating device electronically coupled with plasma-enhanced etching tool reaction chamber, thereby generating a plasma comprising reactive ions of the mixture configured to etch the thin film of the integrated circuit material
314
Contacting a surface of the one or more apertures of the masking layer at least partially defined therethrough with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material, as well as any other material disposed between the masking material and thin film of integrated circuit material, to define an aperture exposing a surface of the thin film of integrated circuit material
316
Contacting the surface of the thin film of integrated circuit material with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material, thereby removing a portion of the thin film of integrated circuit material, and generating a pattern in the thin film of the integrated circuit material
318

FIG. 4

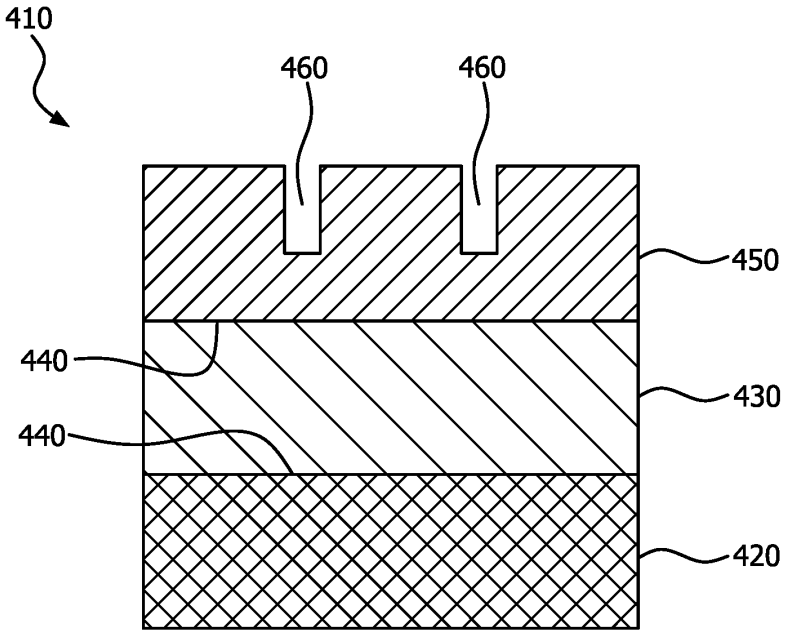


FIG. 5A

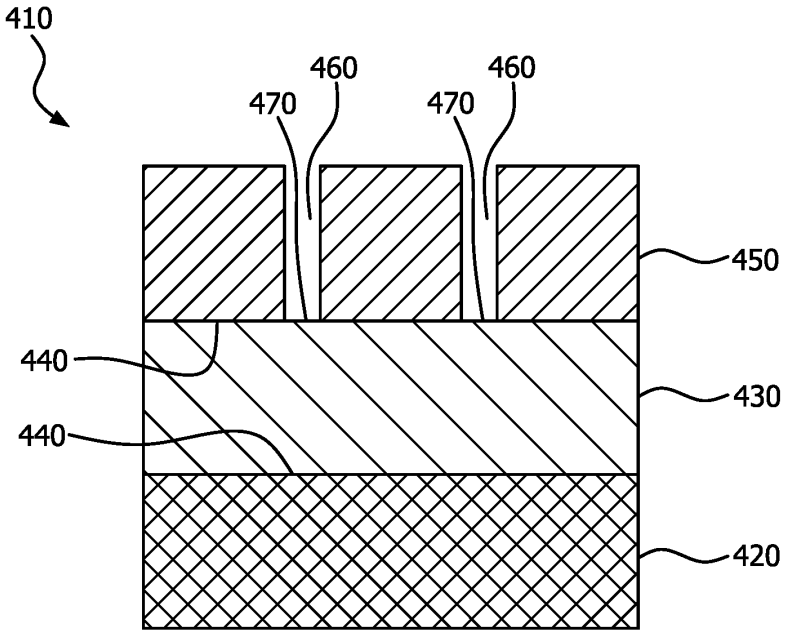


FIG. 5B

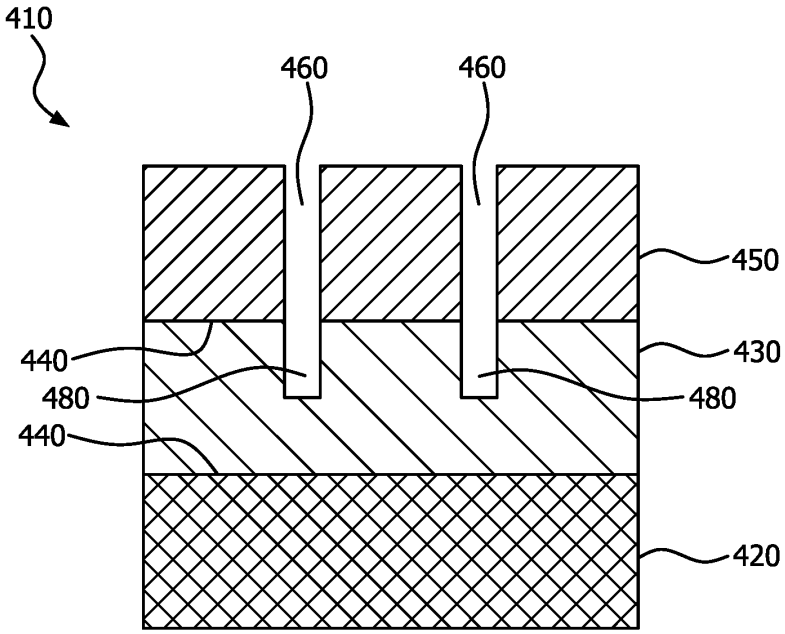


FIG. 5C

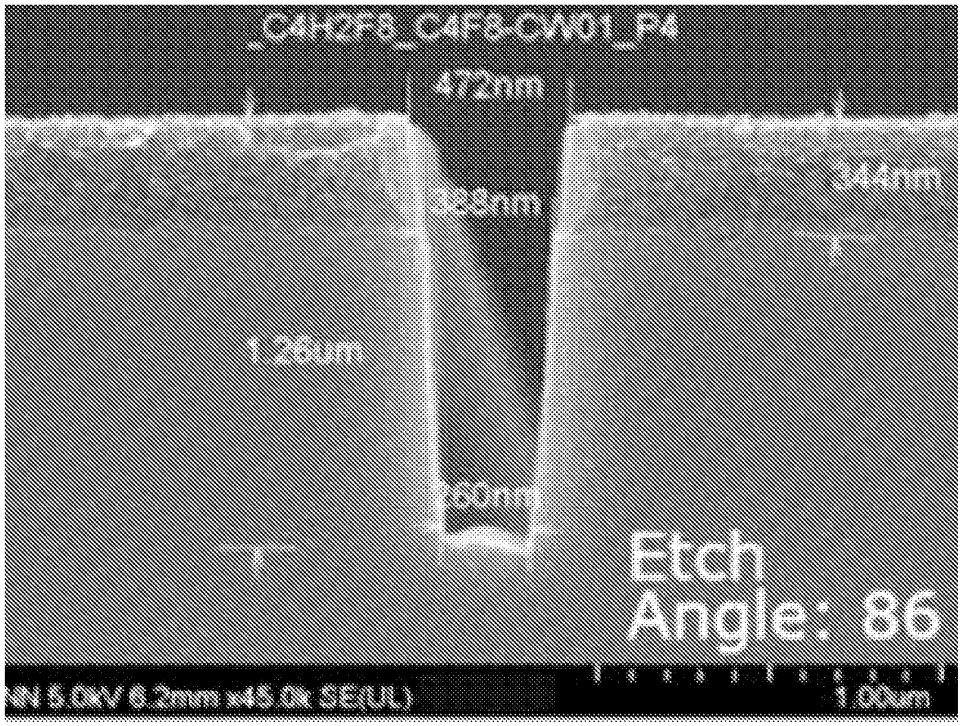

_C4H2F8_C4F8-CW01_P4
472nm
328nm
344nm
1.25um
260nm
Etch
Angle: 86
1.00um

FIG. 6A

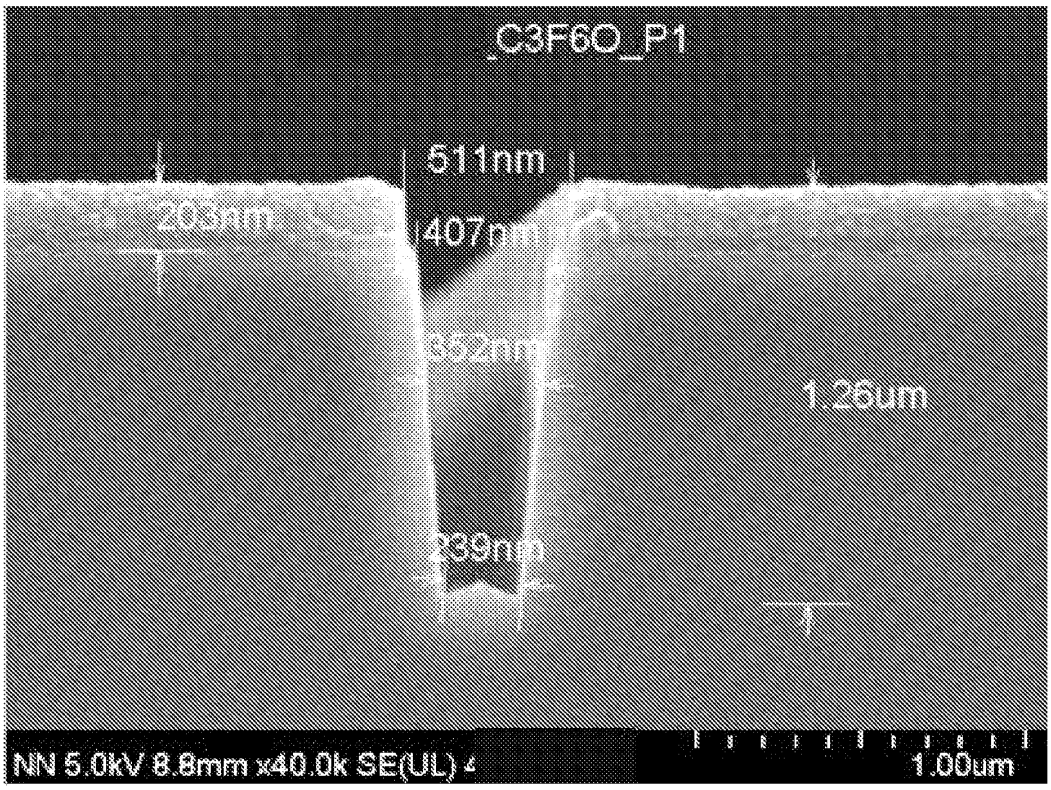

_C3F6O_P1
511nm
203nm
407nm
352nm
1.26um
239nm
NN 5.0kV 8.8mm x40.0k SE(UL)
1.00um

FIG. 6B

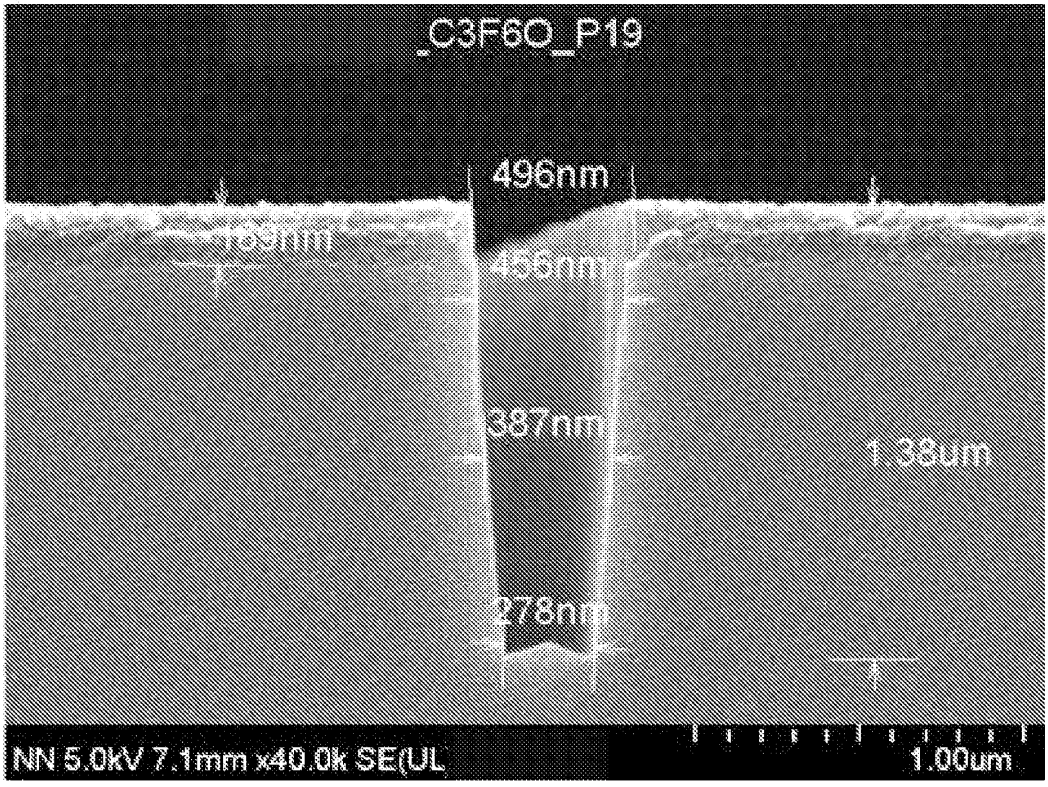

_C3F6O_P19
496nm
199nm
455nm
387nm
1.38um
278nm
NN 5.0kV 7.1mm x40.0k SE(UL
1.00um

FIG. 6C

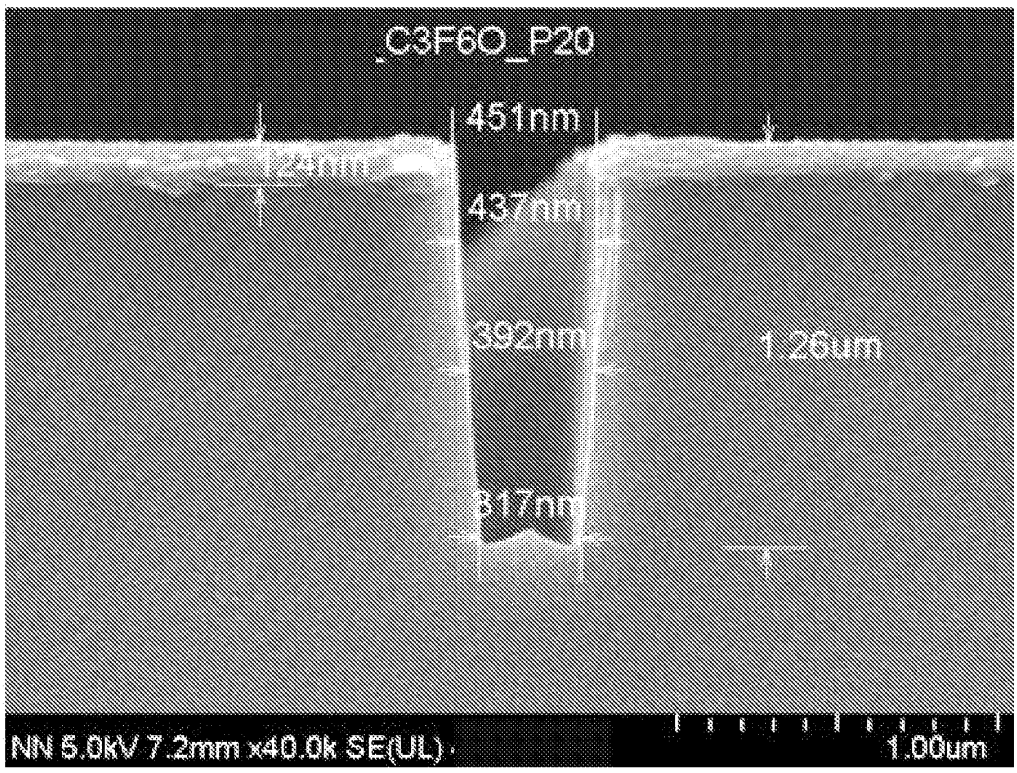

_C3F6O_P20
451nm
124nm
437nm
392nm
1.26um
317nm
NN 5.0kV 7.2mm x40.0k SE(UL)
1.00um

FIG. 6D

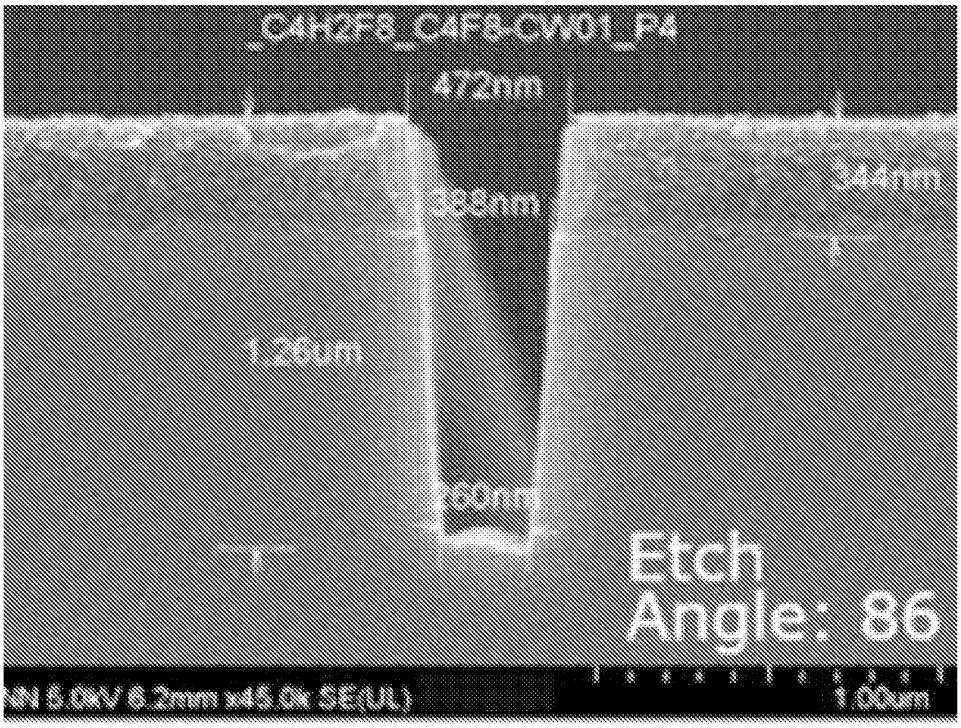

_C4H2F8_C4F8-CM01_F4
472nm
328nm
344nm
1.26um
160nm
Etch
Angle: 86
1.00um

FIG. 7A

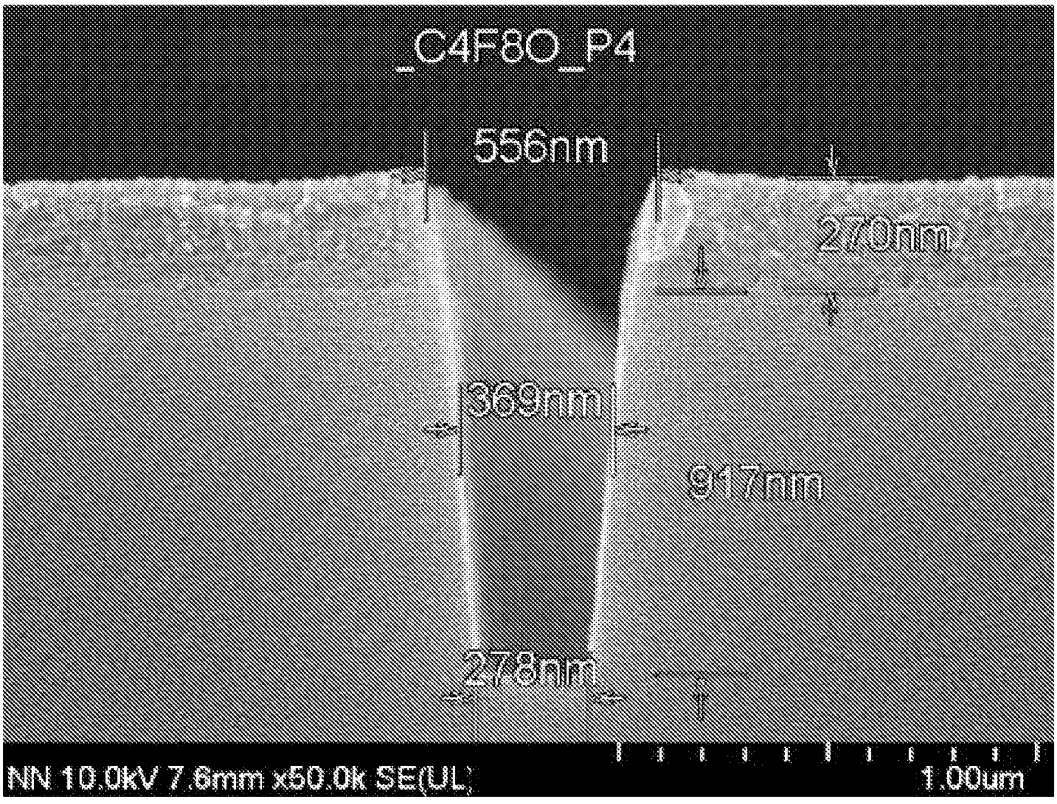

_C4F8O_P4
556nm
270nm
369nm
917nm
278nm
NN 10.0kV 7.6mm x50.0k SE(UL)
1.00um

FIG. 7B

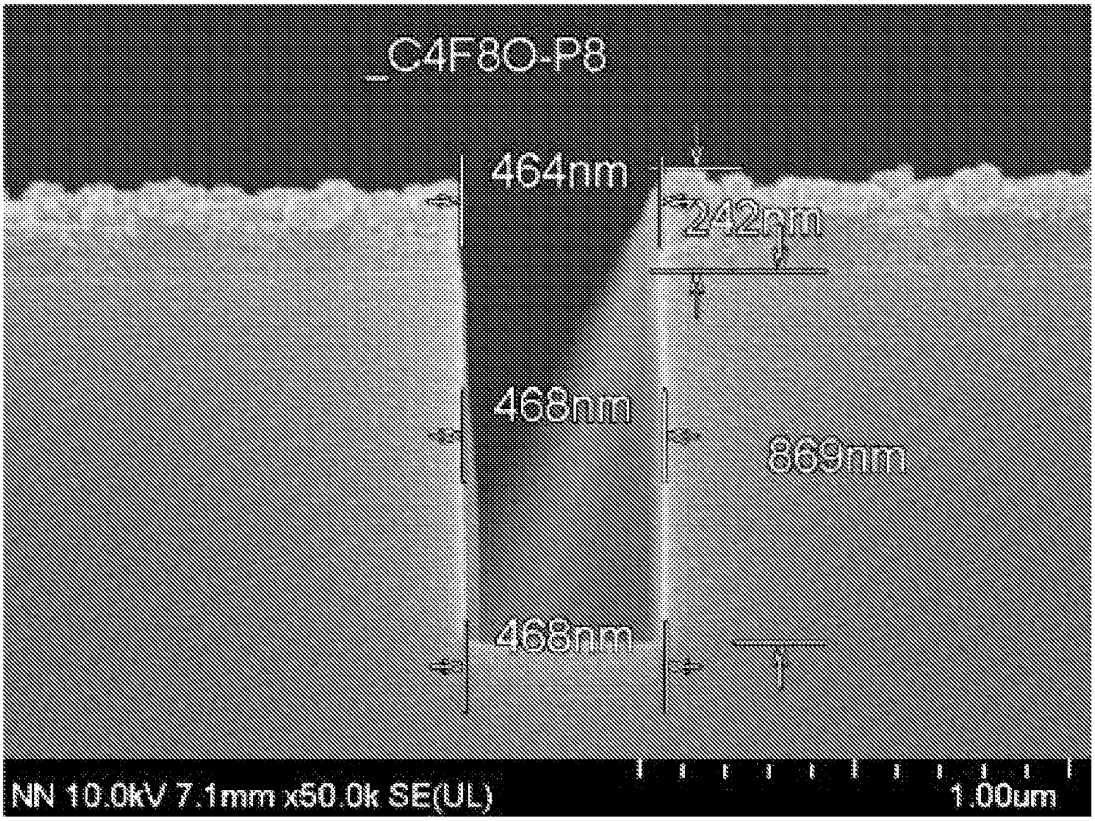

_C4F8O-P8
464nm
242nm
468nm
869nm
468nm
NN 10.0kV 7.1mm x50.0k SE(UL)
1.00um

FIG. 7C

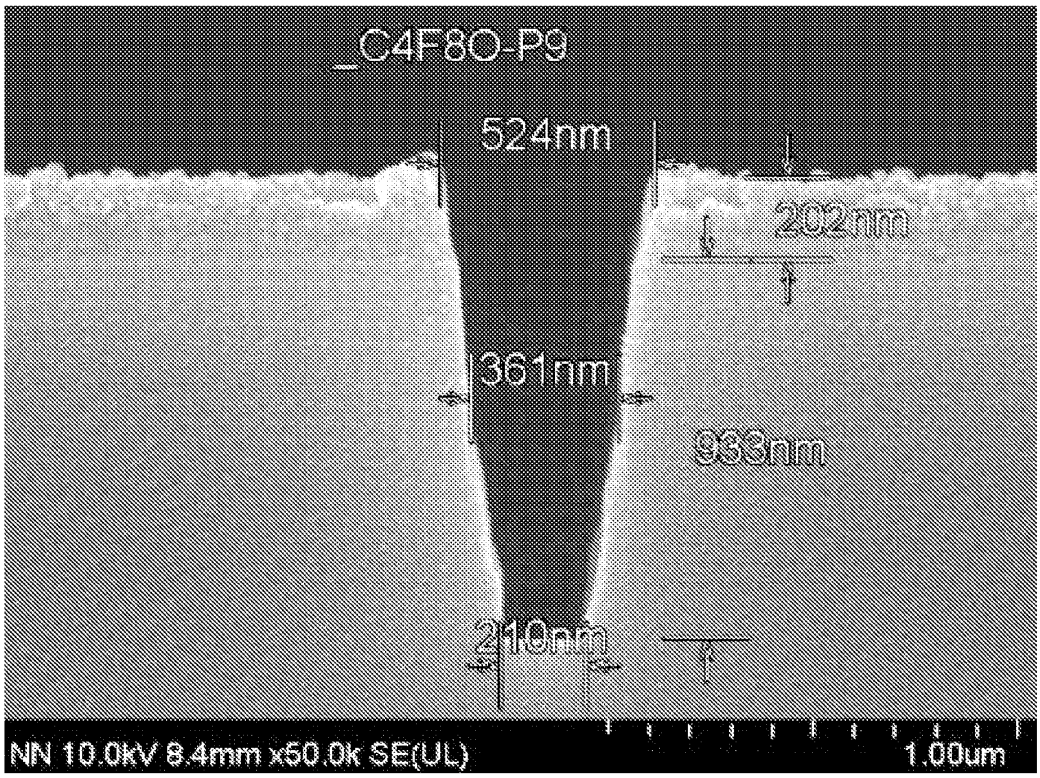

_C4F8O-P9
524nm
202nm
361nm
933nm
210nm
NN 10.0kV 8.4mm x50.0k SE(UL)
1.00um

FIG. 7D

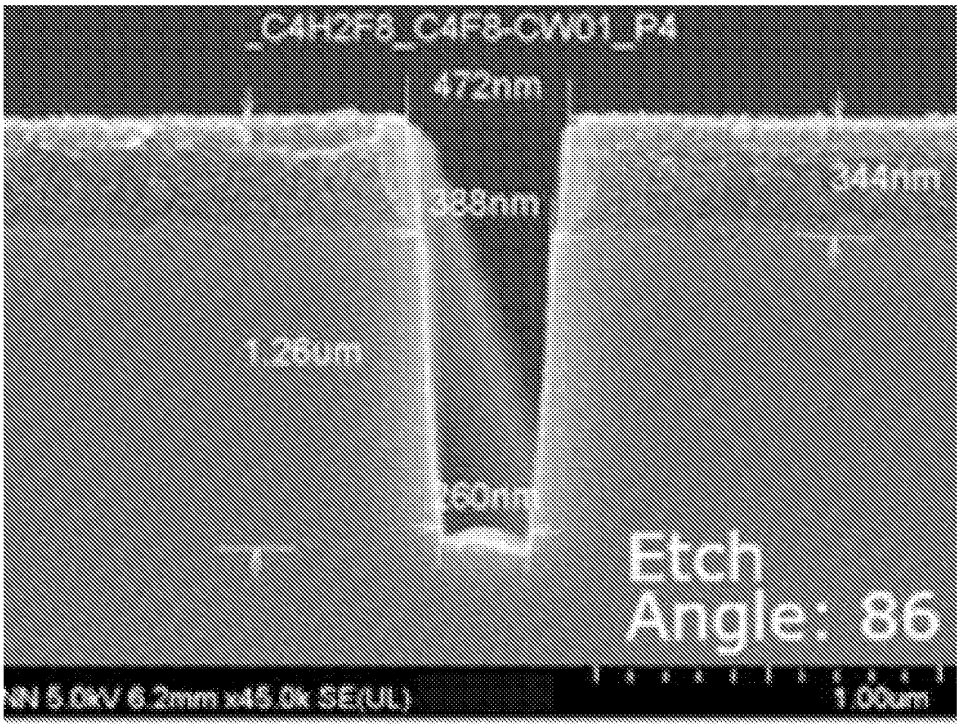

_C4H2F8_C4F8-CW01_P4
472nm
344nm
338nm
1.26um
160nm
Etch
Angle: 86

FIG. 8A

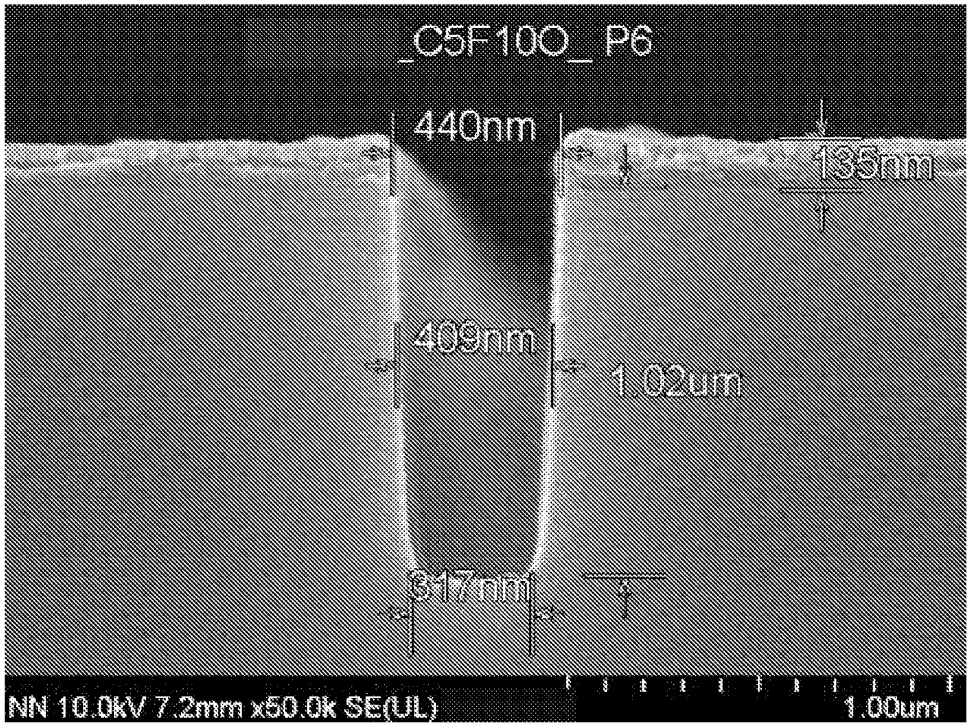

_C5F10O_ P6
440nm
136nm
409nm
1.02um
317nm
NN 10.0kV 7.2mm x50.0k SE(UL)
1.00um

FIG. 8B

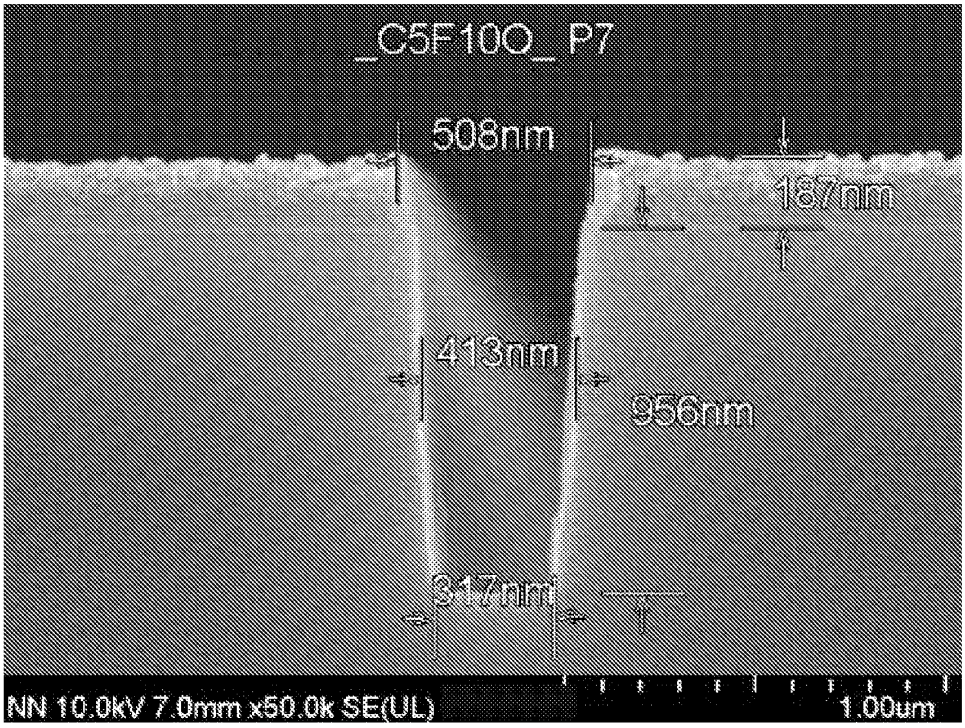

_C5F10O_ P7
508nm
187nm
413nm
956nm
317nm
NN 10.0kV 7.0mm x50.0k SE(UL)
1.00um

FIG. 8C

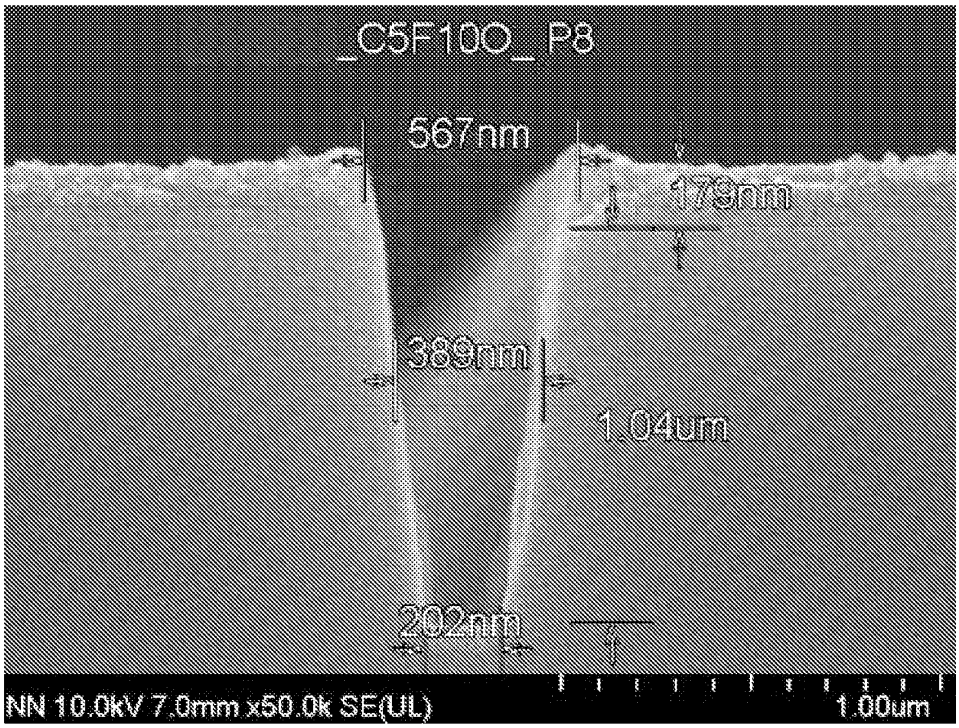

_C5F10O_ P8
567nm
179nm
389nm
1.04um
202nm
NN 10.0kV 7.0mm x50.0k SE(UL)
1.00um

FIG. 8D