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(54) Title: RESISTIVE RANDOM ACCESS MEMORY INTEGRATED WITH STACKED VERTICAL TRANSISTORS

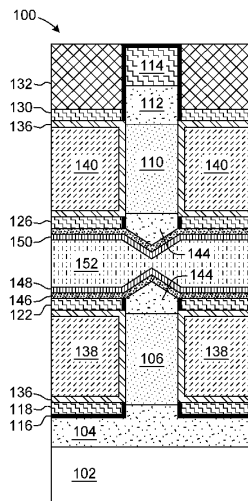


FIG. 15

(57) Abstract: A method may include forming two vertical transport field effect transistors stacked one atop the other and separated by a resistive random access memory structure. The two vertical transport field effect transistors may include a source (104, 112), a channel (106, 110), and a drain, wherein a contact layer (152) of the resistive random access memory structure functions as the drain of the two vertical transport field effect transistors. Forming the two vertical transport field effect transistors may further include forming a first source (104) and a second source (112). The first source (104) is a bottom source and the second source (112) is a top source. The method may include forming a gate conductor layer (138, 140) surrounding the channel (106, 110). The resistive random access memory structures may include faceted epitaxy (144) defined by pointed tips. The pointed tips of the faceted epitaxy (144) may extend vertically toward each other. The faceted epitaxy (144) may be between the two vertical transport field effect transistors.

[Continued on next page]

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