DIGITAL SIGNAL PROCESSING CIRCUIT FOR A TELEVISION RECEIVER

ABSTRACT

Digital signal processing circuit for a television receiver comprising: a first field memory for storing input data representative of the chrominance or luminance portion of one field; first interpolation means for generating interpolated line data based on line data received from said first field memory; zooming and up-conversion control means for controlling the read-out of line data from said first field memory and the interpolation performed by said interpolation means based on a zoom factor input to said zooming and up-conversion control means.

(No suitable figure)

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