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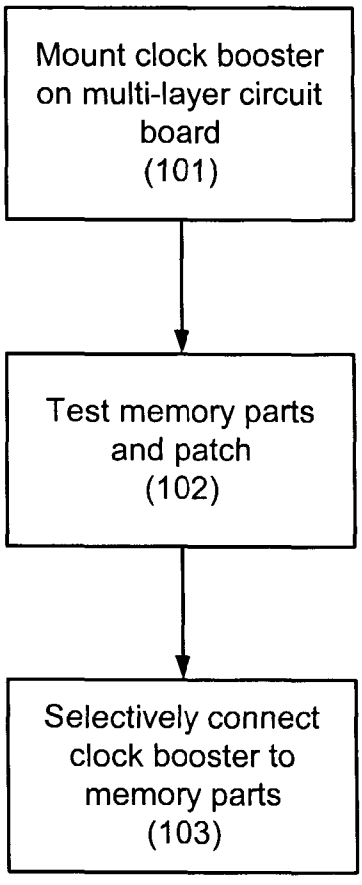
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(54) Title: MEMORY MODULE ASSEMBLY USING PARTIALLY DEFECTIVE CHIPS



(57) Abstract: A method of fabricating a memory module according to one embodiment, a clock booster is mounted on a multi-layer circuit bard (101). The clock booster may be any apparatus that receives a clock input, and output one or more clock signals capable of driving a multiplicity of logic parts without clock distortion. In a preferred embodiment, a phase-locked loop circuit may be used as a clock booster. The test and patching (102) allows a fully-functional memory part adds, it is desirable to only connect the clock signal to those memory parts that are utilized. This may be accomplished using any number of switching mechanisms to connect or disconnect a clock signal to a memory part. In a preferred embodiment, a clock patching network may be used to selectively connect or disconnect outputs of a clock booster to the memory parts (103).

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