

PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE CONTAINING PURIFIED SILICON-28 AND DEVICE THUS OBTAINED

Technical field

The invention relates to the field of semiconductor devices, and more specifically to a process for fabricating a semiconductor device having an upper layer of silicon of isotope ^{28}Si with very little isotope ^{29}Si , which is particularly advantageous for producing spin qubits using silicon technology. The invention also relates to a device obtained by said process.

Technical background

Standard silicon naturally contains isotopes with 14 and 15 neutrons, denoted ^{28}Si and ^{29}Si respectively. Thus, the silicon commonly used in electronics contains approximately 4% of isotope ^{29}Si . However, for certain applications, it is desirable to have a silicon layer with a very low concentration of ^{29}Si . This is particularly the case when producing devices with spin qubits using silicon technology, where it is desirable to have a silicon layer housing the qubits that is as pure as possible in ^{28}Si , in order to prevent rapid decoherence of the qubits.

Although it is known how to grow pure layers of silicon isotope ^{28}Si by epitaxy, a problem arises when it is desired to obtain a pure layer of silicon isotope ^{28}Si on a silicon on insulator (SOI) substrate. Such an SOI substrate comprises a silicon substrate, a layer of buried oxide, BOX, on the silicon substrate, and a first upper layer of silicon on the buried oxide layer.

The formation of pure layers of silicon of isotope ^{28}Si is very costly, as the purified precursor gas containing only the isotope ^{28}Si is very expensive. It is therefore not economically viable to produce a completely pure SOI substrate from silicon of isotope ^{28}Si . The first upper layer of silicon and/or the buried oxide layer therefore generally also contain silicon of isotope ^{29}Si .

A pure layer of silicon of isotope ^{28}Si produced on the first upper layer of silicon is contaminated by ^{29}Si isotopes migrating from the first upper silicon layer and/or the buried oxide layer, since these layers contain them, in particular during subsequent steps of semiconductor device fabrication, such as the production of transistors, which generally involve high temperatures capable of causing the ^{29}Si isotopes to migrate. The performance of the qubits in this silicon layer is therefore not optimal.

Description of the invention

The invention therefore aims to provide a process for obtaining, at lower cost, a semiconductor device having an upper layer of silicon with a very low concentration of isotope ^{29}Si .

For this purpose, the invention proposes a process for fabricating a semiconductor device, the process comprising, starting with an initial silicon on insulator SOI structure comprising a silicon substrate, a layer of buried oxide, BOX, and a first upper layer of silicon on the buried oxide layer, the first upper layer of silicon having a first concentration of isotope ^{28}Si and a first concentration of isotope ^{29}Si :

a) epitaxial growth of a first epitaxial layer of silicon of isotope ^{28}Si on the first upper layer (6) of silicon, the first upper layer of silicon having a first thickness, and the first epitaxial layer of silicon of isotope ^{28}Si having a second thickness;

b) a first homogenisation anneal, the first epitaxial layer of silicon of isotope ^{28}Si and the first upper layer of silicon then forming a second upper layer of silicon with a second concentration of isotope ^{28}Si greater than the first concentration of isotope ^{28}Si , and a second concentration of isotope ^{29}Si less than the first concentration of isotope ^{29}Si ;

c) thinning the second upper layer to a third thickness.

The process is advantageously supplemented by the various following features, taken individually or in various possible combinations:

- the first thickness is less than the third thickness;
- the first thickness is less than 5 nm, and preferably less than or equal to 3 nm;
- the second thickness is greater than 50 nm, and preferably greater than 100 nm;
- the third thickness is between 12 nm and 25 nm.

Advantageously, the process may comprise, following the thinning of the second upper layer:

d) the epitaxial growth, of a second epitaxial layer of silicon of isotope ^{28}Si on the second upper layer 10 of silicon thinned to the third thickness, the second epitaxial layer of silicon of isotope ^{28}Si having a fourth thickness;

e) a second homogenisation anneal, the second epitaxial layer 12 of silicon of isotope ^{28}Si , and the second upper layer of silicon thinned to the third thickness (T_3), then forming a third upper layer of silicon with a third concentration of isotope ^{28}Si greater than the second concentration of isotope ^{28}Si , and a third concentration of isotope ^{29}Si that is less than the second concentration of isotope ^{29}Si .

In this case, the third thickness is preferably less than or equal to 6 nm. Preferably also, the second and fourth thickness are greater than 20 nm. Preferably, the second thickness and/or the fourth thickness are less than 60 nm, and more preferably less than 50 nm.

In all cases, the process may advantageously be supplemented by the various following features, either taken individually or in the various possible combinations thereof:

- the epitaxial growth of a first epitaxial layer of silicon of isotope ^{28}Si and the epitaxial growth of a second epitaxial layer of silicon of isotope ^{28}Si are carried out using a purified precursor gas containing only isotope ^{28}Si .
- the steps of the process are implemented for a first region of a surface of the semiconductor device, and are not implemented for a second region of the surface of the semiconductor device, the process subsequently comprising the formation of transistors on the second region of the surface of the semiconductor device, the first region of the surface being configured to house qubits;
- the first region has a thickness at least 2 nm greater than the thickness of the second region;
- the process may subsequently comprise the production of isolation trenches, and filling of the isolation trenches using a purified precursor gas containing only isotope ^{28}Si ;
- the process may comprise a subsequent step of locally bombarding a surface of the structure with argon in order to make the thickness of the third layer of silicon uniform;
- the process may comprise a preliminary step of thinning the first upper layer of silicon to the first thickness.

Another object of the invention relates to a device obtained by the process described above. Said device comprises a silicon substrate, a layer of buried oxide, BOX, and an upper layer of silicon on the buried oxide layer.

Description of the figures

Other features, aims and advantages of the invention will emerge from the following description, which is given purely by way of illustration and not being limiting and which should be read with reference to the attached drawings, in which:

- Figure 1 illustrates an initial silicon-on-insulator structure, according to one possible embodiment of the invention;
- Figure 2 illustrates the structure following thinning of the first upper layer of silicon, according to one possible embodiment of the invention;
- Figure 3 illustrates the structure following the epitaxial growth of a first layer of silicon of isotope ^{28}Si , according to one possible embodiment of the invention;

- Figure 4 illustrates the structure following the first homogenising annealing, according to one possible embodiment of the invention;
- Figure 5 illustrates the structure following the thinning of the second upper layer of silicon, according to one possible embodiment of the invention;
- Figure 6 illustrates the structure following the epitaxial growth of a second layer of silicon of isotope ^{28}Si , according to one possible embodiment of the invention;
- Figure 7 illustrates the structure following a second homogenisation anneal, according to one possible embodiment of the invention; and
- Figure 8 illustrates the structure following the formation of isolation trenches, according to one possible embodiment of the invention.

Detailed description

With reference to **Figure 1**, the process for fabricating a semiconductor device is implemented starting from an initial structure 1 of silicon-on-insulator, SOI, comprising a silicon substrate 2, a layer 4 of buried oxide, BOX, and a first upper layer 6 of silicon on the buried oxide layer, the first upper layer 6 of silicon having a first concentration $C_{1,28}$ of isotope ^{28}Si and a first concentration $C_{1,29}$ of isotope ^{29}Si . The silicon of the initial structure 1 is standard, i.e. it has not been substantially purified of its ^{29}Si isotopes. Typically, the first concentration $C_{1,28}$ of isotope ^{28}Si is between 92% and 93%, whilst the first concentration $C_{1,29}$ of isotope ^{29}Si is between 4% and 5%. Isotope ^{30}Si is also typically present at a concentration of approximately 3%, but has no significant implications and will not be discussed further, although the process results in the removal of this isotope ^{30}Si in the same way as isotope ^{29}Si . By way of non-limiting demonstration, the values of 96% for $C_{1,28}$ and 4% for $C_{1,29}$ are used. In the present document, the concentrations given are molar concentrations.

The initial silicon-on-insulator structure 1 is preferably a fully depleted silicon-on-insulator (FDSOI) structure, in which at least the first upper layer 6 is completely depleted. The buried oxide layer 4 is typically made of silicon oxide.

If the first upper layer 6 of silicon is not sufficiently thin and, for example, if it is thicker than a first thickness of less than or equal to 5 nm, the process may include a preliminary step of thinning the first upper layer 6 of silicon to a first thickness T_1 less than or equal to 5 nm, and preferably less than or equal to 4 nm, and more preferably less than or equal to 3 nm. For the purpose of demonstration of the following examples, the initial thickness T_1 is taken as 3 nm. Thinning can, for example, be carried out by oxidation in a furnace, followed by etching, for example chemical etching, in particular using hydrofluoric acid (HF), known as "HF wet

etching", or by so-called dry etching, for example using a plasma. **Figure 2** shows the structure with the first upper layer 6 of silicon at the first thickness T_1 .

The process comprises the epitaxial growth of a first epitaxial layer 8 of silicon of isotope ^{28}Si on the first upper layer 6 of silicon, the first epitaxial layer 8 of silicon of isotope ^{28}Si having a second thickness T_2 . Preferably, the second thickness T_2 is greater than or equal to 15 nm, and more preferably greater than or equal to 20 nm. The epitaxy can be carried out using a purified precursor gas containing only the isotope ^{28}Si , i.e. at least 99.9% of isotope ^{28}Si . For example, starting with a gas of SiF_4 , mass-selective separation enables only $^{28}\text{SiF}_4$ to be retained. Chloride compounds then enable silicon isotope ^{28}Si to be obtained. This results, as illustrated in **Figure 3**, in a first epitaxial layer 8 of isotope ^{28}Si on the first upper layer 6 of silicon, with the thickness above the buried oxide layer 4 thus corresponding to the sum of the first thickness T_1 and the second thickness T_2 .

The process then comprises a first homogenisation annealing, aimed at homogenising the concentrations of isotopes ^{28}Si and ^{29}Si between the first epitaxial silicon layer 8 and the first upper silicon layer 6, which then form a second upper layer 10 of silicon, as illustrated in **Figure 4**. The second upper layer 10 of silicon has a second concentration $C_{2,28}$ of isotope ^{28}Si greater than the first concentration $C_{1,28}$ of isotope ^{28}Si , and a second concentration $C_{2,29}$ of isotope ^{29}Si , which is less than the first concentration $C_{1,29}$ of isotope ^{29}Si . During the first homogenisation anneal, the heating of the structure 1 enables the ^{29}Si isotopes to migrate from the first upper silicon layer 6 to the first epitaxial silicon layer 8. For example, the homogenisation annealing may be carried out at a temperature of at least 1000°C for at least 20 minutes, and preferably at least 1050°C for at least 30 minutes. It is, however, possible to adjust the temperature and duration of the annealing, provided that the thermal budget enables sufficient migration of the ^{29}Si isotopes towards the upper part of the second upper layer 10. Reference can be made, for example, to the article of V. Mazzocchi et al. "*99.992% ^{28}Si CVD-grown epilayer on 300 nm substrates for large-scale integration of silicon spin qubits*", Journal of Crystal Growth 509 (2019) 1-7, for information on both epitaxial growth and homogenisation annealing in this context.

The second concentration $C_{2,29}$ of isotope ^{29}Si depends on the first thickness T_1 and the second thickness T_2 , as well as on the first concentration $C_{1,29}$ of isotope ^{29}Si :

$$C_{2,29} = C_{1,29} \times \frac{T_1}{T_1 + T_2}$$

Taking $C_{1,29} = 4\%$, $T_1 = 3$ nm, and $T_2 = 30$ nm, gives $C_{2,29} = 0.36\%$, which is one-tenth of the concentration of isotope ^{29}Si in the second upper layer of silicon compared with the first

upper layer of silicon, i.e. compared with standard silicon. It is, however, possible that some ^{29}Si isotopes may migrate from the buried oxide layer 4 to the second upper silicon layer 10 during the homogenisation annealing. However, this effect does not call into question the substantial decrease in the second concentration $C_{2,29}$ of isotope ^{29}Si compared with the first concentration $C_{1,29}$ of isotope ^{29}Si , and it is possible to limit this effect by limiting the thermal budget of the first homogenisation annealing.

The process then comprises thinning the second upper layer 10 to a third thickness T_3 , as illustrated in **Figure 5**. The same procedures as those used for any thinning of the first upper layer 6 may be employed. Preferably, the third thickness T_3 is less than or equal to 6 nm, and more preferably less than or equal to 4 nm. However, the third thickness, T_3 , may be greater than the first thickness, T_1 .

The process then comprises the epitaxial growth, of a second epitaxial layer 12 of silicon of isotope ^{28}Si on the second upper layer 10 of silicon thinned to the third thickness T_3 , the second epitaxial layer 12 of silicon of isotope ^{28}Si having a fourth thickness T_4 . Preferably, the thickness of the fourth layer T_4 is greater than or equal to 15 nm, and more preferably greater than or equal to 20 nm. This results, as illustrated in **Figure 6**, in a second epitaxial layer 12 of silicon of isotope ^{28}Si on the second upper layer 10 of silicon, with the thickness above the buried oxide layer thus corresponding to the sum of the third thickness T_3 and the fourth thickness T_4 .

The process then comprises a second homogenisation anneal, aimed at homogenising the concentrations of isotopes ^{28}Si and ^{29}Si between the second epitaxial silicon layer 12 and the second upper silicon layer 10, which then form a third upper layer 14 of silicon, as illustrated in **Figure 7**.

The third upper layer 14 of silicon has a third concentration $C_{3,28}$ of isotope ^{28}Si greater than the second concentration $C_{2,28}$ of isotope ^{28}Si , and a third concentration $C_{3,29}$ of isotope ^{29}Si , less than the second concentration $C_{2,29}$ of isotope ^{29}Si . As with the first homogenisation anneal, heating the structure enables the ^{29}Si isotopes to migrate from the second upper layer 10 of silicon to the second epitaxial layer 12 of silicon. For example, the homogenisation annealing may be carried out at a temperature of at least 1000°C for at least 20 minutes, and preferably at least 1050°C for at least 30 minutes. It is, however, possible to adjust the temperature and duration of the annealing, provided that the thermal budget enables sufficient migration of the ^{29}Si isotopes towards the upper part of the third upper layer.

The third concentration $C_{3,29}$ of isotope ^{29}Si depends on the third thickness T_3 and the fourth thickness T_4 , as well as on the second concentration $C_{2,29}$ of isotope ^{29}Si :

$$C_{3,29} = C_{2,29} \times \frac{T_3}{T_3 + T_4}$$

which can also be expressed as a function of the first concentration $C_{1,29}$ of isotope ^{29}Si :

$$C_{3,29} = C_{1,29} \times \frac{T_1}{T_1 + T_2} \times \frac{T_3}{T_3 + T_4}$$

Taking $C_{1,29} = 4\%$, $T_1 = 3$ nm, $T_2 = 30$ nm, $T_3 = 5$ nm and $T_4 = 25$ nm, gives $C_{3,29} = 0.06\%$, which is less than one fiftieth of the concentration of isotope ^{29}Si in the third upper layer 14 of silicon compared with the first upper layer 6 of silicon, i.e. compared with standard silicon. A possible migration of ^{29}Si isotopes from the buried oxide layer 4 to the third upper layer 14 of silicon during the second homogenisation anneal may occur, but to an even lesser extent than before, because the concentration of ^{29}Si isotopes in the buried oxide layer 4 decreases with each migration. It is also possible to limit this effect by limiting the thermal budget during the second homogenisation anneal. In any case, it is possible to obtain a third upper layer 14 of silicon comprising less than 0.1 % of isotope ^{29}Si .

This results in a semiconductor device comprising an upper layer 14 of silicon on the buried oxide layer 4, which is virtually free of isotope ^{29}Si , having undergone only two iterations of thinning, epitaxy and thermal annealing. The process is therefore very cost-effective, as it typically requires only between 30 nm and 80 nm of epitaxial growth using an expensive precursor gas consisting solely of ^{28}Si isotopes. It is possible to increase the purity obtained by repeating a cycle of thinning and epitaxy as described, and/or by further thinning the upper layers 6, 10 of silicon during the thinning process, and/or by increasing the thickness of the epitaxial layers 8, 12. Reducing the thickness of the epitaxial layers 8 and 12 is sufficient to reduce the costs, although this may be at the expense of the degree of purity obtained.

These cycles of thinning, epitaxy and thermal annealing may have the disadvantage of compromising the thickness uniformity of the upper layer 14 of silicon, which is intended to be the active layer of the semiconductor device. However, small variations in thickness are acceptable when forming qubits in the semiconductor device, since qubits are generally formed in a thicker channel (for example, between 10 and 15 nm) than for a conventional transistor channel, which is typically between 7 and 10 nm thick. If it is desired to improve the homogeneity of the thickness of the final upper layer 14 of silicon, which is above the buried oxide layer 4, it is possible to carry out a trimming process, for example by bombarding the upper layer of silicon with argon.

The process can be implemented either across an entire wafer, or only on the regions intended to house qubits, in order to reduce the consumption of pure ^{28}Si precursor gas. In addition, by not implementing the process in certain regions, it is possible to maintain a thinner and more uniform thickness of the upper silicon layer in the regions intended to form the transistors, and to have a greater thickness in the purified regions intended for the qubits. Thus, preferably, the steps of the process are implemented for a first region of a surface of the semiconductor device, and are not implemented for a second region of the surface of the semiconductor device, the process subsequently comprising the formation of transistors on the second region of the surface of the semiconductor device, the first region of the surface being configured to house qubits. Preferably, the first region is at least 2 nm thicker than the second region, and more preferably at least 4 nm thicker than the second region. For example, it is possible to use a silicon nitride mask on the second region of the surface of the semiconductor device during implementation of the described process steps.

As mentioned above, subsequent fabricating steps, for example those involved in producing transistors, may cause the temperature of the semiconductor device to rise, promoting the diffusion of ^{29}Si isotopes into the final upper layer 14, from which they were virtually absent. In order to limit this diffusion, it is possible, following the process described, to produce shallow trench isolation (STI) 16, and to fill the isolation trenches 16 using a purified precursor gas containing only isotope ^{28}Si , as illustrated in **Figure 8**. Thus, the isolation trenches 16 contain no ^{29}Si isotopes, and these cannot therefore migrate into the final upper layer 14 of purified silicon produced by the process steps described. Advantageously, these are at least isolation trenches 16 located near the areas intended to house the qubits. Such isolation trenches 16 pass through at least the upper layer 14, typically also the buried oxide layer 4, and generally reach the substrate 2. However, it is possible to install isolation trenches 16 with shallower depths.

It is also possible, using the same procedures unless otherwise specified, to carry out only a single cycle of formation by epitaxy on a first epitaxial layer 8 of a second thickness T_2 , followed by a first homogenisation anneal, and thinning of the second upper layer 10 to the third thickness T_3 . In this case, the second thickness T_2 is preferably greater than or equal to 50 nm, and more preferably greater than 100 nm. As before, the second concentration $C_{2,29}$ of isotope ^{29}Si depends on the first thickness T_1 and the second thickness T_2 , as well as on the first concentration $C_{1,29}$ of isotope ^{29}Si :

$$C_{2,29} = C_{1,29} \times \frac{T_1}{T_1 + T_2}$$

Taking $C_{1,29} = 4\%$, $T_1 = 3$ nm, and $T_2 = 60$ nm, gives $C_{2,29} = 0.48\%$, which is less than one eighth of the concentration of isotope ^{29}Si in the second upper layer 10 of silicon compared with the first upper layer 6 of silicon, i.e. compared with standard silicon. The greater the second thickness T_2 , the more effective the purification will be; but the cost may be higher than in multi-cycle variants, which consume less epitaxial layer thickness.

Typically, the thinning reduces the second upper layer 10 by at least 30 nm, and preferably by at least 45 nm. The third layer, T_3 , is thicker, as the thinning of the second upper layer is not followed by epitaxial growth of a second epitaxial layer 12. Preferably, the third thickness T_3 is between 12 nm and 25 nm.

The invention is not limited to the embodiment described and shown in the attached figures. Modifications remain possible, in particular in terms of the constitution of the various technical features or by substitution of technical equivalents, without going beyond the scope of protection of the invention, which is defined by the following claims.

Claims

1. A process for fabricating a semiconductor device, the process comprising, starting with an initial silicon on insulator SOI structure (1), comprising a silicon substrate (2), a layer (4) of buried oxide, BOX, and a first upper layer (6) of silicon on the buried oxide layer (4), the first upper layer (6) of silicon having a first concentration of isotope ^{28}Si and a first concentration of isotope ^{29}Si :

a) forming, by epitaxy, a first epitaxial layer (8) of the isotope of silicon ^{28}Si on the first upper layer (6) of silicon, the first upper layer (6) of silicon having a first thickness (T_1) and the first epitaxial layer (8) of silicon of isotope ^{28}Si having a second thickness (T_2);

b) a first homogenisation anneal, the first epitaxial layer (8) of silicon of isotope ^{28}Si and the first upper layer (6) of silicon then forming a second upper layer (10) of silicon with a second concentration of the isotope ^{28}Si greater than the first concentration of the isotope ^{28}Si , and a second concentration of the isotope ^{29}Si less than the first concentration of the isotope ^{29}Si ;

c) thinning of the second upper layer (10) to a third thickness (T_3).

2. The process according to claim 1, wherein the first thickness (T_1) is less than the third thickness (T_3).

3. The process according to any one of the preceding claims, wherein the first thickness (T_1) is less than 5 nm, and preferably less than or equal to 3 nm.

4. The process according to one of the preceding claims, wherein the second thickness (T_2) is greater than 50 nm, and preferably greater than 100 nm.

5. The process according to one of the preceding claims, wherein the third thickness (T_3) is between 12 nm and 25 nm.

6. The process according to one of claims 1 to 3, comprising, following the thinning of the second upper layer (10):

d) epitaxial growth of a second epitaxial layer (12) of silicon of isotope ^{28}Si on the second upper layer (10) of silicon thinned to the third thickness (T_3), the second epitaxial layer (12) of silicon of isotope ^{28}Si having a fourth thickness (T_4);

e) a second homogenisation anneal, the second epitaxial layer (12) of silicon of isotope ^{28}Si , and the second upper layer (10) of silicon thinned to the third thickness (T_3), then forming a third upper layer (14) of silicon with a third concentration of isotope ^{28}Si greater than the second concentration of isotope ^{28}Si , and a third concentration of isotope ^{29}Si that is less than the second concentration of isotope ^{29}Si .

7. The process according to claim 6, wherein the third thickness (T_3) is less than or equal to 6 nm.

8. The process according to either of claims 6 or 7, wherein the second thickness (T_2) and the fourth thickness (T_4) are greater than 20 nm.

9. The process according to any one of the preceding claims, wherein the epitaxial growth of a first epitaxial layer (8) of silicon of isotope ^{28}Si and the epitaxial growth of a second epitaxial layer (12) of silicon of isotope ^{28}Si are carried out using a purified precursor gas containing only isotope ^{28}Si .

10. The process according to any one of the preceding claims, wherein the steps of the process are implemented for a first region of a surface of the semiconductor device, and are not implemented for a second region of the surface of the semiconductor device, the process subsequently comprising the formation of transistors on the second region of the surface of the semiconductor device, the first region of the surface being configured to house qubits.

11. The process according to the preceding claim, wherein the first region has a thickness at least 2 nm greater than the thickness of the second region.

12. The process according to any of the preceding claims, subsequently comprising the production of isolation trenches (16), and filling the isolation trenches (16) using a purified precursor gas containing only isotope ^{28}Si .

13. The process according to any one of the preceding claims, comprising a subsequent step of locally bombarding a surface of the structure with argon in order to make the thickness of the third layer (14) of silicon uniform.

14. The process according to any of the preceding claims, comprising a preliminary step of thinning the first upper layer (6) of silicon to the first thickness (T_1).

15. A semiconductor device comprising a silicon substrate (2), a layer (4) of buried oxide, BOX, and an upper layer (10, 14) of silicon on the buried oxide layer (4), obtained by the process according to one of claims 1 to 14.