

Synthesized Selective Call Receiver Having
Variable Characteristics

5 Background of the Invention

 This invention relates in general to a selective call receiver having a frequency synthesizer for changing receive frequencies in order to receive a paging signal.

10 This invention more specifically relates to varying characteristics of the receiver in response to the receive frequency.

 A paging receiver which receives a paging signal on one of a plurality of receive frequency channels, needs to switch between receive frequency channels. However, the lock time of a frequency synthesizer having a phase lock loop (PLL) may vary depending upon the differences in frequency between two channels. It is desirable to provide a constant lock time when switching channels regardless of the differences in frequency. Furthermore, it is desirable to lock to another channel very rapidly in one instance while the lock time may not be critical in another instance. Thus it is desirable to vary the characteristics of a selective call receiver in order to provide for a desired lock time.

 The loop filter of the PLL also effects the noise level of the synthesized frequency used within a superheterodyne receiver, the noise level effects the selectivity of the receiver. Different applications of paging receivers or different channels upon which paging receivers receive paging signals may require differing selectivity performance. Thus it is desirable to adjust the loop bandwidth of a PLL in order to provide a desired level of selectivity performance.

 During the reception process, a demodulated signal has a DC component and an AC component upon which the paging

signal is included. The DC component is removed in order to digitize the AC component. A complex circuit is used to determine and extract the DC component, such a circuit is shown in U.S. patent 4,631,737 to Davis et al. It is
5 desirable to disable this circuit while the PLL is acquiring lock.

Summary of the Invention

10 It is therefore an object of the invention to provide for the aforementioned desirable ends.

In accordance with the present invention, a selective call receiver comprises a receiving means for receiving and
15 demodulating a selective call signal, said receiving means including a phase lock loop (PLL) for programmably generating an injection frequency used to select a receive frequency for receiving the selective call signal, said receiving means further having a variable characteristic,
20 and a decoding means for processing the demodulated selective call signal and for programming the frequency of the PLL and for varying the characteristic of the receiving means in response to the programmed frequency.

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Brief Description of the Drawings

Figure 1 shows a paging receiver operating in accordance with the present invention.

30 Figure 2 shows a flow chart of a decoder operating in accordance with the present invention.

Description of a Preferred Embodiment

Figure 1 shows a paging receiver operating in accordance with the present invention. RF modulated paging signals are received on antenna 10, amplified by amplifier 12 mixed by mixer 14 with an injection frequency from synthesizer 16 in order to create an intermediate frequency signal. Demodulator 18 generates an audio signal from the intermediate frequency signal. The audio signal is digitized by the peak and valley detector 20 which generates a digital signal from the audio signal. Peak and valley detector 20 is described in U.S. patent 4,631,737 to Davis et al. which is hereby incorporated by reference.

Synthesizer 16 comprises a phase lock loop (PLL) and is driven by a reference frequency from oscillator 22. The reference frequency is compared by phase comparator 24. The output of the phase comparator is filtered by a programmable loop filter 26 which is described in U.S. patent application 07/345,809 to Herold et al. and assigned to the assignee of the present invention which provides for a variable filter characteristic. The output of the loop filter is coupled to voltage controlled oscillator 28 which generates the injection frequency. The injection frequency is further coupled to programmable divider 30 the output of which is coupled to phase comparator 24, thus closing the loop of the PLL.

Decoder 30 receives and processes the digitized signal from peak and valley detector 20 and also enables and disables the peak and valley detector. Programmable filter 26 and programmable divider 30 are also programmed by decoder 40. Decoder 40 includes a microcomputer for performing it's functions. Use of a microcomputer or control functions of a paging receiver is known in the art. A preferred microcomputer is the MC68HC05C4 microcomputer manufactured by Motorola Inc. Some elements of the invention described herein are implemented in software operating within the microcomputer.

Codeplug 50 includes several variables used to vary the characteristics of the receiver in response to the receive frequency. A first portion 52 contains frequency information and corresponding loop bandwidth information. 5 A second portion contains the change in frequency information, ΔF and corresponding bandwidth and lock time information.

For example, if substantial selectivity was required at a first frequency of 131.000 MHz, nominal selectivity 10 was required at a second frequency of 132.000 MHz and selectivity was not critical at 133.000 MHz, table 52 for the paging receiver of this example could read:

	F1 = 131.000 MHz	BW1 = 50 Hz
15	F2 = 132.000 MHz	BW2 = 75 Hz
	F3 = 133.000 MHz	BW3 = 120 Hz

The frequencies above indicate receive frequencies, alternately the injection frequency, which differs from the 20 receive frequency by the intermediate frequency, could be used, while maintaining the same bandwidths. Table 52 governs the loop bandwidth while the PLL is locked.

Table 54 governs the loop bandwidth during lock acquisition and table 54 further governs the lock time 25 provided by the decoder. A relationship exists between the loop bandwidth and the lock time. The relationship is characterized and stored in the codeplug for use by the decoder. The following example uses the above frequencies for table 54.

	ΔF	BW	LOCK TIME
5	F1-F2	330 Hz	10mS
	F2-F3	330 Hz	10mS
	F3-F1	660 Hz	10mS
10	F1-F2	570 Hz	5mS
	F1-F2	75 Hz	25mS
	FS-F1	130 Hz	10mS
	FS-F2	330 Hz	10mS
	FS-F3	570 Hz	10mS

- 15 The first three rows show progression from F1 - F3 and back to F1, much like a scanning receiver would operate while scanning channels F1, F2, and F3. The values provide for maintaining a constant lock time independent of the distance in MHz of the frequencies. In order to provide
- 20 for switching from F1 to F2 or from F2 to F3 with a 10 mS lock time, a 330 Hz bandwidth is used for the loop filter. However, when switching from F3 to F1, a frequency jump twice as far as the prior two, the bandwidth is widened to 660 Hz in order to maintain the constant 10 mS lock time.
- 25 The fourth and fifth rows show changing the bandwidth in order to provide for faster or slower lock times respectively. These rows may be used in response to commands within the paging signal causing the pager to switch from F1 to F2. The final three rows show starting
- 30 from a starting frequency FS and bandwidth required to lock on to F1 through F3 respectively in 10 mS. The starting frequency, FS is indicative of the free running frequency of the VCO when it is initially powered on. Thus these rows are used when power is initially applied to the
- 35 receiver which corresponds to the pager being brought out of the battery saving state.

Figure 2 shows a flowchart of a decoder operating in accordance with the present invention. The flowchart begins in step 70 with the receiver in the battery save state, thereby disabled. Step 70 is executed until it is time to turn the receiver on. Then in step 72 the receiver is activated or turned on, thereby exiting the battery saving state. Then in step 74 the peak valley detector is reset. Step 76 determines the receiver frequency which may be made by one of several known algorithms. One such algorithm is shown in U.S. patent 4,644,347 Feb. 17, 1987 to Lucas et al. which is hereby incorporated by reference. Step 78 determines the loop bandwidth with which to program loop filter 30. For example say from step 76, the determined frequency was F3, since the VCO was just previously enabled, it is free running thus the decoder selects the bandwidth corresponding to FS-F3 from the table above (570 Hz). The divider 30 is then programmed in order to receive frequency F3. Then a delay is executed by the software as determined by the FS-F3 lock time entry in the codeplug (10mS from the above table). Then in step 84, the bandwidth of the loop filter 26 is changed to correspond to the desired bandwidth of frequency F3 (120 Hz from the table above). After the delay of step 82, the peak and valley detector 20 is enabled.

Thereafter the receiver detects valid digitized information and in step 88 the decoder processes the detected signal. Step 90 checks if the frequency is to be changed, which could be in response to a signal received by the receiver. If the frequency is not to be changed, step 92 checks if it is time to turn off the receiver, a decision which may be made after completing reception of a paging signal. If it is not time to turn the receiver off, step 80 is returned to and signal processing continues. If it is time to turn the receiver off, step 94 deactivates the receiver thereby entering the battery save mode and step 70 is executed.

If in step 90, it was decided it was time to change to a new receive frequency, step 74 would be executed. The peak and valley detector would be reset and the next frequency would be determined. If for example, the pager
5 was in the scanning mode, currently receiving F3, and F1 was the next frequency to be scanned, information from the F3-F1 row of the above table would be used in steps 78-86. If for example, the receiver was receiving F1 and detected a paging signal directing the pager to rapidly switch to
10 F2, the receiver would use the 5mS lock time setting from the F1-F2 row of the table above in steps 78-86.

Note that the programmable loop filter draws higher current when operating in the wider bandwidth, so it is generally desirable to use narrower bandwidths when
15 possible. Furthermore, narrower bandwidths provides for reduced phase noise which may be desirable.

Although the invention has been described by way of example, it should be clear that numerous alternate applications of the principles described herein may be
20 implemented while remaining within the scope of the invention which is defined by the following claims.

What is claimed is:

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CLAIMS:

1. A selective call receiver comprising:
- 5 receiving means for receiving and demodulating a selective call signal, said receiving means having a plurality of selectable characteristics and including a phase lock loop (PLL) for programmably generating an injection frequency used to select a receive frequency for receiving
- 10 the selective call signal, said PLL having characteristics of a loop filter having a multiplicity of selectable bandwidths, wherein said plurality of selectable characteristics comprises said multiplicity of selectable bandwidths;
- 15 decoding means for processing the demodulated selective call signal and for programming the frequency of the PLL and for selecting one of the plurality of selectable characteristics of the receiving means in response to the programmed frequency;
- 20 determining means for determining the difference between a first injection frequency corresponding to the first receive frequency and a second injection frequency corresponding to the second receive frequency, the determining means generating a difference signal in response thereof; and
- 25 memory means for storing at least one delta bandwidth signal corresponding to the difference signal, wherein said decoding means selects the bandwidth of the loop filter corresponding to the delta bandwidth signal and switches the PLL from the first to the second injection
- 30 frequency.



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2. The selective call receiver of claim 1 wherein said memory means further stores at least one lock time delay signal, said selective call receiver further comprising:

5 delay means for initiating a timed delay in response to said decoding means switching the PLL from the first to the second injection frequency and for generating a completion signal in response to completion of the timed delay, the timed delay having a time duration corresponding to one of the at least one lock time delay signal associated
10 with the difference signal, and wherein

said decoding means having hitherto programmed the first injection frequency and selected a first bandwidth, programs the second injection frequency, and further selects a second PLL bandwidth in response to the completion signal.

15

3. The selective call receiver of claim 1 wherein said receiving means produces the demodulated selective call signal having DC and AC components and further wherein one of the plurality of selectable characteristics of said receiving means includes:

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detecting means for detecting and removing the DC component; and

25 converting means for digitizing the AC component, thereby generating a digital signal including the selective call signal, for processing by the decoding means, the detecting means being enabled in order to detect the DC component of the demodulated signal, and the selective call receiver further comprises:

30 delay means for initiating a timed delay in response to said decoding means programming the second injection frequency and generating a completion signal in response to completion of the timed delay, the timed delay having a time duration provided to said delay means by said decoding means, wherein

35 said decoding means determines said time duration in response to the second injection frequency and enables the detecting means in response to the completion signal.



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4. The selective call receiver of claim 3 wherein said
memory means further stores at least one lock time delay
signal corresponding to the second injection frequency, and
5 wherein

said decoding means determines said time duration
in response to one of the at least one lock time delay signal
stored within said memory means.

10 5. The selective call receiver of claim 3 further
capable of switching from a first receive frequency to a
second receive frequency wherein

said memory means stores at least one lock time
delay signal corresponding to the difference signal, and
15 wherein

said decoding means, having hitherto programmed the
first injection frequency, disables said detecting means and
programs the second injection frequency, said decoding means
determining said time duration in response to the lock time
20 delay signal, and subsequently enabling said detecting means
in response to the completion signal.



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6. A method of controlling a selective call receiver for receiving radio frequency modulated information, said selective call receiver having a plurality of selectable characteristics and a frequency synthesizer having a phase
- 5 lock loop for selecting a receive frequency, the phase lock loop having characteristics of a loop filter having a multiplicity of selectable bandwidths, the method comprising the step of:
- selecting a first receive frequency;
 - 10 selecting one of the plurality of selectable characteristics in response to the selected first receive frequency;
 - switching from the first receive frequency to a second receive frequency;
 - 15 determining the difference between a first injection frequency corresponding to the first receive frequency and a second injection frequency corresponding to the second receive frequency;
 - generating a difference signal in response thereof;
 - 20 storing at least one delta bandwidth signal corresponding to the difference signal;
 - selecting one of the multiplicity of selectable bandwidths of the loop filter corresponding to the at least one delta bandwidth signal; and
 - 25 switching the phase lock loop from the first to the second injection frequency.
7. The method according to claim 6 wherein the step of storing comprises the step of storing the at least one delta
- 30 bandwidth signal and a lock time delay signal associated with the difference signal, the method further comprising after the step of switching the phase lock loop the steps of:
- initiating a timed delay, the timed delay having a time duration corresponding to the lock time delay signal;
 - 35 generating a completion signal in response to completion of the programmed delay; and



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selecting a second phase lock loop bandwidth in response to the completion signal.

8. The method according to claim 6 further comprising
5 before the step of selecting a first receive frequency the steps of:

receiving a selective call signal having an AC component; and

10 digitizing the AC component to generate a digital signal, the digital signal comprising the radio frequency modulated information; and the method further comprising after the step of switching of the phase lock loop the steps of:

15 initiating a timed delay in response to the switching of the phase lock loop from the first to the second injection frequency; and

generating a completion signal in response to completion of the timed delay.

20 9. The method according to claim 6 wherein said step of storing comprises the step of storing at least one lock time delay signal corresponding to the second injection frequency; and wherein said step of initiating a timed delay comprises the step of initiating a timed delay having a time duration,
25 the time duration determined in response to the at least one lock time delay signal.

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10. An electronic device comprising:

circuit means for generating an operating signal,
said circuit means including a phase lock loop (PLL) for
programmably generating a reference frequency for generating
5 the operating signal, said circuit means further having a
plurality of selectable characteristics;

processor means for processing the operating signal
and for programming the frequency of the PLL and for
selecting one of the plurality of selectable characteristics
10 of the circuit means in response to the programmed frequency,
wherein the PLL has the characteristics of a loop filter
having a multiplicity of selectable bandwidths and the
electronic device further capable of switching from a first
reference frequency to a second reference frequency;

15 determining means for determining the difference
between a first operating frequency corresponding to the
first reference frequency and a second operating frequency
corresponding to the second reference frequency, the
determining means generating a difference signal in response
20 thereof; and

memory means for storing at least one delta
bandwidth signal corresponding to the difference signal,
wherein said processor means selects the bandwidth of the
loop filter corresponding to the delta bandwidth signal and
25 switches the PLL from the first to the second operating
frequencies.

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11. The electronic device of claim 10 further comprising:

delay means for generating a completion signal in response to the completion of a timed delay, wherein

5 said memory means further stores a lock time delay signal associated with the difference signal, and

said processor means having hitherto programmed the first operating frequency and selected a first bandwidth, provides a time duration to the delay means, the time
10 duration determined in response to the lock time delay signal, and the processor means programs the second operating frequency and coincidentally signals the delay means to initiate the timed delay for the time duration, and the processor means further selects a second PLL bandwidth in
15 response to the completion signal.

12. The electronic device of claim 10 wherein said circuit means produces a demodulated signal having DC and AC components and further wherein one of the plurality of
20 selectable characteristics of said circuit means includes:

detecting means for removing the DC component; and
converting means for digitizing the AC component into a digital signal including the operating signal for processing by the decoding means, the detecting means being
25 enabled in order to determine the DC component of the demodulated signal, and the electronic device further comprises:

delay means for generating a completion signal in response to the completion of a timed delay, wherein

30 said processor means signals said delay means to initiate said timed delay for a time duration in response to the programming of the second operating frequency, the time duration determined by the processing means in response to the second operating frequency, and the processing means
35 enables the detecting means in response to the completion signal.

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13. The electronic device of claim 12 wherein
said memory means further stores at least one lock
time delay signal corresponding to the second operating
frequency, and wherein

5 said decoding means determines said time duration
in response to the lock time delay signal.

14. The electronic device of claim 12 further capable
of switching from a first reference frequency to a second
10 reference frequency wherein

said memory means further stores at least one lock
time delay signal corresponding to the difference signal, and
wherein

said processing means, having hitherto programmed
15 the first operating frequency, disables said detecting means,
programs the second operating frequency, and determines said
time duration in response to the lock time delay signal, said
processor means further enables said detecting means in
response to the completion signal.

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