

Semiconductor-on-Insulator Chip Incorporating Strained-Channel Partially-Depleted, Fully-Depleted, and Multiple-Gate Transistors

ABSTRACT OF THE DISCLOSURE

In accordance with a preferred embodiment of the present invention, a silicon-on-insulator (SOI) chip includes a silicon layer of a predetermined thickness overlying an insulator layer. A multiple-gate fully-depleted SOI MOSFET including a strained channel region is formed on a first portion of the silicon layer. A planar SOI MOSFET including a strained channel region formed on another portion of the silicon layer. For example, the planar SOI MOSFET can be a planar fully-depleted SOI (FD-SOI) MOSFET or the planar SOI MOSFET can be a planar partially-depleted SOI (PD-SOI) MOSFET.

FIG. 5