METHOD OF TESTING A SEMICONDUCTOR ON INSULATOR STRUCTURE AND APPLICATION OF SAID TEST TO THE FABRICATION OF SUCH A STRUCTURE

FIELD OF THE INVENTION

The present invention concerns a method of testing and a method of fabricating a semiconductor on insulator type structure comprising successively from its base to its surface a support substrate, a dielectric layer having a thickness of less than 50 nm and a semiconductor layer.

BACKGROUND OF THE INVENTION

In semiconductor on insulator (SeOI) type structures, a buried dielectric layer electrically insulates the semiconductor layer from the support substrate.

If the material of the dielectric layer is silicon dioxide (SiO_2), the buried dielectric layer is generally designated by the acronym BOX derived from the expression Buried OXide.

In partially depleted (PD) SeOI structures, the thickness of the buried dielectric layer is generally greater than 100 nm and is therefore sufficient to ensure the electrical integrity and the quality of said layer.

On the other hand, in fully depleted (FD) SeOI structures, the semiconductor layer and the buried dielectric layer have an ultrathin thickness, i.e. less than 50 nm, possibly as little as around 5 nm.

Such structures are notably intended for the fabrication of transistors, the channel layer being formed in or on the ultrathin semiconductor layer, which is not doped.

Thanks to the ultrathin thickness of the buried dielectric layer and the semiconductor layer, these structures have the advantage of enabling precise control of the channel of the transistor, improving the short channel effect and reducing the variability of the transistor.

The properties of these transistors enable significant reduction of the length of the gate.

Moreover, the ultrathin buried dielectric layer provides improved electrostatic control and the possibility of applying a voltage to the rear face - by means of an electrode arranged on the face of the support substrate opposite the semiconductor layer - for controlling the threshold voltage or adjusting the power/performance trade-off.

In this regard reference may be made to the publications of R. Tsuchiya et al, IEDM Proc., 2007, p. 475 and F. Andrieu et al, VLSI Tech. Proc., 57, 2010.

To be able to apply a voltage to the rear face effectively, the thickness of the buried dielectric layer must be less than 50 nm and preferably 25 nm for transistors based on the fully depleted technology with a size of 28 nm.

Even thinner dielectric layers - down to 5 nm - are expected for future transistor sizes.

However, the very thin buried dielectric layer, which has to withstand a voltage applied to the rear face of the order of a few volts, raises the question of its electrical reliability.

This problem is addressed in the paper by Ishigaki et al, IEEE Trans. Electron. Devices, 58(4), p. 1197, 2011.

An object of the present invention is thus to define a method for measuring the electrical quality of the buried dielectric layer with a view to its application in the Fully Depleted technology.

Another object of the invention is to design a method enabling improvement of the electrical properties of the dielectric layer of a semiconductor on insulator structure intended to be used in the Fully Deleted technology.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention, there is proposed a method of testing a semiconductor on insulator type structure comprising successively from its base to its surface a support substrate, a dielectric layer having a thickness of less than 50 nm and a semiconductor layer, said structure comprising a bonding interface between the support substrate and the dielectric layer or between the dielectric layer and the semiconductor layer or inside the dielectric layer.

Said method is characterized in that it comprises measuring the charge to breakdown Q_{BD} of said dielectric layer and in that information is deduced from said measurement relating to the hydrogen concentration in said layer and/or at the bonding interface.

For measuring the charge to breakdown, at least one capacitor is formed on the semiconductor on insulator structure, the formation of said at least one capacitor comprising the deposition of a gate electrode on the semiconductor layer and the formation of trenches

through the dielectric layer around said gate, and the charge to breakdown is measured for each capacitor.

Another object of the invention concerns a method of determining the temperature and the duration of a heat treatment to be applied to a semiconductor on insulator type structure comprising successively from its base to its surface a support substrate, a dielectric layer having a thickness of less than 50 nm and a semiconductor layer, said fabrication method comprising the following steps:

(a) procuring a donor substrate comprising said semiconductor layer,

(b) forming the dielectric layer on the surface of said semiconductor layer of the donor substrate and/or on the surface of the support substrate,

(c) bonding the donor substrate to the support substrate, the dielectric layer being at the bonding interface,

(d) transferring the semiconductor layer from the donor substrate to the support substrate, so as to form said semiconductor on insulator structure,

(e) applying to said structure a heat treatment at a temperature between 1000°C and 1250°C for a duration between 3 minutes and 100 hours to evacuate hydrogen atoms from the dielectric layer and/or the bonding interface.

Said method is characterized in that said structure is fabricated in accordance with steps (a) to (d), in that the test method as defined above is carried out on said structure, and in that the duration and the temperature of the heat treatment of step (e) are chosen as a function of the measured charge to breakdown so as to obtain after said heat treatment a charge to breakdown greater than or equal to a predetermined threshold.

Another object of the invention concerns a method of fabricating a batch of semiconductor on insulator type structures, each structure comprising successively from its base to its surface a support substrate, a dielectric layer having a thickness of less than 50 nm and a semiconductor layer, characterized in that it comprises the following steps:

- procuring a donor substrate comprising said semiconductor layer,
- forming the dielectric layer on the surface of said semiconductor layer of the donor substrate and/or on the surface of the support substrate,
- bonding the donor substrate to the support substrate, the dielectric layer being at the bonding interface,
- transferring the semiconductor layer from the donor substrate to the support substrate so as to form said semiconductor on insulator structure,
- applying to said structure a heat treatment at a temperature between 1000°C and 1250°C for a duration between 3 minutes and 100 hours to evacuate hydrogen atoms from the dielectric layer and/or from the bonding interface,
- sampling a structure from the batch and carrying out on said structure the test method as defined above to check that the charge to breakdown of said structure is greater than or equal to a predetermined threshold.

Said threshold may be 10 C/cm^2, for example.

The thickness of the semiconductor layer is preferably between 1 and 30 nm.

Moreover, the thickness of the dielectric layer is preferably between 3 and 50 nm, preferably between 10 and 30 nm.

The material of the semiconductor layer is advantageously chosen from silicon, strained silicon (sSi), silicon-germanium (SiGe), strained silicon-germanium (sSiGe), germanium, strained germanium (sGe) and semiconductors from groups III-V.

The dielectric layer may comprise a layer of silicon dioxide, a layer of nitrided silicon dioxide, a layer of silicon oxynitride and/or a stack of layers of silicon dioxide, silicon nitride and/or alumina.

The temperature of the heat treatment is advantageously between 1050 and 1200°C.

The duration of the heat treatment is preferably between 5 minutes and 2 hours.

In one embodiment the heat treatment is carried out in an atmosphere of argon or of a mixture of argon and nitrogen.

Before the application of the heat treatment a protective oxide layer may advantageously be formed on the semiconductor on insulator structure.

Another object concerns a semiconductor on insulator type structure adapted to be fabricated by the method described above that has a charge to breakdown greater than or equal to 10 C/cm^2.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will emerge from the following detailed description with reference to the appended drawings in which:

- Figures 1A to 1D illustrate diagrammatically the fabrication of the semiconductor on insulator structure by the Smart Cut™ method,

- Figure 2 shows the SIMS profile of an SOI structure before the long heat treatment carried out during post-fracture finishing of the SOI,

- Figure 3 is a graph showing the value of the charge to breakdown as a function of the duration and the temperature of said heat treatment,

- Figure 4 is a graph showing the evolution of the charge to breakdown as a function of the heat treatment temperature for a fixed duration of 2 hours,

- Figure 5 shows the SIMS profile of a structure similar to that for which the SIMS profile is shown in figure 3 after application of the heat treatment.

To clarify the illustrations, the various layers are not represented here to their true scale.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1A to 1D illustrate diagrammatically steps of the fabrication of a semiconductor on insulator structure based on the Smart Cut™ method.

Referring to Figure 1A, a donor substrate 1 is procured on which a dielectric layer 2 is formed.

Said donor substrate 1 may be solid, i.e. constituted of a single semiconductor material which is that of the semiconductor layer of the SeOI structure to be formed.

Alternatively (this is not shown), the donor substrate is a composite, i.e. constituted of a stack of at least

two layers of different materials, one of which comprises, at its surface, a semiconductor material intended to form the semiconductor layer.

The material of the semiconductor layer is chosen from silicon (the structure then being referred to as Silicon On Insulator (SOI)), constrained silicon (sSi) (the structure then being referred to as Strained Silicon On Insulator (sSOI)), silicon-germanium (SiGe), strained silicon-germanium (sSiGe), germanium, strained germanium, and semiconductor materials from groups III-V - by "material from groups III-V" is meant an alloy of at least one element from group III and at least one element from group V of the periodic table of the elements.

The application of strain to the semiconductor material and/or an alloy with germanium enables the mobility of the carriers in the semiconductor layer to be increased.

The dielectric layer 2 may be formed by oxidation of the donor substrate 1 if the latter is of silicon; the dielectric layer then comprises silicon dioxide (SiO_2).

Said oxidation may consist of dry oxidation, wet oxidation and/or oxidation by the ISSG (In Situ Steam Generation) technique.

The dielectric layer 2, if it is in SiO_2, may equally result from the deposition of oxide by LPCVD, PECVD or any other deposition technique, such as that obtained with a TEOS type precursor, for example.

However, the material of the dielectric layer is not limited to SiO_2 but may comprise nitrided silicon dioxide (formed for example by plasma nitriding of thermal SiO_2, producing an SiO_xN_y/SiO_2 stack the

thickness and the stoichiometry of which depend on the applications), silicon oxynitride (with the general formula SiO_xN_y), or even a stack of layers of silicon dioxide, silicon nitride (Si_3N_4) and/or alumina (Al_2O_3).

For more details on silicon oxynitride, reference may be made to the paper "Propriétés optiques et électriques de couches minces d'oxynitrure de silicium déposées par pulvérisation cathodique r.f. réactive" by F. Rebib, PhD ["Optical and electrical properties of thin layers of silicon oxynitride deposited by reactive r.f. cathode sputtering"].

In this embodiment, the dielectric layer 2 is intended to constitute the buried dielectric layer in the finished SeOI structure.

In another embodiment (not shown here), the dielectric layer may be formed entirely on the support substrate, the donor substrate then being covered, if necessary, only with a layer of native oxide.

In another embodiment (not shown), a dielectric layer is formed on each of the donor and support substrates so that after bonding of said substrates the assembly of the two layers constitutes the buried dielectric layer.

For a fully depleted SeOI structure, the buried dielectric layer has a thickness between 3 and 50 nm, preferably between 10 and 30 nm.

Referring to figure 1B, atomic species are implanted in the donor substrate 1 through the dielectric layer 2.

The implantation dose and energy are chosen so that the implantation peak, i.e. the area in which most of the species are implanted in the donor substrate 1, is

situated at a depth greater than or equal to the thickness of the semiconductor layer 12 to be transferred onto the support substrate.

During the determination of the implantation depth, account is taken of any finishing treatments that will be applied to the semiconductor layer 12 after fracture, for example with a view to reducing its surface roughness, and which will be liable to reduce its thickness by consumption of material.

At the implantation depth there is formed an area of weakening 11 that delimits the semiconductor layer 12.

To this end a single species (for example hydrogen) may be implanted or a plurality of species (for example helium and hydrogen) implanted simultaneously or successively.

As an alternative to implantation, the atomic species may be introduced into the donor substrate by diffusion from the surface of the donor substrate, for example.

Referring to Figure 1C, the donor substrate 1 implanted in this way is bonded to a support substrate 3 so that the dielectric layer 2 is located at the bonding interface I.

Said support substrate 3 may be solid or composite.

The support substrate 3 essentially has a stiffener function vis à vis the semiconductor layer to be transferred.

The support substrate may comprise at least one of the following materials: monocrystalline silicon, polycrystalline silicon, glass, quartz, metal covered with polycrystalline silicon.

The bonding advantageously consists of molecular adhesion bonding.

Bonding is preferably preceded by a step of cleaning the surfaces of the donor substrate and/or the support substrate to be brought into contact in order to remove any impurities present on the surface.

This cleaning step may also comprise activation of the surface of one or both substrates so as to increase the bonding energy.

Cleaning and activation techniques are well known to the person skilled in the art and will therefore not be described further in the present text.

Bonding is preferably followed by consolidation heat treatment aiming to increase the bonding energy between the two surfaces brought into contact.

Referring to Figure 1D, the donor substrate 1 is fractured in the area 11 of weakening.

To this end, a mechanical, chemical and/or thermal force may be applied for starting and propagating a fracture front over all the surface of the area of weakening.

After fracture, the SeOI structure formed is separated from the support substrate 3, the dielectric layer 2 and the semiconductor layer 12, on the one hand, and the remains of the donor substrate 1, on the other hand.

Said remains (not shown) may advantageously be recycled for later use.

For its part the SeOI structure may be subjected to finishing treatments aiming to heal the semiconductor layer, which may have been damaged by implantation, reduce the roughness of the semiconductor layer linked to fracture, etc.

Such treatments include for example RTA (Rapid Thermal Annealing) or RTP (Rapid Thermal Processing) treatments, which are heat treatments of short duration, i.e. having a duration of less than 2 minutes.

The finishing treatments may also comprise polishing treatments (for example chemical-mechanical polishing (CMP)), etching, etc.

As a general rule, said treatments may lead to reduction of the thickness of the semiconductor layer 12.

In the final SeOI structure, obtained after any finishing treatments, the thickness of the semiconductor layer may be between 1 nm and a few micrometers, preferably between 1 and 50 nm, and more preferably of the order of 12 nm.

In the example shown and described above, the fabrication method used is the Smart Cut™ method, but it goes without saying that this method is not limiting on the invention and that, without departing from the scope of the present invention, another method could be chosen for fabrication of the semiconductor structure by bonding and transfer of the semiconductor layer onto a support substrate.

For example, the method could comprise bonding the unweakened donor substrate to the support substrate and

then thinning the donor substrate until the required thickness of the semiconductor layer is obtained.

On the other hand, the SIMOX process, which involves no bonding but in which post-implantation annealing is effected at a temperature higher than 1250°C, is excluded from the scope of the present invention.

Because of the method of fabricating the SeOI structure, it is possible that hydrogen may have been trapped in the dielectric layer and/or in interface defects, said interface being located, depending on the bonding method chosen, between the dielectric layer and the support substrate or between the dielectric layer and the semiconductor layer, or inside the dielectric layer (in the case of dielectric/dielectric bonding).

Indeed, if hydrogen is implanted in the donor substrate through the dielectric layer, it is liable to damage the dielectric material through collisions between atoms.

Moreover, in so far as bonding is effected between the donor substrate and the support substrate, molecules of water may be trapped at the bonding interface.

Consequently, during heat treatments after bonding (such as consolidation heat treatment, RTA or RTP finishing treatment, etc.), hydrogen atoms (coming from some of the water molecules) on the one hand diffuse into the dielectric layer 2 and on the other hand are trapped at the bonding interface I and in the dielectric layer 2.

These phenomena have been verified by SIMS measurements of the hydrogen concentration C_H (expressed in atoms/cm^3) as a function of the depth p (expressed in nm) of the semiconductor on insulator structure.

Figure 2 shows the SIMS profile of an SOI structure comprising a support substrate 3, a buried silicon dioxide (BOX) layer having a thickness of 25 nm and a silicon layer 12 of 12.5 nm thickness.

SIMS measurement enables measurement of a high hydrogen surface density (expressed in atoms/cm^2) between 5×10^{13} and 5×10^{15} atoms/cm^2 and of the order of 5×10^{14} atoms/cm^2 in the BOX layer 2.

In particular, the Figure 2 curve exhibits a very sharp peak at the level of the bonding interface I, corresponding to a hydrogen concentration C_H of the order of 5×10^{20} atoms/cm^3.

Now, the inventors have demonstrated a link between the charge to breakdown Q_{BD} and the presence of hydrogen at the bonding interface and in the dielectric layer.

The charge to breakdown is a measurement reserved at present to checking gate oxides fabricated for MOS transistors by depositing oxide on an SOI structure and/or by thermal oxidation of the active layer of the SOI structure.

In contrast to the fabrication of the SOI structure which, as described above, involves a bonding step, the fabrication of a gate oxide does not involve any bonding.

For an MOS transistor, the charge to breakdown is representative of the reliability of the gate oxide.

This magnitude is typically measured by forcing the flow of current (or by injecting charge carriers) through the gate oxide at constant voltage.

To this end, capacitors are formed distributed at different locations of the SOI structure.

In a manner known in itself, the formation of a capacitor on an SOI structure typically comprises the deposition of a gate electrode on the active layer and the formation of trenches around the gate to isolate each capacitor from the rest of the structure. Said trenches are therefore formed through the dielectric layer and into the support substrate.

An electrode is also formed on the rear face of the support substrate to force the flow of current through the dielectric layer.

Since measuring the charge to breakdown is electrically destructive, the measurement is carried out on a sample SOI structure taken from a fabrication batch.

The time at which the voltage falls (which corresponds to damage of the oxide) is recorded and, on the basis of the current at said time, it is possible to determine the total charge to breakdown of the oxide.

The charge to breakdown (expressed in C/cm^2) is defined by the equation:

$$Q_{BD}(T_{OX}, A_{OX}, T, V) = \frac{N_{BD}(T_{OX}, A_{OX})}{\xi(V, T)}$$

the critical defect density N_{BD} being defined by the equation:

$$N_{BD}(T_{OX}, A_{OX}) = \frac{T_{OX}}{a_0^3} \exp\left(-\frac{a_0}{T_{OX}} \ln\left(\frac{A_{OX}}{a_0^2}\right)\right)$$

in which A_{OX} is the area of the oxide (expressed in cm^2), T_{OX} is the thickness of the oxide (expressed in nm), ξ is the rate of generation of defects, which depends on the applied electric field (magnitude without units), V is the voltage at the terminals of the oxide and T is the time of breakdown.

The intensity of the current injected is typically between 100 and 300 mA/cm^2.

The inventors have measured the charge to breakdown Q_{BD} of the semiconductor on insulator structure described above by applying it not to a gate oxide but to the buried dielectric layer 2.

In these tests, the size of the capacitor created on the SOI structure is considered to be A_{OX} = 6400 μm^2 and T_{OX} = 25 nm.

For an SOI structure comprising a silicon layer 12 nm thick and a buried oxide layer 25 nm thick, the inventors measured a charge to breakdown Q_{BD} between 1 and 5 C/cm^2, typically of the order of 3 C/cm^2.

Such a value of Q_{BD} is significantly less than that usually measured on a gate oxide.

Indeed, on a thermal oxide 25 nm thick constituting a gate oxide, the values of Q_{BD} are of the order of 10 C/cm^2, and may be as high as 20 C/cm^2.

This difference may be explained by the fact that the fabrication of the SOI structure differs from that of a gate oxide, notably in that it involves a bonding step.

Publications have already produced hypotheses for explaining the degraded charge to breakdown Q_{BD} for gate oxides.

In this regard reference may be made to the papers by WK Meyer and DL Crook, Proc. Int. Reliability Physics Symposium, p. 242 (1983) and S. Holland, IC Chen, TP Ma and C. Hu, IEEE Electron Device Letters, 5, p. 302 (1984).

However, the oxide reliability problems discussed in those papers are specific to the formation of a gate oxide in the CMOS technology.

The inventors have moreover verified that the application to the SeOI structure of a long heat treatment having the effect of eliminating the hydrogen present at the bonding interface and in the dielectric layer enables the charge to breakdown Q_{BD} of the dielectric layer to be significantly increased, up to a level comparable with that obtained for gate oxides.

Such long heat treatment may be applied after the steps of finishing the SOI structure (polishing, etching, etc.) but could equally be carried out after fracture and be followed by the finishing steps mentioned above.

In the present text, "long" means a treatment the duration of which is greater than or equal to 3 minutes, preferably greater than or equal to 5 minutes, as opposed to the RTA and RTP treatments, the duration of which is less than or equal to 2 minutes.

Figure 3 is a graph showing the values of Q_{BD} for the aforementioned capacitors as a function of the duration t (expressed in hours) and the temperature T of the heat treatment.

This graph shows that heat treatment at high temperature enables the value of Q_{BD} to be increased, the dominant factor being the temperature of said heat treatment.

Indeed, even if the heat treatment lasts only about 5 minutes but is carried out at a temperature greater than 1100°C the value of Q_{BD} is increased by a factor of 3.

For example, for an SOI structure in which the silicon layer has a thickness of 12 nm and the oxide layer has a thickness of 25 nm, the final value of Q_{BD} is of the order of 8 C/cm^2 for a treatment of 2 hours duration at 1050°C, of the order of 10 C/cm^2 for a treatment of 2 hours duration at 1100°C, and of the order of 11 C/cm^2 for a treatment of 1 hour duration at 1200°C.

In another example, for an SOI structure in which the silicon layer has a thickness of 12 nm and the dielectric layer a thickness of 10 nm, after heat treatment at 1200°C for 5 minutes a final value of Q_{BD} is measured of up to 15 C/cm^2.

Figure 4 is a graph showing the evolution of the charge to breakdown Q_{BD} as a function of the heat treatment temperature, the duration of said treatment being equal to 2 hours.

Moreover, the fact of extending the length of the heat treatment does not contribute to increasing the value of Q_{BD}.

Given the foregoing, the heat treatment is advantageously applied to the SeOI structure at a temperature of between 1000 and 1250°C, preferably of the order of 1100°C, and for a duration of between 3 minutes and 100 hours, preferably between 5 minutes and 2 hours.

Said heat treatment may be carried out in any appropriate device.

Thus the heat treatment may be carried out in a furnace, for example a furnace from the companies Tokyo Electron (TEL), ASM International or Hitachi Kokusai Electric.

Alternatively, the heat treatment may be carried out in an RTP device in which the heat treatment is extended beyond the usual duration of an RTP treatment.

The heat treatment atmosphere preferably comprises argon, either alone or mixed with nitrogen.

In one form of execution of the method, the SeOI structure is protected, either by encapsulation or by covering the surface of the semiconductor layer, by a protective layer enabling prevention of dissolving of the oxide of the dielectric layer if the atmosphere consists of argon or pitting of the semiconductor layer if the atmosphere contains nitrogen.

Said protective layer is advantageously a layer of oxide formed by thermal oxidation or by deposition.

In this case, the heat treatment atmosphere has no particular function with regard to the treatment of the structure.

Consequently, an even slightly oxidizing atmosphere could be envisaged.

Figure 5 shows the SIMS profile of a structure similar to that for which the SIMS profile is shown in Figure 3 after application of the long heat treatment.

Here, the heat treatment was applied at 1100°C for 2 hours.

The value of Q_{BD} measured after the heat treatment is 10 C/cm^2.

Moreover, the surface density of hydrogen is of the order of 5×10^{13} atoms/cm^2, i.e. approximately 10 times

lower than before the heat treatment (the value of Q_{BD} measured before the heat treatment then being 3 C/cm^2).

It is also seen that the hydrogen concentration is much more homogeneous along the depth of the SOI structure.

In particular, no concentration peak is observed at the bonding interface I, which shows that the hydrogen that had been trapped in the interface defects and in the oxide layer has been eliminated thanks to a diffusion phenomenon.

The charge to breakdown may advantageously be measured on a semiconductor on insulator type structure before or after its heat treatment.

Thus it enables a choice of the heat treatment conditions (temperature, duration) to be applied to achieve a given threshold for all of the wafers obtained from the fabrication method concerned following said heat treatment and the finishing process.

Said threshold may vary according to the applications of the SeOI structure.

Thus, for Flash memories, a charge Q_{BD} of the order of 10 C/cm^2 is desirable.

On the other hand, for other applications the requirements may be lower and a charge Q_{BD} of less than 10 C/cm^2, for example 2 to 4 C/cm^2, may be sufficient.

To determine the parameters of the heat treatment, curves of the type shown in Figure 4 are advantageously used.

Accordingly, if the charge Q_{BD} measured after finishing the SeOI structure has a value of the order of 1 or 2 C/cm^2, heat treatment is carried out at a temperature preferably between 1150 and 1200°C and/or for a duration of between 1 and 2 hours in order to achieve a final charge Q_{BD} of 10 C/cm^2.

If on the other hand the charge Q_{BD} measured after the finishing of the SeOI structure has a value of 4 or 5 C/cm^2, heat treatment is carried out at a temperature preferably between 1100 and 1150°C and/or for a duration between 5 minutes and 1 hour in order to achieve a final charge Q_{BD} of 10 C/cm^2.

The charge to breakdown may also be measured during fabrication of a batch of semiconductor on insulator type structures.

To this end, after the long heat treatment, a structure is sampled from the batch and its charge to breakdown measured in order to check that it indeed has the expected value.

If the charge Q_{BD} has a value less than the expected value, this may mean that the parameters of the method are inappropriate and an analysis may be carried out to identify the reasons for the failure and to remedy it.

CLAIMS

1. Method of testing a semiconductor on insulator type structure comprising successively from its base to its surface a support substrate (3), a dielectric layer (2) having a thickness of less than 50 nm and a semiconductor layer (12), said structure comprising a bonding interface (I) between the support substrate (3) and the dielectric layer (2) or between the dielectric layer (2) and the semiconductor layer (12) or inside the dielectric layer (2), characterized in that it comprises measuring the charge to breakdown (Q_{BD}) of said dielectric layer (2) and in that information is deduced from said measurement relating to the hydrogen concentration in said layer (2) and/or at the bonding interface (I).

2. Method according to Claim 1, characterized in that it comprises, for measuring the charge to breakdown, the formation of at least one capacitor on the semiconductor on insulator structure, the formation of said at least one capacitor comprising the deposition of a gate electrode on the semiconductor layer and the formation of trenches through the dielectric layer around said gate, and in that the charge to breakdown is measured for each capacitor.

3. Method of determining the temperature and the duration of a heat treatment to be applied during the fabrication of a semiconductor on insulator type structure comprising successively from its base to its surface a support substrate (3), a dielectric layer (2) having a thickness of less than 50 nm and a semiconductor layer (12), said fabrication method comprising the following steps:

(a) procuring a donor substrate (1) comprising said semiconductor layer (12),

(b) forming the dielectric layer (2) on the surface of said semiconductor layer (12) of the donor substrate (1) and/or on the surface of the support substrate (3),

(c) bonding the donor substrate (1) to the support substrate (3), the dielectric layer (2) being at the bonding interface (I),

(d) transferring the semiconductor layer (12) from the donor substrate (1) to the support substrate (3), so as to form said semiconductor on insulator structure,

(e) applying to said structure a heat treatment at a temperature between 1000°C and 1250°C for a duration between 3 minutes and 100 hours to evacuate hydrogen atoms from the dielectric layer (2) and/or the bonding interface (I),

said method being **characterized** in that said structure is fabricated in accordance with steps (a) to (d), in that the test method according to either one of Claims 1 or 2 is carried out on said structure, and in that the duration and the temperature of the heat treatment of step (e) are chosen as a function of the measured charge to breakdown (Q_{BD}) so as to obtain after said heat treatment a charge to breakdown (Q_{BD}) greater than or equal to a predetermined threshold.

4. Method of fabricating a batch of semiconductor on insulator type structures, each structure comprising successively from its base to its surface a support substrate (3), a dielectric layer (2) having a thickness of less than 50 nm and a semiconductor layer (12), **characterized** in that it comprises the following steps:

- procuring a donor substrate (1) comprising said semiconductor layer (12),

- forming the dielectric layer (2) on the surface of said semiconductor layer (12) of the donor substrate (1) and/or on the surface of the support substrate (3),
- bonding the donor substrate (1) to the support substrate (3), the dielectric layer (2) being at the bonding interface (I),
- transferring the semiconductor layer (12) from the donor substrate (1) to the support substrate (3) so as to form said semiconductor on insulator structure,
- applying to said structure a heat treatment at a temperature between 1000°C and 1250°C for a duration between 3 minutes and 100 hours to evacuate hydrogen atoms from the dielectric layer (2) and/or from the bonding interface (I),
- sampling a structure from the batch and carrying out on said structure the test method according to either one of Claims 1 or 2 to check that the charge to breakdown (Q_{BD}) of said structure is greater than or equal to a predetermined threshold.

5. Method according to any one of Claims 1 to 4, characterized in that the thickness of the semiconductor layer (12) is between 1 and 30 nm.

6. Method according to any one of Claims 1 to 5, characterized in that the thickness of the dielectric layer (2) is between 3 and 50 nm, preferably between 10 and 30 nm.

7. Method according to any one of Claims 1 to 6, characterized in that the material of the semiconductor layer (12) is chosen from silicon, strained silicon (sSi), silicon-germanium (SiGe), strained silicon-germanium (sSiGe), germanium,

strained germanium (sGe) and semiconductors from groups III-V.

8. Method according to any one of Claims 1 to 7, characterized in that the dielectric layer (2) comprises a layer of silicon dioxide, a layer of nitrided silicon dioxide, a layer of silicon oxynitride and/or a stack of layers of silicon dioxide, silicon nitride and/or alumina.

9. Method according to any one of Claims 1 to 8, characterized in that the temperature of the heat treatment is between 1050 and 1200°C.

10. Method according to any one of Claims 1 to 9, characterized in that the duration of the heat treatment is between 5 minutes and 2 hours.

11. Method according to any one of Claims 1 to 10, characterized in that the heat treatment is carried out in an atmosphere of argon or of a mixture of argon and nitrogen.

12. Method according to any one of Claims 1 to 11, characterized in that before the application of the heat treatment a protective oxide layer is formed on the semiconductor on insulator structure.

13. Semiconductor on insulator type structure adapted to be fabricated by the method according to any one of Claims 4 to 12, **characterized** in that it has a charge to breakdown (Q_{BD}) greater than or equal to 10 C/cm^2.