What Is Claimed Is:

1. A semiconductor device, comprising:

gate electrodes stacked along a direction perpendicular to an upper surface of a substrate in a first region of the substrate, the gate electrodes extending to different lengths in a first direction in a second region of the substrate, and each gate electrode including:

subgate electrodes spaced apart from each other in a second direction perpendicular to the first direction, and

gate connection portions connecting subgate electrodes of a same gate electrode of the gate electrodes to each other in the second region;

channels extending through the gate electrodes perpendicularly to the upper surface of the substrate; and

dummy channels extending through the gate electrodes perpendicularly to the upper surface of the substrate, the dummy channels including first dummy channels in the second region arranged in rows and columns, and second dummy channels in the second region arranged between the first dummy channels in a region including the gate connection portions,

wherein at least some of the second dummy channels pass through the gate connection portions and at least some of the second dummy channels are on at least one side of the gate connection portions in the second direction.

2. The semiconductor device as claimed in claim 1, wherein the second dummy channels are arranged in a different pattern than the first dummy channels.

3. The semiconductor device as claimed in claim 2, wherein the second dummy channels are a plurality of second dummy channels in a single gate connection portion of the gate connection portions.

4. The semiconductor device as claimed in any one of claims 1 to 3, wherein a distance between the gate connection portions and a second dummy channel of the second dummy channels most adjacent to the gate connection portions is smaller than a distance between the gate connection portions and a first dummy channel of the first dummy channels most adjacent to the gate connection portions.

5. The semiconductor device as claimed in any one of claims 1 to 4, wherein:

the gate electrodes include contact regions at edges thereof, respectively, a lower gate electrode of the gate electrodes extending farther in the first direction than an upper gate electrode of the gate electrodes,

the first dummy channels are at a boundary of the contact regions, and

the second dummy channels are in the contact regions.

6. The semiconductor device as claimed in any one of claims 1 to 5, wherein the channels are positioned in the first region.

7. The semiconductor device as claimed in any one of claims 1 to 4, wherein:

the gate electrodes include contact regions at edges thereof, respectively, a lower gate electrode of the gate electrodes extending farther in the first direction than an upper gate electrode of the gate electrodes, and

the semiconductor device further comprises contact plugs connected to the gate electrodes through the contact regions.

8. The semiconductor device as claimed in claim 7, wherein a number of contact plugs in the contact regions including the gate connection portion is smaller than that in the contact regions not including the gate connection portion.

9. The semiconductor device as claimed in claim 7 or claim 8, wherein the contact plugs are shifted in a direction oriented away from the second dummy channels in the contact regions including the gate connection portion.

10. The semiconductor device as claimed in any one of claims 1 to 9, wherein some of the gate electrodes include the gate connection portions provided as a plurality of gate connection portions.

11. The semiconductor device as claimed in any one of claims 1 to 10, wherein a lowermost gate electrode of the gate electrodes is divided into the subgate electrodes by a lower isolation region disposed below the gate connection portions.

12. The semiconductor device as claimed in any one of claims 1 to 11, wherein one or more gate electrodes in an uppermost portion of the stacked gate electrodes are divided into the subgate electrodes by an upper isolation region.

13. A semiconductor device, comprising:

gate electrodes stacked in a direction perpendicular to an upper surface of a substrate in a first region of the substrate, the gate electrodes extending to different lengths in a second region of the substrate, and each gate electrode including:

subgate electrodes spaced apart from each other in a first direction, and

gate connection portions connecting subgate electrodes of a same gate electrode of the gate electrodes to each other in the second region;

channels extending through the gate electrodes perpendicularly to the upper surface of the substrate; and

dummy channels extending perpendicularly to the upper surface of the substrate, the dummy channels passing through the gate connections portions and the subgate electrodes near the gate connection portions on at least one side of the gate connection portions in the first direction.

14. The semiconductor device as claimed in claim 13, wherein the dummy channels are at a higher density in a region including the gate connection portions as compared to a region not including the gate connection portions.

15. The semiconductor device as claimed in claim 13 or claim 14, wherein the dummy channels are at a smaller separation distance in a region including the gate connection portions as compared to a region not including the gate connection portions.

16. A semiconductor device, comprising:

a substrate having a first region and a second region;

gate electrodes spaced apart from each other in a first direction, the gate electrodes being stacked perpendicularly to an upper surface of the substrate in the first region, and extending to different lengths in a second direction perpendicular to the first direction in the second region;

first isolation regions extended in the second direction while passing through the gate electrodes in the first region and the second region, the first isolation regions being spaced apart from each other in a third direction perpendicular to the first direction and the second direction;

a plurality of second isolation regions through the gate electrodes between the first isolation regions, the plurality of second isolation regions being spaced apart from each other in the second direction;

channels extending perpendicularly to an upper surface of the substrate through the gate electrodes in the first region; and

dummy channels extending perpendicularly to the upper surface of the substrate through the gate electrodes, the dummy channels including first dummy channels in the second region arranged in rows and columns and second dummy channels in the second region adjacent to a region in which the second isolation regions are spaced apart from each other,

wherein at least some of the second dummy channels pass through at least some of the gate electrodes between the plurality of second isolation regions.

17. The semiconductor device as claimed in claim 16, further comprising:

an upper isolation region extending in the second direction, and passing through at least one gate electrode including a gate electrode in an uppermost portion among the gate electrodes, between the first isolation region and the second isolation regions; and

a lower isolation region passing through at least one gate electrode including a gate electrode in a lowermost portion among the gate electrodes, in the region in which the second isolation regions are spaced apart from each other.

18. The semiconductor device as claimed in claim 17, further comprising an auxiliary upper isolation region between the second isolation regions in the second direction, and passing through at least one gate electrode including a gate electrode in an uppermost portion among the gate electrodes, in the first region.

19. The semiconductor device as claimed in any one of claims 16 to 18, wherein the second dummy channels are between the second isolation regions.