

SUBSTRATE FOR ELECTRONIC PACKAGING, PIN JIG FIXTURE

FIELD OF THE INVENTION

This invention relates to substrates for electronic packaging including *inter alia* ball grid array packaging (BGA), chip size/scale packaging (CSP) and multi-chip/module packaging (MCP/MCM), and a process of
5 manufacturing therefor. In addition, the invention relates to a fixture for masking purposes, and a process using the fixture for preparing a selectively patterned valve metal surface.

BACKGROUND OF THE INVENTION

Conventional electronic packaging includes a discrete substrate on
10 which one or more integrated circuit chips (ICCs) are mounted on its topside, for example, in the case of BGA, as illustrated and described in US Patent No. 5,355,283 to Marrs et al. The discrete substrate can be of a wide range of materials including *inter alia* aluminum and irrespective of its material, through holes are drilled between its topside and underside. In the case of an
15 aluminum substrate, each hole is initially anodized to create an insulating sleeve prior to the insertion of a metal pin, thereby enabling electrical and thermal communication between its topside and underside.

Depending on the intended complexity of an electronic package, a multi-layer interconnect structure can be interdisposed between the ICCs and

the substrate, for example, as illustrated and described in US Patent No. 5,661,341 to Neftin. Such a multi-layer interconnect structure has one or more aluminum layers, each layer being deposited on a previously prepared topside and typically having a thickness in the order of between about 0.5 μ m
5 and about 20 μ m.

Conventional masking for area selective anodization purposes is a relatively complicated and expensive process including the application and subsequent removal of an inert masking layer using photolithography and deposition techniques, the layer being in the form of a photoresist material, a
10 dense oxide layer, a tantalum metal thin film, and the like.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention, there is provided a substrate for electronic packaging, the substrate comprising a discrete, generally prismatoid, initially electrically conductive valve metal
15 solid body with a pair of opposing major surfaces, said body having one or more original valve metal filled vias substantially perpendicular to said major surfaces, said filled vias being spaced apart and individually electrically isolated by a porous oxidized body portion therearound.

A substrate in accordance with the present invention can be fabricated
20 from suitable valve metal blanks of aluminum, titanium, or tantalum, and preferably *inter alia* Al 5052, Al 5083, Al 1100, Al 1145, and the like. Such a substrate can be readily manufactured to customer requirements in terms of a desired filled via pattern; electrical properties; the relative proportions of the original valve metal filled vias and the porous oxidized body portions;
25 thermo-mechanical properties such as thermal coefficient of expansion (TCE), substrate strength, Young modulus, elasticity; thermal properties such as thermal conductivity coefficient; and other factors. Such a substrate can be manufactured with a minimum filled via diameter of about 25 μ m and a

minimum center to center distance between adjacent filled vias of about 50 μm , thereby affording high miniturization and high frequency operation of electronic packaging.

In accordance with a second aspect of the present invention, there is
5 provided a process for manufacturing a discrete substrate for electronic packaging, the process comprising the steps of:

- 10 (a) providing a discrete, generally prismatoid, initially electrically conductive valve metal, solid blank having a pair of opposing major surfaces, the blank having a plurality of spaced apart generally cylindrical through sections, each through section having end surfaces and extending substantially perpendicular to the pair of opposing major surfaces;
- (b) selectively masking both end surfaces of one or more of the through sections; and
- 15 (c) porously oxidizing the blank whereupon a porous oxidized portion forms around a through section whose both end surfaces are masked thereby retaining the through section as an original metal valve filled via.

A process of manufacturing a discrete substrate for electronic
20 packaging in accordance with the present invention involves a low number of steps and is suitable for large area panel production. During or post anodization, suitable materials can be impregnated into the blank's oxidized portions which typically thicken and therefore require planarization to restore them to their original thickness.

25 The porous anodization can be either one- or two-sided depending on the thickness of the generally cylindrical through sections some of which are to be retained as original valve metal filled vias. Typically, one-sided porous anodization can be applied to a maximum through section thickness of about 150 μm whilst two-sided porous anodization can be applied to a maximum

through section thickness of about 300 μm . One- and two-sided porous anodization can be effected in a conventional manner, for example, as illustrated and described in US Patent No. 5,661,341 to Neftin.

In accordance with a third aspect of the present invention, there is
5 provided a pin jig fixture for mechanically masking a valve metal surface, the pin jig fixture comprising an anodization resistant bed of pins each having a leading end surface for intimate juxtaposition against a portion of the metal surface whereby said portion is masked.

A pin jig fixture in accordance with the present invention enables the
10 simultaneous masking of one or more portions of a valve metal surface by its mechanical clamping thereagainst. Typically, the pins have planar end surfaces which are co-planar, however, a jig pin fixture can have pins of different lengths whereby their end surfaces lie on different parallel planes. The bed of pins can be fabricated from any suitable anodization resistant
15 material including ceramics, valve metals, and the like.

The pin jig fixture can be preferably employed to directly oxidize those non-masked portions immediately surrounding the metal surface portions masked thereby, in which case, the pins are fabricated from valve metal and have electrically conductive end surfaces connectable to a power
20 source. In addition, the pin jig fixture advantageously negates the need for an otherwise redundant portion of a substrate, such portion conventionally being initially used for connection to an electrical source and which is subsequently removed.

In accordance with a fourth aspect of the present invention, there is
25 provided a process for preparing a selectively patterned valve metal surface, the process comprising the steps of:

- (a) providing a pin jig fixture having an anodization resistant bed of pins each having a leading end surface;

- (b) intimately juxtaposing leading end surfaces against a valve metal surface to mask portions thereof; and
- (c) anodizing the masked metal surface.

BRIEF DESCRIPTION OF THE DRAWINGS

5 In order to understand the invention and to see how it may be carried out in practice, preferred embodiments will now be described, by way of non-limiting examples only, with reference to the accompanying drawings, in which:

 Fig. 1 is a pictorial view of a finished discrete aluminum substrate in
10 accordance with a first embodiment of the present invention;

 Fig. 2 is a cross section view of the substrate of Figure 1 along line A-A;

 Fig. 3 is a pictorial view showing the porous oxidization of a blank during the manufacture of the substrate of Figure 1;

15 Figs. 4-6 correspond to Figures 1-3 for a finished discrete aluminum substrate in accordance with a second embodiment of the present invention;

 Figs. 7-9 correspond to Figures 1-3 for a finished discrete aluminum substrate in accordance with a third embodiment of the present invention;

 Figs. 10-12 correspond to Figures 1-3 for a finished discrete aluminum
20 substrate in accordance with a fourth embodiment of the present invention;

 Fig. 13 is a perspective view of a pin jig fixture in accordance with the present invention;

 Fig. 14 is a cross section view of the pin jig fixture of Figure 13 along line E-E; and

25 Fig. 15 is a side view showing the mechanical clamping of a substrate by two pin jig fixtures of Fixture 13.

DETAILED DESCRIPTION OF THE DRAWINGS

With reference now to Figures 1 and 2, a finished discrete aluminum substrate 1 has a prismatoid porously oxidized solid body 2 with opposing major surfaces 3 and 4. The substrate 1 is of uniform thickness h_1 of 100 μm .

- 5 The substrate 1 has an array of aluminum filled vias 6 each having two opposing end surfaces 7 and 8 respectively constituting part of the major surfaces 3 and 4. The filled vias 6 have a minimum diameter of 75 μm at end surface 8 monotonically diverging to a maximum diameter of 150 μm at end surface 7. Adjacent filled vias 6 are spaced apart at a center to center distance
10 of 300 μm .

- Turning now to Figure 3, an aluminum blank 9 undergoes one-sided porous anodization in an anodization bath 11, namely, its entire major surface 3 is masked by a mask 12 whilst portions of its major surface 4 are masked by circular masks 13. The circular masks 13 have a diameter of 150 μm . During
15 anodization (see arrows), the mask 12 and each of the masks 13 ensure a non-oxidized zone constituting an aluminum filled via 6. In addition, due to some unisotropy of the anodization process, the blank 9 is oxidized such that the effectively masked area by a mask 13 is less than its actual area. Also, the blank 9 thickens in the non-masked areas (see dotted lines) which may require
20 planarization after anodization to restore them to their original thickness.

- Turning now to Figures 4-6, a discrete aluminum substrate 16 is similar to the substrate 1 except that it is thicker, namely, of a uniform thickness h_2 of 150 μm . Due to this thickness, an aluminum blank 17 necessarily undergoes two-sided porous anodization by means of pairs of
25 oppositely disposed circular masks 18A and 18B which each effect a barrel shaped aluminum filled via 19.

Turning now to Figures 7-9, a discrete aluminum substrate 21 is similar to the substrate 1 except that it is considerably thicker, namely, of a uniform thickness h_3 of 500 μm . Due to this thickness, an aluminum blank 22

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is formed with frusto-conical shaped recesses 23 atop of which remain through sections 24 of thickness h_4 of 100 μm , each through section 24 having a lower surface 26. Due to this, the aluminum blank 22 can undergo one-sided porous anodization similar to the blank 9 except that cone shaped masks 27 mask the lower surfaces 26 whereby the through sections 24 are retained as aluminum filled vias 28. In this case, anodization might leave small aluminum pockets 29 between adjacent aluminum vias 28, however, the aluminum filled vias 28 are still individually electrically isolated.

Turning now to Figures 10-12, a discrete aluminum substrate 31 is similar to the substrate 21 except that it has thicker aluminum vias 32 of a thickness h_5 of 150 μm , the substrate 31 being from an aluminum blank 33 which undergoes two-sided anodization similar to the blank 17.

Turning now to Figures 13-15, a pin jig fixture 41 has a bed of cone shaped pins 42, each pin 43 having a planar leading end surface 44 for intimate juxtaposition against a metal surface. The pins 43 are made from titanium and have a peripheral titanium oxide surface 46 and an inner titanium core 47 terminating at the leading end surface 44. The pins 43 can be directly connected to a power source (PS).

A single pin jig fixture 41 can be employed in one-sided porous anodization, for example, to selectively pattern aluminum blanks 9 and 22 in the manufacture of discrete aluminum substrates 1 and 21, respectively. Or a pair of face-to-face pin jig fixtures 41 can be employed in two-sided porous anodization, for example, to selectively pattern aluminum blanks 17 and 33 in the manufacture of discrete aluminum substrates 16 and 31, respectively.

While the invention has been described with respect to a limited number of embodiments, it will be appreciated that many variations, modifications and other applications of the inventions can be made.

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CLAIMS:

1. A substrate for electronic packaging, the substrate comprising a discrete, generally prismatic, initially electrically conductive valve metal solid body with a pair of opposing major surfaces, said solid body having one
5 or more original valve metal filled vias substantially perpendicular to said major surfaces, said filled vias being spaced apart and each individually electrically isolated by a porous oxidized body portion therearound.
2. The substrate according to claim 1 wherein a filled via has a diverging
10 cross section area therealong and a thickness between about 25 μm and about 150 μm .
3. The substrate according to claim 1 wherein a filled via has a barrel shaped cross section area therealong and a thickness between less than about
15 300 μm .
4. The substrate according to any one of claims 1-3 wherein said solid body has a substantially uniform thickness substantially equal to the thickness of a filled via.
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5. The substrate according to any one of claims 1-3 wherein said solid body has recessed portions whose thicknesses correspond to the thickness of a filled via.
- 25 6. The substrate according to claim 5 wherein non-recessed portions of said solid body have thicknesses between about 200 μm and about 10 mm.
7. The substrate according to claim 5 wherein said recessed portions are of substantially frusto-conical shape.

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8. A process for manufacturing a discrete substrate for electronic packaging, the process comprising the steps of:
- 5 (a) providing a discrete, generally prismatoid, initially electrically conductive valve metal blank having a pair of opposing major surfaces, the blank having a plurality of spaced apart generally cylindrical through sections each extending between a pair of opposing end surfaces, the opposing end surfaces being substantially parallel with the pair of opposing major surfaces;
- 10 (b) selectively masking both end surfaces of one or more of the through sections; and
- (c) porously anodizing the substrate whereupon a porous oxidized portion forms around a through section whose both end surfaces are masked thereby retaining the through section as an
- 15 original metal valve filled via.
9. The process according to claim 8 wherein the substrate undergoes one-sided porous anodization limited up to a through section thickness of about 150 μm .
- 20 10. The process according to claim 8 wherein the substrate undergoes two-sided porous anodization limited up to a through section thickness of about 300 μm .
- 25 11. A pin jig fixture for mechanically masking a metal surface, the pin jig fixture comprising an anodization resistant bed of pins each having a leading end surface for intimate juxtaposition against a portion of the metal surface whereby said portion is masked.

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12. The fixture according to claim 11 wherein the leading end surfaces of said bed of pins are substantially co-planar.

13. The fixture according to claim 11 wherein said pins are of different
5 lengths whose leading end surfaces lie on different parallel planes.

14. The fixture according to any one of claims 11-13 adapted for connection to an electrical source and wherein said leading end surfaces are electrically conductive for conducting electrical energy to the metal surface.

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15. The fixture according to claim 14 wherein at least said pins are fabricated from valve metal and have peripheral oxide plated surfaces.

16. A process of preparing a selectively masked valve metal surface, the
15 process comprising the steps of:

- (a) providing a pin jig fixture having an anodization resistant bed of pins each having a leading end surface;
- (b) intimately juxtaposing the leading end surfaces against a valve metal surface to mask portions thereof; and
- 20 (c) anodizing the masked metal surface.

17. The process according to claim 16 wherein the step (c) includes passing electrical current through electrically conductive pins.

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