

CIRCUIT AND METHOD OF SYNCHRONIZING CLOCK SIGNALS

Abstract of the Disclosure

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10 A digital clock circuit (10) generates a high-speed clock (14) and window pulses (58) substantially centered about transitions of the high-speed clock in one quadrant (12) of an integrated circuit (IC) and routes the high-speed clock and window pulses to other quadrants (18, 19, 20) of the IC where a low-speed clock generator develops a low-speed clock signal from the window pulses. A control circuit (130) checks alignment between the high-speed and low-speed clock signals and adjusts first (90) and second (92) shift registers to control the delay in generating the low-speed clock as necessary to maintain alignment. The first shift register controls the falling edge of the low-speed clock signal and the second shift register controls the rising edge of the low-speed clock signal.

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FIG. 1 accompanies this abstract.

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