We claim:

1. A memory device, comprising:

an array of electroentropic storage devices (EESDs), each EESD comprising a dielectric material having a relative permittivity greater than 3.9, wherein each EESD is a storage element in the memory device;

a plurality of address lines arranged in rows to select a row of the EESDs; and

a plurality of data lines arranged in columns to select a column of the EESDs, wherein each EESD is coupled in series between an address line connected to one side of the EESD and a data line connected to an opposing side of the EESD.

2. The memory device of claim 1, wherein there is a spatial separation at each intersection where a data line crosses an address line, and each of the spatial separations is occupied by an EESD coupled in series between the address line and the data line.

3. The memory device of claim 1 or claim 2, wherein the dielectric material comprises a plurality of polymeric molecules.

4. The memory device of claim 3, wherein the polymeric molecules comprise proteins, poly(*p*-xylylene), acrylic acid polymers, methacrylic acid polymers, polyethylene glycol, urethane polymers, epoxy polymers, silicone polymers, terpenoid polymers, naturally occurring resin polymers, polyisocyanates, or combinations thereof.

5. The memory device of claim 3 or claim 4, wherein the dielectric material further comprises an inorganic salt.

6. The memory device of claim 5, wherein the dielectric material further comprises a permittivity increasing material including Y, Ni, Sm, Sc, Tb, Yb, La, Te, Ti, Zr, Ge, Mg, Pb, Hf, Cu, Ta, Nb, Bi, or a combination thereof, which is substantially evenly distributed throughout the material.

7. The memory device of any one of claims 1-6, wherein each of the plurality of address lines and/or the plurality of data lines comprises an electrically insulated metal, a carbonized polymer, conductive carbon, or an electrically conductive polymer.

8. The memory device of any one of claims 1-7, wherein:

the memory device does not include a transistor; or

the memory device includes one or more transistors, and the memory device has a transistor to EESD ratio of less than 1.

9. The memory device of any one of claims 1-8, wherein each EESD has a logic state determined by a voltage applied between the address line and the data line to which the EESD is coupled.

10. The memory device of claim 9, wherein the EESD has an intrinsic capacitance, and the voltage modifies the intrinsic capacitance, optionally wherein the intrinsic capacitance of the EESD remains unchanged when the applied voltage is removed.

11. The memory device of claim 9 or claim 10, wherein:

(i) the EESD has from 2-4096 logic states;

(ii) the EESD has a volume of 0.00001-10000 μm^3;

(iii) the EESD has a density within a range of from 0.01 kb to 1024 TB per cm^3; or

(iv) any combination of (i), (ii), and (iii).

12. The memory device of any one of claims 1-11, wherein the plurality of address lines or the plurality of data lines is disposed on a non-silicon substrate.

13. The memory device of claim 1 having a layered structure, the layered structure comprising:

a first layer comprising the plurality of address lines arranged in rows;

a second layer comprising the plurality of data lines arranged in columns, wherein there are first spatial separations at each intersection where data line of the second layer crosses an address line of the first layer;

the array of EESDs, wherein the EESDs of the array are located in the first spatial separations and each EESD is coupled in series between an address line of the first layer connected to one side of the EESD and data line of the second layer connected to an opposing side of the EESD;

a third layer of address lines arranged in rows crossing the second layer of data lines, wherein there are second spatial separations at each intersection where an address line of the third layer crosses a data line of the second layer; and

a second array of EESDs, wherein each EESD of the second array is a storage element in the memory device, and wherein the EESDs of the second array are located in the second spatial separations and each EESD of the second array is coupled in series between electrode data line of the second layer connected to one side of the EESD and an address line of the third layer connected to an opposing side of the EESD.

14. The memory device of claim 13, further comprising:

a fourth layer of data lines arranged in columns crossing the third layer of address lines, wherein there are third spatial separations at each intersection where a data line of the fourth layer crosses an address line of the third layer; and

a third array of EESDs, wherein each EESD of the third array is a storage element in the memory device, and wherein the EESDs of the third array are located in the third spatial separations and each EESD of the third array is coupled in series between an address line of the third layer connected to one side of the EESD and a data line of the fourth layer connected to an opposing side of the EESD.

15. A method of refreshing a memory device, comprising:

providing an array of entropic energy storage devices (EESDs), wherein each EESD is a storage element in the memory device;

charging an EESD in the array to a voltage *V1*, wherein the voltage *V1* discharges, at least in part, due to leakage over time;

subsequently determining a capacitance *C* of the EESD;

determining, based on the capacitance *C*, the voltage *V1*; and

recharging the EESD to the voltage *V1*.

16. The method of claim 15, wherein determining the capacitance *C* of the EESD comprises:

reading a voltage *V* of the EESD;

applying a perturbing charge *dQ* to the EESD, wherein the perturbing charge *dQ* has a magnitude sufficient to induce a change in the voltage *V* without inducing a change in the capacitance *C*;

subsequently reading a voltage *V′* of the EESD; and

determining the capacitance *C*, where $C = dQ/(V'-V)$.

17. The method of claim 16, wherein the perturbing charge *dQ*:

has a magnitude approximately equal to a magnitude of discharge due to leakage over time; or

has a magnitude within a range of 1×10^{-15} coulombs to 1×10^{-2} coulombs.

18. The method of any one of claims 15-17, wherein determining the initial voltage *V1* prior to leakage comprises comparing the capacitance *C* of the EESD to predetermined capacitance values for the EESD in charged and uncharged states, thereby correlating the capacitance *C* to the voltage *V1*.

19. The method of any one of claims 15-18, wherein recharging the EESD to the voltage *V1* comprises:

selecting a voltage *V2* sufficient to recharge the EESD to the voltage *V1*; and

writing the selected voltage *V2* to the EESD, thereby recharging the EESD to the voltage *V1*.