CLAIMS

1. An integrated circuit for a fluid ejection device comprising a plurality of fluid actuation devices, the integrated circuit comprising:

a plurality of memory cells, each memory cell corresponding to a fluid actuation device;

a select circuit to select fluid actuation devices and memory cells corresponding to the selected fluid actuation devices;

configuration logic to enable or disable access to the plurality of memory cells; and

control logic to either activate the selected fluid actuation devices or access the memory cells corresponding to the selected fluid actuation devices based on a state of the configuration logic.

2. The integrated circuit of claim 1, wherein the select circuit comprises an address decoder to select fluid actuation devices and memory cells corresponding to the selected fluid actuation devices in response to an address.

3. The integrated circuit of claim 1 or 2, wherein the select circuit comprises activation logic to activate the selected fluid actuation devices and the memory cells corresponding to the selected fluid actuation devices based on a data signal and a fire signal.

4. The integrated circuit of any of claims 1-3, further comprising:

a write circuit coupled to the plurality of memory cells.

5. The integrated circuit of any of claims 1-4, wherein the configuration logic comprises a configuration register storing data to enable or disable access to the plurality of memory cells, and

wherein the control logic is to either activate the selected fluid actuation devices or access the memory cells corresponding to the selected fluid actuation devices based on the data stored in the configuration register.

6. The integrated circuit of claim 5, wherein the configuration register stores data to enable write access or read access to the plurality of memory cells.

7. The integrated circuit of claim 5 or 6, further comprising:

a sensor,

wherein the configuration register stores data to enable or disable the sensor.

8. The integrated circuit of any one of claims 1-7, further comprising:

an elongate substrate having a length, a thickness, and a width, the length being at least twenty times the width, wherein on the elongate substrate there is provided:

a plurality of fluid actuation devices arranged in a column along the length of the elongate substrate,

the plurality of memory cells arranged adjacent to the plurality of fluid actuation devices, each memory cell corresponding to a fluid actuation device.

9. The integrated circuit of claim 8, wherein each fluid actuation device of the plurality of fluid actuation devices has a corresponding memory cell.

10. The integrated circuit of claim 8, wherein every other fluid actuation device of the plurality of fluid actuation devices has a corresponding memory cell.

11. The integrated circuit of any of claims 8-10, wherein the plurality of memory cells comprises a single memory cell corresponding to each fluid actuation device.

12. The integrated circuit of any of claims 8-11, wherein the plurality of memory cells are arranged in a plurality of groups, each group including at least two memory cells, and the plurality of groups spaced apart from each other.

13. The integrated circuit of claim 8, wherein the plurality of memory cells comprises at least two memory cells corresponding to each fluid actuation device.

14. The integrated circuit of claim 13, wherein a first memory cell corresponding to each fluid actuation device is arranged in a first bank of memory cells and a second memory cell corresponding to each fluid actuation device is arranged in a second bank of memory cells.

15. The integrated circuit of claim 8, wherein the plurality of memory cells comprises three memory cells corresponding to each fluid actuation device.

16. The integrated circuit of claim 15, wherein the plurality of memory cells are arranged in a plurality of groups, each group including six memory cells, and the plurality of groups spaced apart from each other.

17. The integrated circuit of claim 15 or 16, wherein a first memory cell corresponding to each fluid actuation device is arranged in a first bank of memory cells, a second memory cell corresponding to each fluid actuation device is arranged in a second bank of memory cells, and a third memory cell corresponding to each fluid actuation device is arranged in a third bank of memory cells.

18. The integrated circuit of claim 14 or 17, wherein the fluid control logic is to either eject fluid from the selected fluid actuation devices or access memory cells corresponding to the selected fluid actuation devices and a selected bank of memory cells.

19. The integrated circuit of claim 1, further comprising:

a single interface coupled to each of the plurality of memory cells, the single interface to connect to a single contact of a host print apparatus;

20. The integrated circuit of claim 19, further comprising:

a write circuit coupled to the single interface, the write circuit to write data to the memory cells.

21. The integrated circuit of claim 19 or 20, wherein each memory cell comprises a non-volatile memory cell.

22. The integrated circuit of any of claims 19-21, wherein the single interface comprises a single contact pad.