WHAT IS CLAIMED IS:

1. A processing method of a wafer which has on a front surface thereof a device region with a plurality of devices formed therein and an outer peripheral surplus region surrounding the device region and which has a chamfered portion at an outer periphery thereof, by grinding the wafer at a back surface thereof to thin the wafer to a finish thickness, the processing method comprising:

a trimming step of cutting the wafer along an outer peripheral edge thereof while causing a cutting blade to cut from the front surface of the wafer into the chamfered portion to a depth greater than the finish thickness, so that an annular stepped portion is formed in the outer peripheral surplus region;

a protective member bonding step of, after performing the trimming step, bonding a protective member to a side of the front surface of the wafer;

a laser processing step of, after performing the protective member bonding step, applying, to the annular stepped portion, a laser beam of a wavelength that has transmissivity for the wafer; and

a grinding step of, after performing the laser processing step, ~~of~~ grinding the wafer from the back

surface thereof to thin the wafer to the finish thickness,

wherein,

in the laser processing step, fracture starting points from which the wafer is to be fractured under an external force to be applied by the grinding are formed in the stepped portion, so that fragments of the stepped portion, the fragments being to occur in the grinding step, are to be subdivided, .

~~2. The processing method according to claim 1, wherein~~

the fracture starting points formed in the laser processing step are a plurality of annular modified layers formed along the outer peripheral edge of the wafer, and the annular modified layers are formed concentrically with each other, and .

~~3. The processing method according to claim 2, wherein~~ the annular modified layers formed concentrically with each other along the outer peripheral edge of the wafer have a greater length in a thickness direction of the wafer as the annular modified layers are each located closer to the outer peripheral edge.

2. The processing method according to claim 1, wherein the annular modified layers are continuous.

3. The processing method according to claim 1, wherein the annular modified layers are discontinuous and regions free of any annular modified layer are interposed individually between adjacent continuous modified layers.