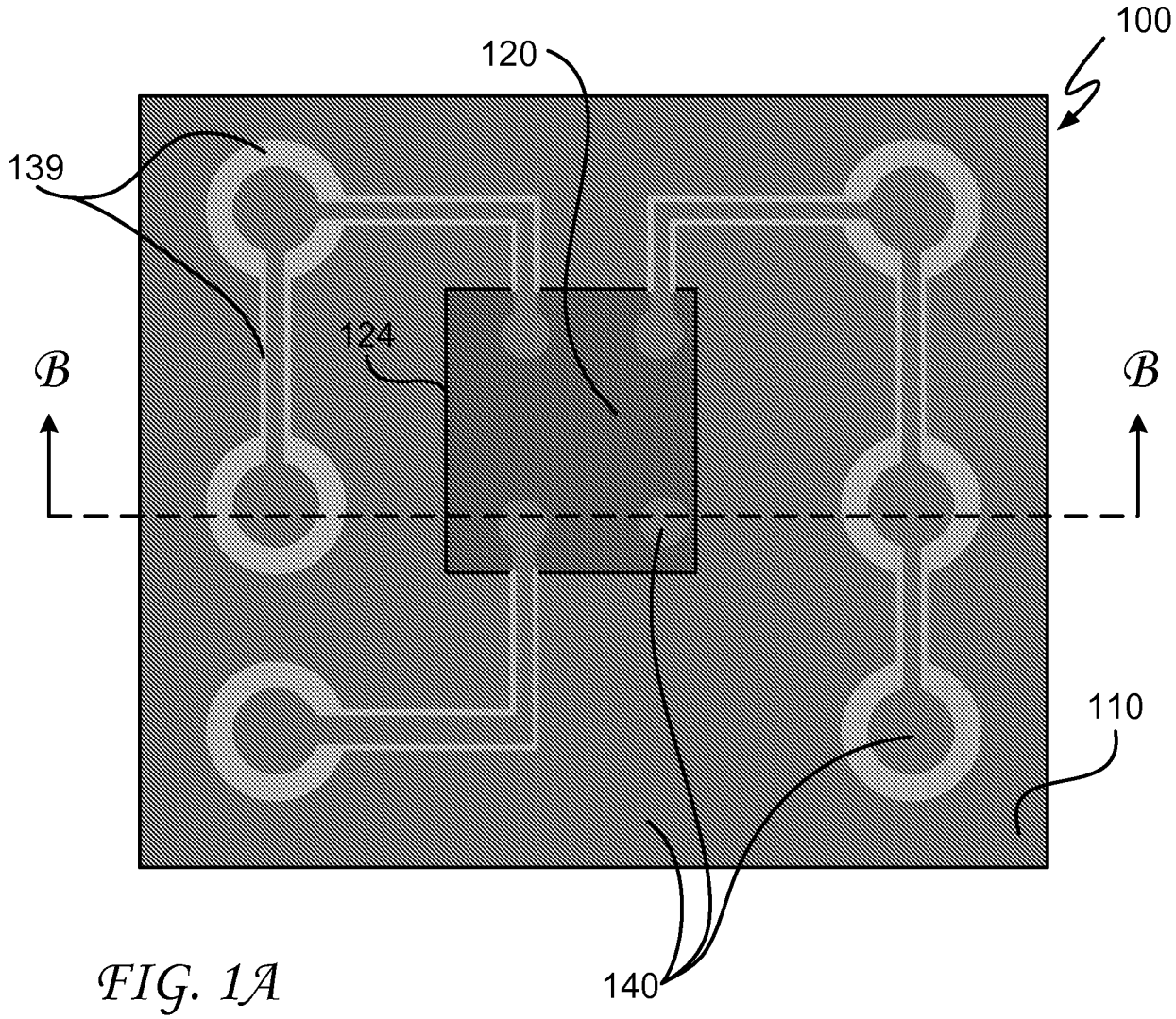

100
120
139
124
B
B
110
140

FIG. 1A

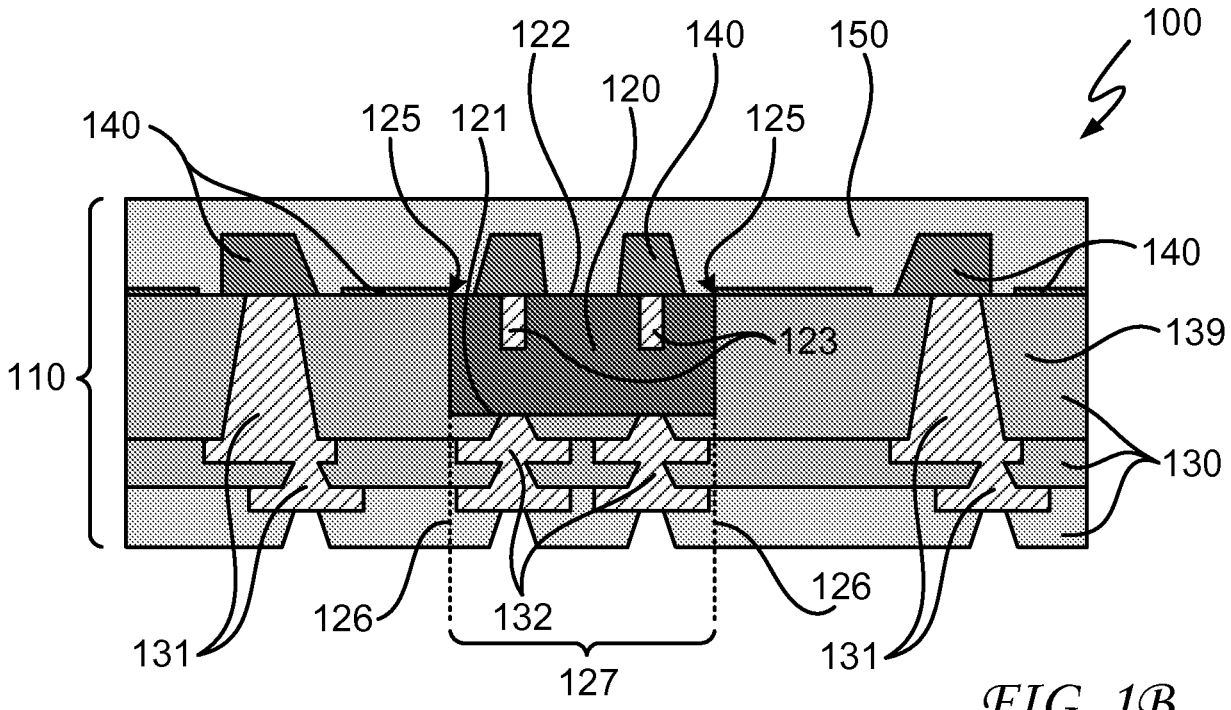

100
122
140
150
120
140
125
121
125
140
139
123
110
130
126
126
132
131
131
127

FIG. 1B

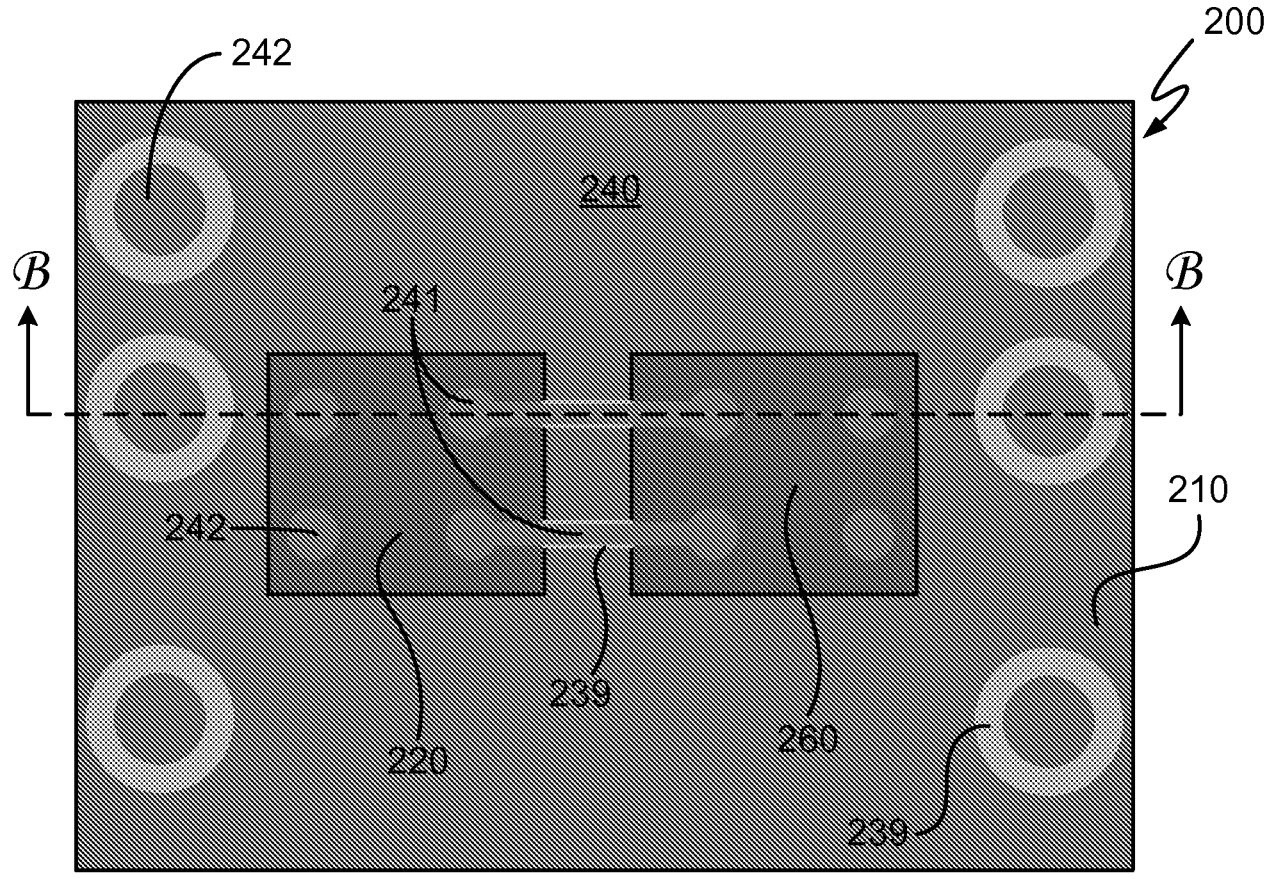

200
242
240
B
B
241
242
210
239
220
260
239

FIG. 2A

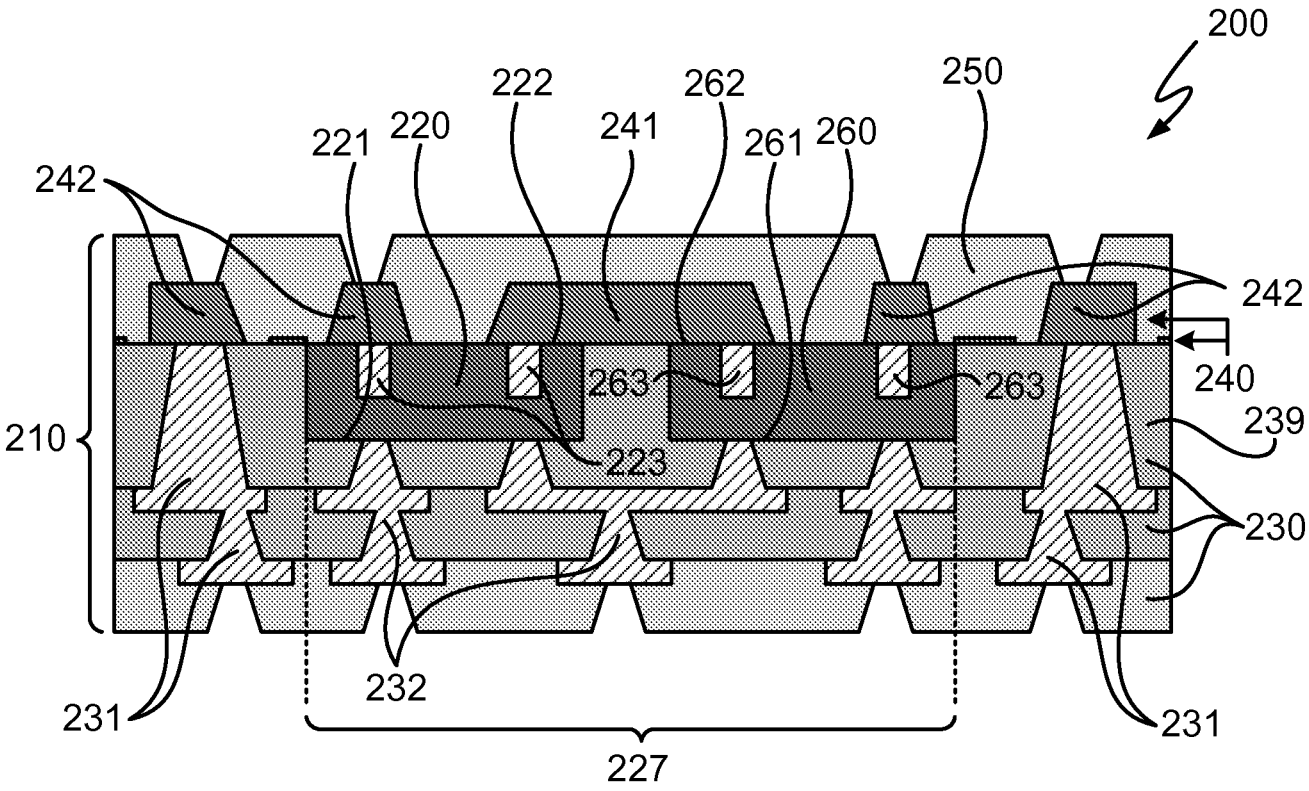

200
222
262
250
221
220
241
261
260
242
242
263
263
240
210
239
223
230
232
231
231
227

FIG. 2B

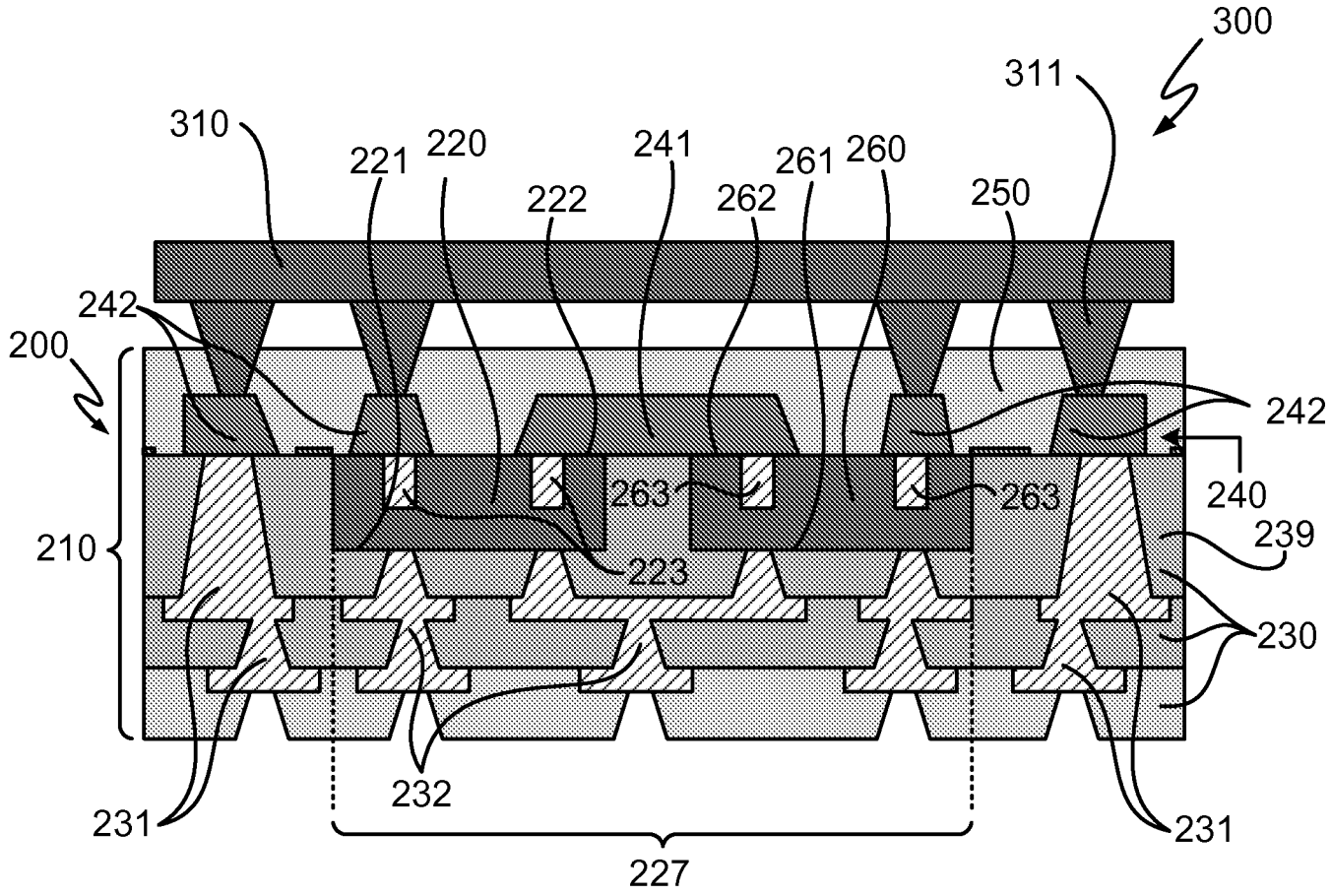

300
311
310
221
220
241
261
260
222
262
250
242
200
242
240
263
263
210
239
223
230
231
232
231
227

FIG. 3

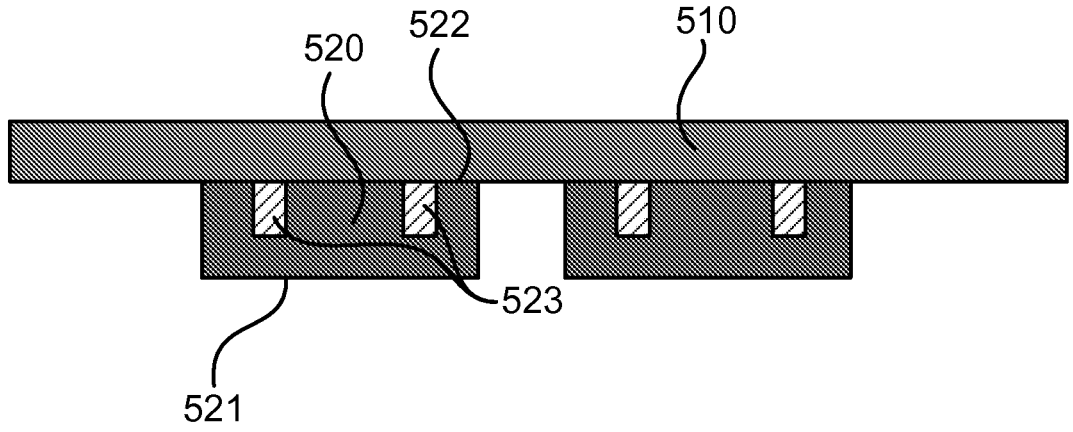

520
522
510
523
521

FIG. 5

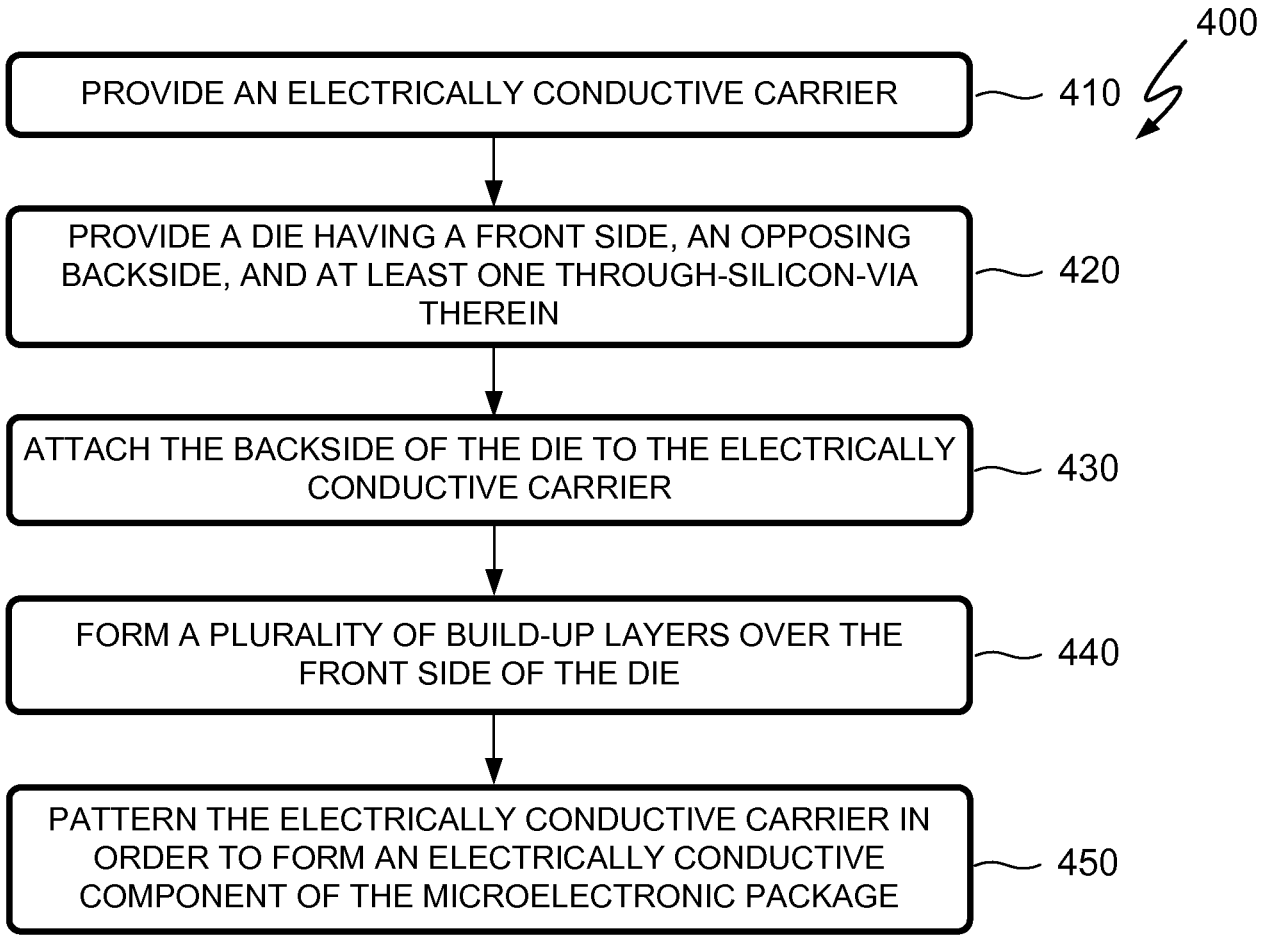

400
PROVIDE AN ELECTRICALLY CONDUCTIVE CARRIER
410
PROVIDE A DIE HAVING A FRONT SIDE, AN OPPOSING BACKSIDE, AND AT LEAST ONE THROUGH-SILICON-VIA THEREIN
420
ATTACH THE BACKSIDE OF THE DIE TO THE ELECTRICALLY CONDUCTIVE CARRIER
430
FORM A PLURALITY OF BUILD-UP LAYERS OVER THE FRONT SIDE OF THE DIE
440
PATTERN THE ELECTRICALLY CONDUCTIVE CARRIER IN ORDER TO FORM AN ELECTRICALLY CONDUCTIVE COMPONENT OF THE MICROELECTRONIC PACKAGE
450

FIG. 4

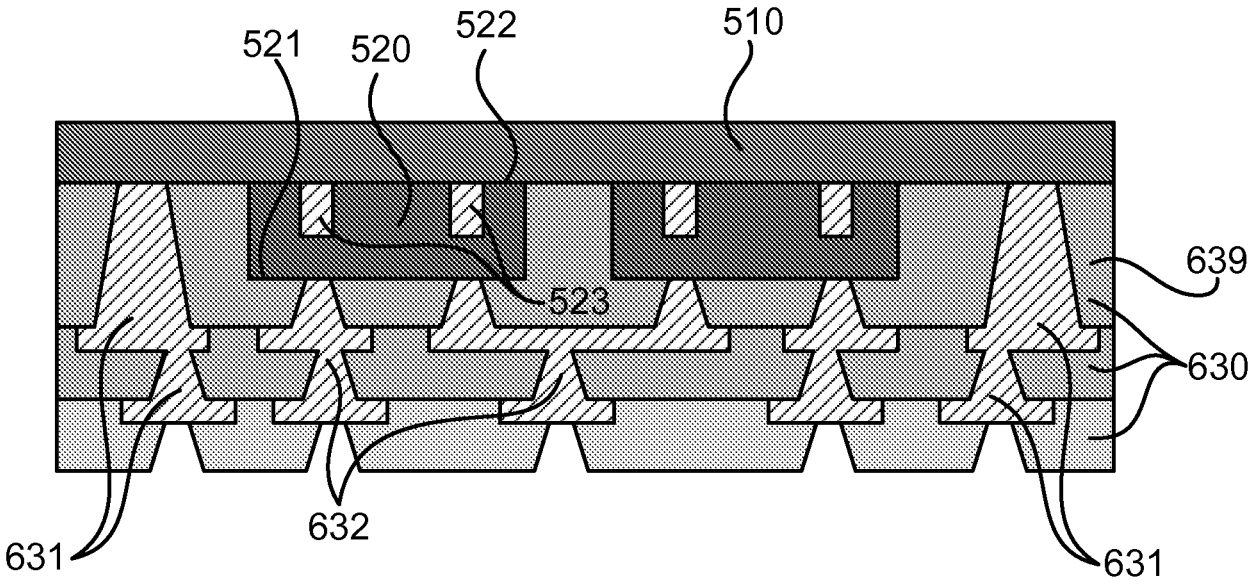

521
520
522
510
523
639
630
631
632
631

FIG. 6