

THREE-DIMENSIONAL STACKING SEMICONDUCTOR ASSEMBLIES WITH NEAR ZERO BOND LINE THICKNESS

TECHNICAL FIELD

[0001] The present technology is directed to semiconductor assemblies having stackable semiconductor packages therein. More particularly, some embodiments of the present technology relate to semiconductor assemblies manufactured by a three-dimensional stacking (3DS) process. In such embodiments, the semiconductor packages are directly, electrically coupled to one another with negligible (e.g., near zero) bond line thickness (BLT) and without using through-silicon vias (TSVs).

BACKGROUND

[0002] Packaged semiconductor dies, including memory chips, microprocessor chips, logic chips and imager chips, typically include a semiconductor die mounted on a substrate and encased in a plastic protective covering. Individual semiconductor die can include functional features, such as memory cells, processor circuits, imager devices and other circuitry, as well as bond pads electrically connected to the functional features. Semiconductor manufacturers continually reduce the size of die packages to fit within the space constraints of electronic devices. One approach for increasing the processing power of a semiconductor package is to vertically stack multiple semiconductor dies on top of one another in a single package. The dies in such vertically-stacked packages can be electrically interconnected by using TSVs, which require multiple processing steps, such as photolithography, to construct.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Many aspects of the present technology can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale. Instead, emphasis is placed on illustrating the principles of the present technology.

[0004] Figure 1 is a schematic cross-sectional view of a semiconductor device package assembly in accordance with the present technology.

[0005] Figures 2A-2J are schematic cross-sectional views illustrating a method of forming a semiconductor device package in accordance with the present technology.

[0006] Figures 3A-3I are schematic cross-sectional views illustrating a method of forming a semiconductor device package in accordance with the present technology.

[0007] Figures 4A-4D are schematic cross-sectional views illustrating a method of processing multiple semiconductor device package assemblies in accordance with the present technology.

[0008] Figures 5A-5D are schematic cross-sectional views illustrating a method of processing multiple semiconductor device package assemblies in accordance with the present technology.

[0009] Figure 6 is a block diagram illustrating a system that incorporates a semiconductor assembly in accordance with the present technology.

DETAILED DESCRIPTION

[0010] Specific details of several embodiments of stacked semiconductor die packages and methods of manufacturing such die packages are described below. The term “semiconductor device” generally refers to a solid-state device that includes one or more semiconductor materials. A semiconductor device can include, for example, a semiconductor substrate or wafer, or a die that is singulated from a wafer or substrate. Throughout the disclosure, semiconductor dies are generally described in the context of semiconductor devices but are not limited thereto.

[0011] The term “semiconductor device package” can refer to an arrangement with one or more semiconductor devices incorporated into a common package. A semiconductor package can include a housing or casing that partially or completely encapsulates at least one semiconductor device. The term “semiconductor device package assembly” can refer to an assembly that includes multiple stacked semiconductor device packages. As used herein, the terms “vertical,” “lateral,” “upper,” and “lower” can refer to relative directions or positions of features in the semiconductor device or package in view of the orientation shown in the Figures. These terms, however, should be construed to include semiconductor devices having other orientations, such as inverted or inclined orientations.

[0012] Figure 1 is a schematic cross-sectional view of a semiconductor device package assembly 100 in accordance with an embodiment of the present technology. As shown, the semiconductor device package assembly 100 includes a base component 101 and multiple

semiconductor device packages 103 stacked on the base component 101. Although the illustrated embodiment shows thirteen (13) separate, stacked semiconductor device packages 103, it will be appreciated that the semiconductor device package assembly 100 can include any suitable number (e.g., 10, 12, 14, 16, 18, etc.) of stacked semiconductor device packages 103 in other embodiments. The semiconductor device package assembly 100 includes an encapsulant material 104 covering the base component 101 and the semiconductor device packages 103. In some embodiments, the encapsulant material 104 can include resin, plastic, silicon, oxide, polymer, or other suitable dielectric materials.

[0013] As shown in Figure 1, the semiconductor device packages 103 are electrically coupled to electric couplers 106 via a metallization structure 108. In some embodiments, the electric couplers 106 can include solder bumps, solder balls, conductive pads, and/or other suitable devices. The metallization structure 108 can include conductive materials, such as metal (e.g., copper), configured into traces, vias, planes, etc., that define a circuitry which electrically connects the semiconductor device packages 103 to the electric couplers 106. By this arrangement, the base component 101 and the semiconductor device packages 103 can be electrically coupled to an external device via the electric couplers 106 and the metallization structure 108.

[0014] The semiconductor device package assembly 100 has a vertically compact design. For example, the base component 101 and the multiple semiconductor device packages 103 are directly stacked together such that a Bond Line Thickness (BLT) between the multiple semiconductor device packages 103 can be zero or near zero. In some embodiments, the BLT between the base component 101 and the adjacent semiconductor device package 103 can also be zero or near zero.

[0015] In some embodiments, the base component 101 can include one or more semiconductor components 102 (e.g., integrated circuitry) therein. The base component 101 can be a circuit board or other type of substrate commonly used in semiconductor device packages or the base component can be a semiconductor device, such as a logic device, memory device, or processor. As shown, the base component 101 has a first side 1011 (e.g., a front/active side) and a second side 1013 (e.g., a back/inactive side) opposite the first side 1011.

[0016] The base component 101 can include a passivation layer 1015 at the first side 1011 of the base component 101. In some embodiments, the passivation layer 1015 can include an

oxide layer, an inert layer (e.g., a layer that is less likely to chemically react with air or corrode), or other suitable protective layers. The passivation layer 1015, for example, can include a protective film. The passivation layer 1015 protects the base component 101. In some embodiments, the base component 101 can be further coupled to an interposer substrate by electric couplers such as solder bumps or solder balls.

[0017] As shown, the base component 101 includes a metallization structure 105 electrically coupled to the semiconductor components 102 in the base component 101. In the illustrated embodiments, the metallization structure 105 can include one or more metallization layers defining traces, vias and/or planes. In some embodiments, the metallization layers can include aluminum (e.g., an aluminum pad), copper, or other suitable metal or conductive materials.

[0018] In the illustrated embodiments, the metallization structure 105 can be formed during a back-end-of-line (BEOL) manufacturing process. The metallization structure 105 can include a contacting area 107 configured to be in contact with the lowermost semiconductor device package 103 (e.g., electrically and physically) when the semiconductor device package 103 is stacked on the base substrate 101.

[0019] In the illustrated embodiments shown in Figure 1, individual semiconductor device packages 103 have a first side 1031 (e.g., a front/active/face side) and a second side 1033 (e.g., a back/inactive side) opposite to the first side 1031. As shown, the individual semiconductor device packages 103 also can include a passivation layer 1035 at the first side 1031 of the semiconductor device package 103 to protect the semiconductor device package 103. In some embodiments, the passivation layer 1035 can include an oxide layer, an inert layer (e.g., a layer that is less likely to chemically react with air or corrode), or other suitable protective layers. The passivation layer 1035 can alternatively be a pre-formed protective film.

[0020] As shown, the individual semiconductor device packages 103 can also include a dielectric layer 1037 at the second side 1033 of the semiconductor device package 103 to protect the semiconductor device package 103. In some embodiments, the dielectric layer 1037 can be a dielectric film.

[0021] The individual semiconductor device packages 103 can also include a metallization structure 109 electrically coupled to one or more semiconductor components 1032 (e.g., integrated circuitry, etc.) in the semiconductor device package 103. The metallization structure

109 can extend through the thickness of the semiconductor device package 103. The metallization structure 109 can include layers of aluminum, copper, or other suitable metals or conductive materials. The metallization structure 109 can be formed during a BEOL manufacturing process and include multiple layers of traces, vias or other electrical features. The metallization structure 109 can have a conductive pad 109a at the first side 1031 and a contacting region 109b at the back side 1033.

[0022] As shown in Figure 1, the base component 101 and the lowermost semiconductor device package 103 are stacked in a “face-to-face” manner such that the first side 1011 (e.g., “face” side) of the base component 101 faces the first side 1031 (e.g., “face” side) of the lowermost semiconductor device package 103. The passivation layer 1035 on the lowermost semiconductor device package 103 can directly contact the passivation layer 1015 on the base component 101 such that there is zero BLT between the lowermost semiconductor device package 103 and the base component 101. However, a very small gap may exist between the lowermost semiconductor device package 103 and the base component 101 such that there is near zero BLT in some embodiments. As also shown in Figure 1, additional semiconductor device packages 103 are stacked above the lowermost semiconductor device package 103 in a “face-to-back” manner. For example, the second side 1033 (“back” side) of one semiconductor device package 103 is directly coupled to the first side 1031 (“face” side) of an adjacent semiconductor device package 103. By this arrangement, the base component 101 and the semiconductor device packages 103 can be quickly stacked. The semiconductor device package assembly 100 can have more device density as more semiconductor device packages 103 are stacked on each other.

[0023] The semiconductor device package assembly 100 further includes metal bumps 111 (or metal pillars) at the first side 1031 of the lowermost semiconductor device package 103. The metal bumps 111 are electrically coupled to the metallization structure 109 of the lowermost semiconductor device package 103 and to the metallization structure 105 of the base component 101 (e.g., at the contacting area 107). The metal bumps 111 can be made from indium or other suitable conductive materials. In some embodiments, the metal bumps 111 can be electrically coupled to the first metallization layer 105a of the base component 101 by an annealing process, such as heating the metal bumps 111 at 100-200 degrees Celsius for a period of time.

[0024] The individual semiconductor device packages 103 have a recess 113 (e.g., a “divot” or “trench”) at their second side 1033, and metal bumps 115 (or metal pillars) can be positioned in the recesses 113. The metal bumps 115 can be electrically coupled to the metallization structures 109 of adjacent semiconductor device packages 103. By this arrangement, the present technology enables the base component 101 to be electrically coupled to the semiconductor device packages 103 without using TSVs in either the base component 101 or the semiconductor device packages 103. In some embodiments, the metal bumps 115 can be electrically coupled to the semiconductor device packages 103 by an annealing process, such as heating the metal bumps 115 to about 100-300 degrees Celsius (e.g., 200°C) for about 50-200 seconds (e.g., 100 seconds).

[0025] In some embodiments, the semiconductor device package assembly 100 can be a memory device in which the semiconductor device packages 103 are memory dies (e.g., DRAM, LPDRAM, SRAM, Flash, etc.). In some embodiments, the base component 101 can be a logic device, processor, and/or another memory device.

[0026] Figures 2A-2J are schematic cross-sectional views of a method for manufacturing a semiconductor device package 203 (e.g., the semiconductor device package 103 described in Figure 1) in accordance with the present technology. Like reference numbers refer to like components throughout Figures 2A-2J. Referring to Figure 2A, at this stage of the method the semiconductor device package 203 has a substrate 2037 with a first side 2031 (e.g., a front/active side) and a second side 2033 (e.g., a back/inactive side) opposite to the first side 2031. The semiconductor device package 203 can have a metallization structure 205 formed during a BEOL manufacturing process including first, second, and third metallization layers 205a, 205b, and 205c in the substrate 2037. In some embodiments, the first metallization layer 205a can include aluminum or another suitable metal or conductive materials. For example, the first metallization layer 205a can be an aluminum pad. The second metallization layer 205b can include copper or another suitable metal or conductive material, and the third metallization layer 205c can include copper or another suitable metal or conductive materials. The metallization structure 205 is electrically coupled to one or more semiconductor components 202 (e.g., integrated circuitry) in the semiconductor device package 203.

[0027] In some embodiments, the semiconductor device package 203 can also have a barrier layer 217 between a portion of the metallization structure 205 and the substrate 2037.

The barrier layer 217, for example, can be adjacent to the second metallization layer 205b. The barrier layer 217 can be made of a metal, such as tantalum, to prevent diffusion into the substrate 2037. For example, the second metallization layer 205b can include copper and the barrier layer 217 can be made of tantalum to inhibit the copper from diffusing into the substrate 2037.

[0028] Figure 2A shows the semiconductor device package 203 after a passivation layer 2035 has been applied to the first side 2031 of the semiconductor device package 203 to protect the semiconductor device package 203. In some embodiments, the passivation layer 2035 can include an oxide layer, an inert layer (e.g., a layer that is less likely to chemically react with air or corrode), other suitable protective layers, or a pre-formed protective film. The semiconductor device package 203 can also include a contacting area 207 on the first metallization layer 205a at the first side 2031.

[0029] Figure 2B shows the semiconductor device package 203 after metal bumps 211 have been formed on the contacting area 207. The metal bumps 211 are electrically coupled to the metallization structure 205 and configured to provide the electrical and mechanical connection to a metallization structure of another semiconductor device package (see e.g., Figure 1) stacked on the semiconductor device package 203. The metal bumps 211 can be made from indium or other suitable conductive materials.

[0030] In some embodiments, the metal bumps 211 can have a vertical dimension VD of approximately 10-20 μm , or more specifically approximately 15 μm . The metal bump 211 can be formed by an electroplating process in which a seed material is deposited on the contact area 207 of the first metallization layer 205a, and then a conductive material is plated onto the seed material to form the metal bumps 211 on the first metallization layer 205a. Alternatively, the metal bumps 211 can be formed by an inkjet process, cold annealing, or other suitable methods.

[0031] Figure 2C shows the semiconductor device package 203 after it has been coupled to a carrier 215 via a bonding layer 213. The carrier 215 is configured to temporarily hold and support the semiconductor device package 203 in the manufacturing process described below with reference to Figures 2D-2J. The carrier 215 can be reusable or disposable, such as a glass carrier, a silicon carrier, or a plastic carrier. In some embodiments, the bonding layer 213 can be a release tape (e.g., gas-sensitive or temperature-sensitive), flowable adhesive, or other suitable materials. The bonding layer 213 can be dissolved using a fluid (gas or liquid) or ablated using a laser to release the semiconductor device package 203 from the carrier 215.

[0032] Figure 2D illustrates the semiconductor device package 203 after the substrate 2037 has been thinned. Referring to Figure 2D, the substrate 2037 can be thinned to a thickness D between a thinned surface 219 and the first side 2031. In some embodiments, the thickness D of the substrate 2037 can range from 5-30 μm , and for example not more than 30 μm , 25 μm , 20 μm , 15 μm , 10 μm or 5 μm .

[0033] By thinning the substrate 2037 to this extent, the metallization structure 205 of the semiconductor device package 203 can be accessed and electrically coupled to other metallization structures or semiconductor components of stacked semiconductor device packages without using TSVs. Generally speaking, to form a TSV in a semiconductor structure, the smallest thickness of the semiconductor substrate can be around 50 μm . This is 200%-1000% thicker than the semiconductor device package 203 and semiconductor device packages 103 (Figure 1) of the present technology. Therefore, the improved method provided by the present technology is advantageous at least because it provides semiconductor device packages with smaller thicknesses (or vertical dimensions) and that can be stacked without forming TSVs. It is particularly beneficial for manufacturing compact semiconductor devices or packages.

[0034] Figure 2E illustrates a stage of the process after a first patterned photo-resist layer 221 has been formed on the second side 2033 (back/inactive side) of the semiconductor device package 203. As shown, the first patterned photo-resist layer 221 has multiple openings 223 (only three are shown in Figure 2E - first, second, and third openings 223a, 223b, and 223c). As shown, the first and third openings 223a, 223c are on opposite sides of the base component 203. The first and third openings 223a, 223c can be used to separate or “singulate” the semiconductor device package 203 in a later stage of the process. The second opening 223b is aligned with at least a portion of the metallization structure 205 in the semiconductor device package 203.

[0035] Figure 2F shows a stage of the process after openings 226 have been formed through the substrate 2037 via the first and third openings 223a, 223c to expose the passivation layer 2035. The openings 226 can be formed by etching the substrate 2037 of the semiconductor device package 203. In the same etching process, a recess 225 (e.g., a divot or trench) can be formed in the substrate 2037 through the second opening 223b (e.g., the second opening 223b extends in the direction toward the first side 2031 of the semiconductor device package 203). The recess 225 can be another opening that exposes the barrier layer 217. As shown, the recess 225 has sloped sidewalls (at both left and right sides of the recess 225, as shown in Figure 2F),

which can facilitate coupling a metal bump of another semiconductor device package to the metallization layers 205. Alternatively, the opening 226 and recess 225 can be formed by laser ablating the substrate 2037 without forming the patterned photo-resist layer 221.

[0036] Figure 2G shows a stage of the process after the first photo-resist layer 221 has been removed and a dielectric layer 227 has been formed on the second side 2033 of the semiconductor device package 203. The dielectric layer 227 can be formed by a chemical vapor deposition (CVD) process, such as a CVD tetraethyl-orthosilicate (TEOS) layer. Alternatively, the dielectric layer 227 can be formed by a spin-on process.

[0037] Figures 2H and 2I show stages of the process after a second patterned photo-resist layer 229 (or a second photo-pattern mask) has been formed on the second side 2033 (back/inactive side) of the semiconductor device package 203. The second patterned photo-resist layer 229 fills the first and third openings 223a, 223c and has an opening 231 aligned with the metal structure 205. Figure 2I shows a stage of the process after the dielectric layer 227 and the barrier layer 217 within the opening 231 have been removed to expose the third metallization layer 205c through an opening 2133. In some embodiments, the barrier layer 217 is not removed. Factors to consider whether to remove the barrier layer 217 include, for example, the types of materials used in the barrier layer 217, the third metallization layer 205c, and the metal bump 211.

[0038] Figure 2J shows a stage of the process after the second photo-resist layer 229 has been removed. The recess 225 has a lateral dimension L_1 that is larger than the lateral dimension L_2 of a metal bump 211 (shown in dotted lines) to be attached to the metal structure 205. As such, a sidewall 225a of the recess 225 and a sidewall portion 227a of the dielectric layer 227 are spaced apart from a sidewall 211a of the metal bump 211. At this stage of the process, the carrier 215 can be removed and one or more semiconductor device packages 203 can be stacked on each other.

[0039] Figures 3A-3I are schematic cross-sectional views illustrating a method of forming a semiconductor device package in accordance with the present technology. Like reference numbers refer to like components throughout Figures 3A-3I. Referring to Figure 3A, a semiconductor device package 300 has a first side 301 (e.g., a front/active side) and a second side 303 (e.g., a back/inactive side) opposite to the first side 301. The semiconductor device package 300 can have a substrate 307 and a metallization structure 305 formed during a BEOL

manufacturing process, including first, second, and third metallization layers 305a, 305b, and 305c. The semiconductor device package 300 can have conductive vias 331 coupled to features in the metallization structure 305. In the illustrated embodiments shown in Figures 3A-3I, the conductive vias 331 are coupled to the second metallization layer 305b. In other embodiments, the conductive vias 331 can be coupled to other metallization layers (e.g., the first metallization layer 305a or the third metallization layer 305c). The metallization layers 305a-c can include conductive traces, pads, conductive planes and/or electrical components (e.g., capacitors, resistors, etc.) that form one or more circuits (e.g., a live circuit, an open circuit, etc.).

[0040] The substrate 307 can be a semiconductor substrate that formed from silicon or other suitable materials, and integrated circuitry can be formed on/in the substrate to form memory devices, logic devices or processors. In the illustrated embodiment, the metallization structure 305 is electrically coupled to a semiconductor component 302 (e.g., integrated circuitry) in the substrate 307. The first metallization layer 305a can include aluminum, or other suitable metal or conductive materials, and be formed into one or more pads. In some embodiments, the second and third metallization layers 305b and 305c can include copper or other suitable metal or conductive materials.

[0041] In some embodiments, the semiconductor device package 300 can have a barrier layer (not shown in Figure 3A, similar to the barrier layer 217 shown in Figure 2A) between a portion of the metallization structure 305 and the substrate 307. The barrier layer can alternatively be adjacent to the second metallization layer 305b. In some embodiments, the barrier layer can be made of a metal, such as tantalum, and the second metallization layer 305b can include copper, such that the tantalum barrier layer inhibits diffusion of the copper into the substrate 307.

[0042] The semiconductor device package 300 can also include a passivation layer (not shown) similar to the passivation layer 2035 shown in Figure 2A at the first side 301 of the semiconductor device package 300. The passivation layer can protect the semiconductor device package 300. In some embodiments, the passivation layer can include an oxide layer, an inert layer (e.g., a layer that is less likely to chemically react with air or corrode), or other suitable protective layers or protective films.

[0043] As shown in Figure 3A, the semiconductor device package 300 includes a center metal bump 308a and side metal bumps 308b (four are shown in Figure 3A) at both sides of the

center metal bump 308a. As shown, the center metal bump 308a has a vertical dimension greater than those of the side metal bumps 308b. For example, the center metal bump 308a can have a vertical dimension VDC of approximately 10-20 μm and the side metal bumps 308b can have a vertical dimension VDS of approximately 5-10 μm . The vertical dimension VDC can be approximately 15 μm , while the vertical dimension VDS can be approximately 7.5 μm . The center metal bump 308a is taller than the side metal bumps 308b so that the center metal bump 308a can be positioned in a cavity of another semiconductor device package when the semiconductor device package 300 is stacked on that semiconductor device package, as described below with reference to Figures 3G and 3H.

[0044] The center and side metal bumps 308a, 308b are electrically coupled to the metallization structure 305 and configured to be in electrical contact with a metallization layer of another semiconductor device package (see e.g., Figure 3H). In some embodiments, the metal bumps 308a, 308b can include an indium bump. In other embodiments, the metal bumps 308a, 308b can include other suitable conductive materials.

[0045] In some embodiments, the center and side metal bumps 308a, 308b can be pillars formed by an electroplating process. For example, the metal bumps 308a, 308b can be formed by having a seed material adjacent to the first metallization layer 305a, and the conductive material can be plated onto the seed material. In other embodiments, the metal bumps 308a, 308b can be formed by an inkjet process or other suitable methods. In some embodiments, the metal bumps 308a, 308b can be cold annealed (e.g., at 200°C).

[0046] Figure 3B shows the semiconductor device package 300 after it has been inverted and coupled to a carrier 315 via an adhesive 316. The carrier 315 is configured to hold and support the semiconductor device package 300 in the manufacturing process described below with reference to Figures 3C-3H. The carrier 315 can be a reusable carrier or a non-reusable carrier made from glass, silicon or plastic. The metal bumps 308a and 308b are embedded in the adhesive 316, which can be a partially cured layer of resin or other suitable material.

[0047] Figure 3C illustrates the semiconductor device package 300 after the substrate 307 has been thinned. Referring to Figure 3C, the semiconductor device package 300 can be thinned such that a depth H_1 between a thinned surface 319 and the first side 2031 of the semiconductor device package 203 is approximately 10 μm . The depth H_1 can range from 5-30 μm , and more specifically the depth H_1 is not more than 30 μm , 25 μm , 20 μm , 15 μm , 10 μm or 5 μm .

[0048] By thinning the substrate 307 to this extent, the metallization structure 305 can be accessed and electrically coupled to other metallization layers or semiconductor components of another semiconductor device package without using a TSV. Generally speaking, to form a TSV in a semiconductor structure, the smallest depth of the semiconductor structure that the semiconductor structure can be thinned is around 50 μm . Therefore, the improved method provided by the present technology is advantageous at least in part because it can manufacture and stack semiconductor device packages with smaller depths (or vertical dimensions) and without the processing steps to form TSVs. It is particularly beneficial for manufacturing compact semiconductor devices or packages.

[0049] Figure 3C also shows the semiconductor package 300 after a coating layer 333 has been formed on the thinned surface 319. The coating layer can be an oxide layer that protects the thinned substrate 307 in subsequent processing, such as photolithographic and other processes discussed below with reference to Figures 3D and 3E.

[0050] Figure 3D illustrates the semiconductor package 300 after a patterned photo-resist layer 321 (or a photo-pattern mask) has been formed on the second side 303 (back/inactive side) of the semiconductor device package 300. As shown, the photo-resist layer 321 has multiple openings 323 (identified as first, second, and third openings 323a, 323b, and 323c). The first and third openings 323a, 323c are formed on opposite sides of the semiconductor device package 300 and can be used to separate or “singulate” the semiconductor device package 300 later in the process. The second opening 323b is at the midline, and more particularly it can be aligned with the center metal bump 308a.

[0051] Figure 3E shows the semiconductor device package 300 after channels 326a, 326c have been formed through the semiconductor device package 300 via the first and third openings 323a, 323c. The channels 326a, 326c can be formed by etching the substrate 307 through the openings 323a, 323c.

[0052] In the same process as forming the channels 326a, 326c, a cavity 326b can be formed through the substrate 307 and a portion of the metallization structure 305 via the second opening 323b. The cavity 326b can extend to the second metallization layer 305b and thereby expose a portion of the second metallization layer 305b.

[0053] Figure 3F shows the semiconductor device package 300 after the photo-resist layer 321 and the coating layer 333 have been removed and a dielectric layer 327 has been formed on

the second side 303 of the semiconductor device package 300. In some embodiments, the dielectric layer 327 can be formed by a chemical vapor deposition (CVD) process, such as a CVD tetraethyl-orthosilicate (TEOS) layer. Alternatively, the dielectric layer 327 can be formed by a spin-on process or applying a pre-formed dielectric film. In some embodiments, a portion of the substrate 307 can also be removed to further thin the substrate. In such embodiments, depth H_2 as indicated in Figure 3F can be smaller than depth H_1 .

[0054] Figure 3G shows the semiconductor device package 300 after portions of the dielectric layer 327 at the bottom of the channels 326a and 326c and the bottom of the cavity 326b have been removed. In some embodiments, the portion of the dielectric layer 327 can be removed by an etching process. As shown in Figure 3G, after removing the portion of the dielectric layer 327 within the cavity 326b, a portion of the second metallization layer 305b is exposed in the cavity 326b.

[0055] Figure 3H shows the semiconductor device package 300 after connecting sites 350 (four are shown in Figure 3H) have been formed on the second side 303 of the semiconductor device package 300. The connecting sites 350 are aligned with the side metal bumps 308b and configured to be coupled to and in contact with side metal bumps (similar to the side metal bumps 308b discussed above) of another semiconductor device package in a stacked arrangement. In some embodiments, the multiple connecting sites 350 can be formed by a masking/etching process. The multiple connecting sites 350 can be made of a metal such as aluminum, titanium, copper, etc.

[0056] Figure 3I shows the semiconductor device package 300 after the carrier 315 has been removed and another semiconductor device package 300a of the same configuration is stacked on the semiconductor device package 300. As shown, the center metal bump 308a of the semiconductor package 300a is aligned and positioned in the cavity 326b of the semiconductor device package 300 and electrically coupled to the second metallization layer 305b of the semiconductor device package 300. The side metal bumps 308b of the semiconductor device package 300a are aligned with and electrically coupled to corresponding connecting sites 350 of the semiconductor device package 300, respectively. In this way, several semiconductor device packages 300 can be stacked on each other with zero or near zero BLT and without forming TSVs through the substrate 307.

[0057] Figures 4A-4D illustrate methods of processing semiconductor device package assemblies 401 similar or identical to the semiconductor device package assembly 100 described with respect to Figure 1, but the semiconductor device packages can also be used in the stacks of die. Each of the semiconductor device package assemblies 401 has a face side 4011 and a back side 4013. In Figure 4A, the semiconductor device package assemblies 401 are carried by a temporary carrier 403. Each of the multiple semiconductor device package assemblies 401 includes a base substrate (e.g., the base component 101 in Figure 1) at the back side 4013 and multiple semiconductor device packages (e.g., the semiconductor device packages 103 or 203) at the face side 4011. In the illustrated embodiments, the back sides 4013 of the semiconductor device package assemblies 401 are coupled to the temporary carrier 403 such that the device package assemblies 401 are spaced apart from each other.

[0058] Figure 4B shows the assembly after the semiconductor device package assemblies 401 have been covered by an encapsulant material 405. In some embodiments, the encapsulant material 405 can include resin, plastic, silicon, oxide, polymer, or other suitable dielectric materials.

[0059] Figure 4C shows the assembly after the temporary carrier 403 has been detached from the semiconductor device package assemblies 401. In Figure 4C, the semiconductor device package assemblies 401 are inverted compared to Figure 4B. An upper portion (e.g., the portion above plane P as indicated) of the assembly shown in Figure 4C can be removed such that metallization structures 4018 of the semiconductor device package assemblies 401 can be exposed.

[0060] Figure 4D shows the assembly after a polymer layer 407 has been formed on the semiconductor device package assemblies 401. The method can include forming a redistribution structure 409 using the polymer layer 407. The redistribution structure 409 is electrically coupled to the metallization layers 4018 in individual semiconductor device package assembly 401. In some embodiments, the redistribution structure 409 can include copper or other suitable conductive material.

[0061] As shown in Figure 4D, multiple connectors 411 can be formed on and electrically coupled to the redistribution structure 409. The connectors 411 are further electrically coupled to the metallization structures of the semiconductor device packages and the base components in the individual semiconductor device package assemblies 401. In some embodiments, the

connectors 411 can be ball grid array (BGA), including a solder ball, a pad, or other suitable connecting devices. The semiconductor device package assemblies 401 can then be “singulated” or separated by cutting through the encapsulant material 405 at the locations indicated by dashed lines shown in Figure 4D.

[0062] Figures 5A-5D illustrate methods of processing semiconductor device package assemblies 501 in accordance with the present technology. In Figure 5A, the semiconductor device package assemblies 501 are carried by a temporary carrier 503, and each of the semiconductor device package assemblies 501 has a face side 5011 and a back side 5013. In this embodiment, the face sides 5011 of the semiconductor device package assemblies 501 are coupled to the temporary carrier 503, as opposed to the back sides 5013 in Figures 4A and 4B. The semiconductor device package assemblies 501 are spaced apart such that they can later be separated during a singulation process.

[0063] Figure 5B shows the assembly after the semiconductor device package assemblies 501 have been covered by an encapsulant material 505. In some embodiments, the encapsulant material 505 can include resin, plastic, silicon, oxide, polymer, or other suitable dielectric materials.

[0064] Figure 5C shows the assembly after the temporary carrier 503 has been detached from the semiconductor device package assemblies 501. In Figure 5C, the semiconductor device package assemblies 501 covered by the encapsulant material 505 are inverted compared to Figure 5B.

[0065] Figure 5D shows the assembly after a polymer layer 507 has been formed on the semiconductor device package assemblies 501. The method can include forming a redistribution structure 509 using the polymer structures 507. The redistribution structure 509 is electrically coupled to the metallization layers (e.g., the metallization structures 105 or 205) in individual semiconductor device package assembly 501. In some embodiments, the redistribution structure 509 can include copper or other suitable conductive material.

[0066] As shown in Figure 5D, multiple connectors 511 can be formed on and electrically coupled to the redistribution structure 509. The connectors 511 are further electrically coupled to the metallization structures of the semiconductor device packages and the base components in the individual semiconductor device package assembly 501. In some embodiments, the connectors 511 can be BGA connectors that include a solder ball, a pad, or other suitable

connecting devices. The semiconductor device package assemblies 501 can then be “singulated” or separated, by cutting through the encapsulant material 505 at the locations indicated by dashed lines shown in Figure 5D.

[0067] Any one of the semiconductor devices having the features described above with reference to Figures 1-5D can be incorporated into any of a myriad of larger and/or more complex systems, a representative example of which is a system 600 shown schematically in Figure 6. The system 600 can include a processor 601, a memory 603 (e.g., SRAM, DRAM, flash, and/or other memory devices), input/output devices 605, and/or other subsystems or components 607. The semiconductor assemblies, devices, and device packages described above with reference to Figures 1-5D can be included in any of the elements shown in Figure 6. The resulting system 600 can be configured to perform any of a wide variety of suitable computing, processing, storage, sensing, imaging, and/or other functions. Accordingly, representative examples of the system 600 include, without limitation, computers and/or other data processors, such as desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants, music players, etc.), tablets, multi-processor systems, processor-based or programmable consumer electronics, network computers, and minicomputers. Additional representative examples of the system 600 include lights, cameras, vehicles, etc. With regard to these and other examples, the system 600 can be housed in a single unit or distributed over multiple interconnected units, e.g., through a communication network. The components of the system 600 can accordingly include local and/or remote memory storage devices and any of a wide variety of suitable computer-readable media.

[0068] This disclosure is not intended to be exhaustive or to limit the present technology to the precise forms disclosed herein. Although specific embodiments are disclosed herein for illustrative purposes, various equivalent modifications are possible without deviating from the present technology, as those of ordinary skill in the relevant art will recognize. In some cases, well-known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments of the present technology. Although steps of methods may be presented herein in a particular order, alternative embodiments may perform the steps in a different order. Similarly, certain aspects of the present technology disclosed in the context of particular embodiments can be combined or eliminated in other embodiments. Furthermore, while advantages associated with certain

embodiments of the present technology may have been disclosed in the context of those embodiments, other embodiments can also exhibit such advantages, and not all embodiments need necessarily exhibit such advantages or other advantages disclosed herein to fall within the scope of the technology. Accordingly, the disclosure and associated technology can encompass other embodiments not expressly shown or described herein.

[0069] Throughout this disclosure, the singular terms “a,” “an,” and “the” include plural referents unless the context clearly indicates otherwise. Similarly, unless the word “or” is expressly limited to mean only a single item exclusive from the other items in reference to a list of two or more items, then the use of “or” in such a list is to be interpreted as including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term “comprising” is used throughout to mean including at least the recited feature(s) such that any greater number of the same feature and/or additional types of other features are not precluded. Reference herein to “one embodiment,” “some embodiment,” or similar formulations means that a particular feature, structure, operation, or characteristic described in connection with the embodiment can be included in at least one embodiment of the present technology. Thus, the appearances of such phrases or formulations herein are not necessarily all referring to the same embodiment. Furthermore, various particular features, structures, operations, or characteristics may be combined in any suitable manner in one or more embodiments.

[0070] From the foregoing, it will be appreciated that specific embodiments of the present technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the scope of the invention. The present technology is not limited except as by the appended claims.