Claims

1. A waveform generator, comprising:
a first voltage stage having:
a first voltage source;
a first switch; and
a second switch, wherein a first terminal of the first voltage source is coupled to a first terminal of the first switch, and a second terminal of the first voltage source is coupled to a first terminal of the second switch, wherein the first terminal of the second switch is coupled to an output node of the waveform generator, and wherein the output node of the waveform generator is coupled to a load;
a second voltage stage having:
a second voltage source;
a third switch; and
a fourth switch, wherein a first terminal of the second voltage source is coupled to a first terminal of the third switch, wherein a second terminal of the second voltage source is coupled to a first terminal of the fourth switch, and wherein the first terminal of the fourth switch is coupled to a first node between second terminals of the first switch and the second switch; and
a current stage coupled to a second node between second terminals of the third switch and the fourth switch, the current stage having:
a current source, wherein the current source comprises a capacitive element and an inductive element coupled in series with the capacitive element; and
a fifth switch coupled to the current source.

2. The waveform generator of claim 1, wherein the first voltage source comprises a capacitive element.

3. The waveform generator of claim 1, wherein each of the first switch, the second switch, the third switch, the fourth switch, and the fifth switch comprises a transistor.

4. The waveform generator of claim 1, wherein the current source is coupled in parallel with the fifth switch.

5. The waveform generator of claim 1, further comprising a third voltage stage having:
a third voltage source;
a sixth switch; and
a seventh switch, wherein a first terminal of the third voltage source is coupled to a first terminal of the sixth switch, wherein a second terminal of the third voltage source is coupled to a first terminal of the seventh switch, and wherein a third node between second terminals of the sixth switch and the seventh switch is coupled to the current stage.

6. The waveform generator of claim 5, wherein:
the first voltage source comprises a first capacitive element;
the second voltage source comprises a second capacitive element;
the third voltage source comprises a third capacitive element; and

the waveform generator further comprises one or more charging circuits configured to charge the first capacitive element, the second capacitive element, and the third capacitive element.

7. The waveform generator of claim 6, wherein the one or more charging circuits are configured to charge the third capacitive element to a lower voltage than the first and second capacitive elements.

8. The waveform generator of claim 1, wherein the load comprises a plasma formed in processing chamber.

9. The waveform generator of claim 1, further comprising a diode coupled between a first terminal and a second terminal of the third switch.

10. The waveform generator of claim 9, wherein the diode comprises a body diode of the third switch.

11. The waveform generator of claim 1, wherein the first switch, the second switch, the third switch, and the fourth switch are configured to couple the second voltage source in series with the first voltage source.

12. A method for waveform generation, comprising:

incorporating, during a first mode of operation, a first voltage source and a second voltage source in an output current path of a waveform generator by controlling multiple switches; and

incorporating, during a second mode of operation, a current source in the output current path by controlling the multiple switches, wherein the current source comprises a capacitive element and an inductive element coupled in series with the capacitive element, wherein the multiple switches comprises:

a first switch;

a second switch, wherein a first terminal of the first voltage source is coupled to a first terminal of the first switch, wherein a second terminal of the first voltage source is coupled to a first terminal of the second switch, wherein the first terminal of the second switch is coupled to an output node of the waveform generator, and wherein the output node of the waveform generator is coupled to a load;

a third switch;

a fourth switch, wherein a first terminal of the second voltage source is coupled to a first terminal of the third switch, a second terminal of the second voltage source is coupled to a first terminal of the fourth switch, and the first terminal of the fourth switch is coupled to a first node between second terminals of the first switch and the second switch; and

a fifth switch coupled in parallel with the current source, the fifth switch being coupled to a second node between second terminals of the third switch and the fourth switch.

13. The method of claim 12, wherein incorporating the first voltage source in the output current path comprises closing the first switch, opening the fifth switch, and closing the third switch.

14. The method of claim 12, wherein incorporating the current source in the output current path comprises closing the first switch, opening the second switch, and opening the fifth switch.

15. The method of claim 12, wherein incorporating the second voltage source in the output current path comprises closing the third switch, and opening the fourth switch.

16. The method of claim 12, further comprising incorporating, during a third mode of operation, a third voltage source in the output current path by controlling the multiple switches, the multiple switches further comprising:

a sixth switch; and

a seventh switch, wherein

a first terminal of the third voltage source is coupled to a first terminal of the sixth switch,

a second terminal of the third voltage source is coupled to a first terminal of the seventh switch, and

a third node between second terminals of the sixth switch and the seventh switch is coupled to the third switch.

17. The method of claim 16, wherein incorporating the third voltage source in the output current path comprises closing the sixth switch, and opening the seventh switch.

18. The method of claim 17, wherein the sixth switch is open and the seventh switch is closed during the first mode of operation and the second mode of operation.

19. The method of claim 16, wherein a voltage associated with the first voltage source or the second voltage source is greater than a voltage associated with the third voltage source.

20. The method of claim 12, wherein the first voltage source comprises a capacitive element.

21. An apparatus for waveform generation, comprising:

a memory; and

one or more processors coupled to the memory, the memory and the one or more processors being configured to:

incorporate, during a first mode of operation, a first voltage source and a second voltage source in an output current path of a waveform generator by controlling multiple switches; and

incorporate, during a second mode of operation, a current source in the output current path by controlling the multiple switches, wherein the current source comprises a capacitive element and an inductive element coupled in series with the capacitive element, wherein the multiple switches comprises:

a first switch;

a second switch, wherein a first terminal of the first voltage source is coupled to a first terminal of the first switch, wherein a second terminal of the first voltage source is coupled to a first terminal of the second switch, wherein the first terminal of the second switch is coupled to an output node of the waveform generator, and wherein the output node of the waveform generator is coupled to a load;

a third switch;

a fourth switch, wherein a first terminal of the second voltage source is coupled to a first terminal of the third switch, a second terminal of the second voltage source is coupled to a first terminal of the fourth switch, and the first terminal of the fourth switch is coupled to a first node between second terminals of the first switch and the second switch; and

a fifth switch coupled in parallel with the current source, the fifth switch being coupled to a second node between second terminals of the third switch and the fourth switch.

22. The apparatus of claim 21, wherein the memory and the one or more processors are configured to incorporate the first voltage source in the output current path by closing the first switch, opening the second switch, and closing the fifth switch.

23. The apparatus of claim 21, wherein the memory and the one or more processors are configured to incorporate the current source in the output current path by closing the first switch, opening the second switch, and opening the fifth switch.

24. A waveform generator, comprising:

a first voltage stage having:

a first voltage source;

a first switch; and

a second switch, wherein a first terminal of the first voltage source is coupled to a first terminal of the first switch, and a second terminal of the first voltage source is coupled to a first terminal of the second switch, wherein the first terminal of the second switch is coupled to an output node of the waveform generator, and wherein the output node of the waveform generator is coupled to a load;

a current stage coupled to a first node between second terminals of the first switch and the second switch, the current stage having:

a current source, wherein the current source comprises a capacitive element and an inductive element coupled in series with the capacitive element; and

a third switch coupled to the current source; and

a second voltage stage having:

a second voltage source;

a fourth switch; and

a fifth switch, wherein a first terminal of the second voltage source is coupled to a first terminal of the fourth switch, wherein a second terminal of the second voltage source is coupled to a first terminal of the fifth switch, and wherein a second node between second terminals of the fourth switch and the fifth switch is coupled to the current stage.