

Sense amplifier for non-volatile semiconductor memory.

FIELD OF INVENTION

This invention relates to an electronic circuit comprising a memory cell for assuming a particular one of two logic states, and sense means for determining the particular logic state of the cell. The invention relates in particular, but not exclusively, to non-volatile semiconductor memories.

BACKGROUND OF INVENTION

An important design consideration for semiconductor memory systems is the support circuitry used to supply sensing of the memory state stored in each of the cells of the memory. Especially important nowadays are non-volatile-memory (NVM) chips, used to store program code, typically of the UV erasable (EPROM), or electrically-erasable (EEPROM), or FLASH type. In a typical conventional EPROM, the cells are connected in rows between horizontal word lines and in columns between vertical bit lines. One current sense amplifier is connected to each bit line adjacent each column of cells. By changing the voltage in a word line, all the cells in the associated row produce in the associated bit line a current, depending on their charge state. The current can be sensed by the sense amplifier connected to that bit line and producing at the output of the amplifier a voltage representative of the programmed state (typically a binary "0"), or the un-programmed state (typically a binary "1") stored in the cell at the intersection of the word and bit lines.

As cells have shrunk in size in order to increase the memory size per chip, the sense currents have also reduced. To increase sensitivity, it is common to sense simultaneously a reference cell which is always in the un-programmed or ON or "1" condition, and at times to use a differential amplifier to which is input both the reference current from the reference cell and the sense current from the memory cell whose state is to be determined (herein referred to as the "sensed cell"). If the sensed cell is in the opposite programmed (OFF) condition, then the differential amplifier outputs one value. When the sensed cell is in the same un-programmed (ON) condition, the differential amplifier outputs the opposite value.

OBJECT OF THE INVENTION

An object of the invention is to furnish an electronic circuit capable of operation over a larger range of supply voltages than in the prior art. Another object of the invention is to create sensing circuitry capable of correct operation over a larger range of supply voltages than in the prior art.

SUMMARY OF THE INVENTION

To this end, the invention provides an electronic circuit as specified in the preamble, characterized in that the circuit comprises bias means operative to control a sensitivity of the sense means dependent on a supply voltage applied to the circuit so as to render the sensitivity higher with a lower supply voltage than with a higher supply voltage. The invention is based on recognizing that a specific relationship exists between programmed and un-programmed cells, the supply voltage available, and the current sensitivity of the sense means required to sense properly a programmed or un-programmed memory cell. The sense means of the invention provides the automatic capability of controlling the sensitivity of the sense amplifier in accordance with the available supply voltage, thus enabling correct circuit operation over a larger range of supply voltages.

In a first embodiment, the sense means comprises a sense load for supplying a sense current to the memory cell for creating a sense voltage, and reference means for creating a reference voltage from a reference current. The sense means further comprises a comparator having inputs coupled to the memory cell and the reference means for providing an output signal indicative of the particular logic state upon comparing the sense voltage to the reference voltage. The bias means is operative to provide a control signal to at least the sense load or the reference means for control of a ratio of the sense current to the reference current. In this embodiment the sensitivity is adapted to the available supply voltage by control of the ratio of sense current to the reference current.

In a further embodiment the reference means comprises a reference cell having a specific logic state, and a reference load coupled to the reference cell via a reference node for supplying the reference current and for creating the reference voltage at the node. The sense means thus utilizes differential sensing of a reference cell and a memory cell. This increases accuracy as the cells are uniform and therefore uniformly susceptible to, e.g., temperature changes, process parameter spread, etc.

Preferably, the reference load and the sense load form an input branch and an output branch, respectively, of a current mirror. The current mirror has a current

amplification factor between the input branch and the output branch. The bias means is operative to control the factor dependent on the supply voltage. This configuration further increases accuracy and its operation is based on a load ratio sensing scheme and in particular on a scalable load ratio sensing scheme. In the typical EPROM memory employing such a sense means, un-programmed cells are ON cells, such as the reference cell, and programmed cells are OFF cells. Each NVM cell has a natural turn-on threshold, V_t , when the state of the cell can be switched from its OFF to its ON state.

In a preferred embodiment of the invention, the reference cell sensing circuit, e.g., the input branch of the current mirror, has a size X and the memory cell sensing circuit, e.g., the output branch of the current mirror, has a size that is a fraction (less than 1) of X in series with an analog control transistor. Preferably, the reference cell sensing circuit comprises A parallel-connected transistors corresponding in size to the size X , where $A \geq 3$, and the memory cell sensing circuit comprises B parallel-connected transistors corresponding in size to the fraction of X , where $B \geq 1$, with the analog control transistor in series with the B transistors. The bias means is connected to the supply voltage and provides to the control electrode of the control transistor a signal that varies in accordance with the supply voltage to control the degree to which the control transistor is ON and thereby provides an effective number, S , of B parallel transistors in the sensing circuit that can vary continuously from $1/B$. This allows the ratio of $A:S$ to vary between $A:1$ and $A:B$ and thus the sensitivity of the sensing circuit as the supply voltage varies from, say, 1-8V.

BRIEF DESCRIPTION OF DRAWINGS

The invention is explained by way of example and in further detail with reference to the accompanying drawing, wherein:

Fig. 1 is a block of a typical semiconductor memory;

Fig. 2 shows typical connections of the semiconductor memory to a differential amplifier;

Fig. 3 is a schematic circuit diagram of a sense amplifier in a traditional non-volatile memory utilizing a fixed load ratio sensing scheme;

Fig. 4 is a schematic circuit diagram of one form of a sense amplifier employing a scalable load ratio sensing scheme in accordance with the invention;

Fig. 5 is a schematic circuit diagram of the sense amplifier of Fig. 4 shown connected to a memory circuit shown only schematically;

Figs. 6 and 7 are graphs illustrating operation of the circuit of the

invention in contrast with that of the prior art;

Fig. 8 is a simple schematic used to help explain the invention.

Throughout the figures, like reference numerals or letters indicate like components.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 shows a typical IC memory comprising two rows of memory cells 10 arranged in three columns, recognizing that most memories of 1K or higher will have many more rows and many more columns. Each memory cell is connected to a word line WL, and to a bit line BL. Each bit line is connected to a sense amplifier SA. Vcc represents the supply voltage. When a word line is asserted, the connected memory cell supplies a current in the connected bit line to the sense amplifier SA. To improve sensitivity, as shown in Fig. 2, the output of the sense amplifier SA is connected to a first input of a differential amplifier 12. The second input is connected to a reference amplifier RA, which in turn is connected to a reference cell RC. Reference cell RC is un-programmed (ON) and establishes a fixed reference current I_{ref} each time a word line is asserted. The fixed reference current (memory cell RC ON) establishes a reference voltage on one input of the differential amplifier. This voltage becomes the amplifier trip point. The sensed current of memory cell 10 is translated into a voltage on the other input of the differential amplifier. This voltage swings above or below the amplifier trip point, depending on the stored memory state (programmed or un-programmed) of the cell, thereby switching the differential amplifier between a logic low ("0") and a logic high ("1") output signal, representative of the memory cell's stored state.

Fig. 3 illustrates a traditional sense amplifier of the load current type with a fixed sensitivity, i.e., a fixed current ratio between the reference NVM cell and the sensed NVM cell. The load 14 for the reference current I_{ref} is supplied by seven p-MOS transistors 15, each having a 10:4 width to length ratio, for example. Each reference transistor (not shown in Fig. 3) is un-programmed which in this instance means it is always ON sinking I_{ref} .

30 The load 16 for the sensed memory cell, in contrast, is formed by a single p-MOS transistor 17 of the same width to length ratio. In this fixed load ratio approach using a fixed load current mirror scheme, the reference portion of the mirror thus consists of 7 p-MOS transistor loads and the multiplier portion consists of one p-MOS load in this example. This results ideally in a fixed sense current, that is, 1:7 or 1/7 of the reference current under

all supply voltages. In general, the smaller the ratio, the greater the current sensitivity.

The problem with the fixed load ratio approach is its fixed sensitivity over the entire supply range. As the supply voltage decreases and approaches the natural threshold V_t of the NVM sensed cell (lower supply voltage range), increased current sensitivity of the sense amplifier is required to sense an un-programmed cell (ON cell). Sensing programmed cells (OFF cells) while operating at the lower voltage range is not a problem since present NVM cell technologies are capable of producing cells with V_t shift (programming mechanism) far in excess of the lower operating supply voltage. As a result, the programmed device remains OFF even at the lower supply voltages. As the supply voltage increases (higher supply voltage range), the supply voltage approaches the programmed V_t of the NVM cell. In this situation, decreased current sensitivity of the sense amplifier is required to sense a programmed cell. Sensing un-programmed cells while operating at the higher supply voltage range is not a problem since the supply voltage is far in excess of that required to turn an un-programmed cell on. This relationship between programmed and un-programmed cells and the supply voltage is what the extended voltage range non-volatile memory sense amplifier of the invention uses to solve the problem.

The extended voltage range NVM sense amplifier of the invention employs a scalable ratio load current sensing scheme. The scaling of the ratio load is a function of the power supply voltage.

Fig. 4 shows one form of the circuit of the invention. In this example, the number of reference load transistors 15 remains the same at seven, but now the multiplier load 20 comprises two controllable or variable load transistors 21 and one fixed load transistor 22 in the multiplier portion of the mirror. The two variable transistors 21 are controlled by a p-MOS transistor 24 that is in series. The transistor 24 in turn is controlled by a bias generator circuit 25 that produces a bias voltage at node 26 that decreases as a percentage of the supply voltage as the supply voltage increases. In the example of Fig. 4, under low voltage supply operation, the high bias cuts OFF transistor 24 thus isolating both transistors 21 and, as a result, the multiplier portion of the mirror is only one p-MOS transistor 22 in size. This results in a current ratio of 1:7, the same as in the fixed ratio load current mirror (Fig. 3). However, under high voltage supply operation, the bias reduces and both transistors 21 are fully ON resulting in a multiplier portion that contains three p-MOS transistors 21, 21, 22. The current ratio is then 3:7 under the higher supply voltage operating condition, thus reducing the current sensitivity of the sense amplifier.

Operation of the system will become clearer with the following

explanation, reference being had to "CMOS Analog Circuit Design" by P.E. Allen, published by Holt, Rinehart & Winston Inc. of Orlando, FL, 1987, which contains a detailed description of a load ratio sensing scheme.

In accordance with general sense amplifier principles, to a first order, the sense amplifier trip point (DC) can be described as follows:

$$V_{t_{trip}} = (M-1/M) (V_{cc}) + V_{t_{ref}}/M \quad (1)$$

where $V_{t_{trip}}$ represents the threshold voltage of the sensed cell, V_{cc} is the power supply voltage, $V_{t_{ref}}$ represents the reference cell threshold voltage, and M represents the ratio of reference cell current to sense cell current (the A:B ratio previously described). Fig. 6 is a graphical representation of Equation 1 using:

$$\begin{aligned} V_{t_{ref}} &= 2.0V, \\ M &= 2, 3, \text{ and } 6, \text{ and} \\ V_{cc} &= 3.0V, 4.0V, \text{ and } 6.0V, \end{aligned}$$

for a typical EPROM of the floating gate type with its I_{DS} -characteristic plotted as current along the ordinate as a function of the EPROM's V_t along the abscissa with V_{cc} as the parameter.

For $M = 2$, the $V_{t_{trip}}$ (represented by V_t for the sensed cell), ranges from 2.5 V at $V_{cc} = 3.0$ V to 4.0 V at $V_{cc} = 6.0$ V for a delta (4.0-2.5) of 1.5 V. For $M = 6$, the $V_{t_{trip}}$ ranges from 2.83 V at $V_{cc} = 3.0$ V to 5.33 V at $V_{cc} = 6.0$ V for a delta of 2.5 V. The significance of the $V_{t_{trip}}$ range can be described as follows; the $V_{t_{trip}}$ at $V_{cc}(\min)$ (3.0 V in the above example) represents the maximum sense cell V_t of an un-programmed cell for a given power supply voltage range, and the $V_{t_{trip}}$ at $V_{cc}(\max)$ (6.0 V in the above example) represents the minimum sense cell V_t of a programmed cell for a given power supply voltage range. The delta voltage between these two numbers represents the "un-usable" range of the sense cell V_t for the specified power supply voltage range. To further illustrate, for $M = 2$, if during non-volatile cell programming, the resultant cell $V_t = 3.5$ V, then at $V_{cc} = 3.0$ V, the cell would be sensed as programmed. At $V_{cc} = 6.0$ V, however, the cell would be sensed as un-programmed.

Two important DC effects should be noted from Fig. 6. First, as M increases from 2 to 6, so does the range of "un-usable" sense cell V_t . This is not a desirable effect since it reduces the usable V_t range of programmed cells ($V_{t_{trip}}$ at $V_{cc}(\max)$ to the maximum programmed cell V_t). Second, as M increases from 2 to 6, so does the delta between the $V_{t_{ref}}$ ($V_{t_{ref}} = 2.0$ V in the above example) and the $V_{t_{trip}}$ at $V_{cc}(\min)$. This a desirable effect since it extends the range of un-programmed cell V_t .

Another important aspect of sense amplifier design is speed of operation. This is controlled by adjusting the ratio of the ratio load current mirror. In general terms, as M increases, the speed of discharge (sensing an un-programmed cell) of the amplifier input increases. This relationship is given in the following expression:

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$$dt = (M/M-1) (C/I)dv \quad (2)$$

where dv is the change in voltage on the amplifier input required for sensing, C is the internal capacitance on the amplifier input, I is the reference current and M is the current mirror ratio. Conversely, as M increases, the speed of charging of the amplifier input decreases. This relationship is given in the following expression:

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$$dt = (M) (C/I) |dv| \quad (3)$$

where dv is the change in voltage on the amplifier input required for sensing, C is the internal capacitance on the amplifier input, I is the reference current and M is the current mirror ratio. Therefore, Equations 2 and 3 place the lower and upper constraints on M, respectively.

15 Equations (2) and (3) are derived from Fig. 8, which is a simplified view of a ratio load current mirror which converts current to voltage to drive an amplifier.

The scalable ratio load current sensing scheme of the invention allows for the adjustment of M as a function of the power supply voltage. This scalability allows for design optimization over a wider power supply voltage range. Fig. 7 illustrates the design improvement. Shown in Fig. 7 for convenience are the three fixed ratios M = 2, M = 3, and M = 6 previously shown in Fig. 6. In addition, the scalable or variable ratio is shown at 30. For the variable ratio, at a power supply voltage of 3.0 V, M = 6; at a power supply voltage of 6.0 V, M = 2.

25 Two important improvements have occurred. First, at low power supply operating voltages (3.0 V in the above example), the speed of the sense amplifier is optimized since memory cells have reduced current drive. Therefore, the optimum value for M is determined using the constraints of Equations 2 and 3 for low current operation. In addition, the DC trip-point has increased providing additional margin between the reference cell and the maximum sense cell Vt of an un-programmed cell.

30 Second, at high power supply operating voltages (6.0 V in the above example), the DC trip-point is optimized. With M = 2, the minimum sense cell Vt of a programmed cell has been reduced. Comparing the "un-usable" range (delta) of sense cell Vt of the fixed ratios with the scalable ratio (1.5 V for M = 2, 2.5 V for M = 6 and 1.15 V for M = scalable), the scalable ratio produces a smaller "un-usable" range. At high power

supply operating voltages, memory cells have increased current drive, thus reducing the need to optimize sense amplifier speed using M.

In the Fig. 4 embodiment, two outputs, DIFIN1 and DIFIN2, are shown. When the output amplifier is a differential amplifier, then DIFIN1 and DIFIN2 represent the two inputs to the amplifier. However, a differential amplifier is not essential. A single-ended amplifier can be used, in which case DIFIN2 alone is used as the output and input to the single-ended amplifier.

The voltage bias generator 25 comprises a voltage divider 31 made up of p-MOS transistors connected as current mirrors, from a node 32 of which is derived a voltage controlling a p-MOS transistor 33 connected in series with p-MOS transistors 34 and 35 from whose node 26 is derived a bias voltage for the gate of transistor 24. As V_{cc} changes, so does the bias voltage in an inverted manner controlling continuously the variable multiplier load represented by the two transistors 21. Thus, increases in V_{cc} result in decreases in the bias voltage at node 26. The transistor 24 in this case acts as a variable resistor.

Fig. 5 shows the sense amplifier circuit of Fig. 4 connected to the memory and several additional conventional circuits. Only several of the many memory cells are shown at 40, and only several of the many reference cells 41. Each word line when asserted activates a reference cell 41 and a row of memory cells 40. The blocks referenced 42-45 are described by their labels and are conventional in EPROM memories. The CONTROL input at 46 corresponds to the BIAS CONTROL input in Fig. 4 and functions to turn off the system in a power-down mode of the IC. Fig. 5 also shows two outputs AMPIN2, corresponding to DIFIN1, and AMPIN1, corresponding to DIFIN2. When a differential amplifier 48 is used, AMPIN2 and AMPIN1 are connected as shown. When a single-end amplifier 49 is used, then only the AMPIN1 output is connected as shown.

The key concept of the invention is that of current mirror scalability. In general terms, the scalable current mirror is composed of four components: a reference load, a fixed multiplier load, a variable multiplier load, and a voltage bias generator that controls the variable multiplier load by generating a bias voltage that decreases as a percentage of supply voltage as the supply voltage increases. Reduced bias voltage means increased I_{sense} and thus a reduced ratio M.

A general relationship between the three load elements can be developed. If X represents the size of reference load in terms of the number of transistors of a unit dimension, Y represents the size of the fixed multiplier load in terms of the number of

transistors of a unit dimension, and Z represents the size of the variable multiplier load in terms of the number of transistors of a unit dimension, then Y and Z are constrained as follows:

$$(X-1) \geq (Y + Z) \geq 2 \quad (4)$$

5 While it is preferred that Y is also ≥ 1 , it is also possible for $Y = 0$, provided that a minimum bias voltage is provided to ensure that the variable multiplier load provides a minimum I_{sense} corresponding to a fixed multiplier load. In this situation, Z would be chosen equal to 3 to emulate the performance of the Fig. 4 circuit. It will also be understood that the invention can be implemented by use of a single MOS transistor with, 10 say, a width (W1) for the reference load and a single MOS transistor with, say, a width (W2) for the multiplier load where the two widths determine the size of the respective transistors and are chosen in accordance with the principles taught herein.

 While the sizes of components have been given in the example, this is not critical, and other component sizes can be used. Also, the voltage supply operating ranges 15 given, while preferred, are not critical. Similarly, the p-MOS transistors can be replaced by n-MOS transistors or by bipolar transistors with appropriate changes in supply voltage polarities. Other kinds of bias generators that will supply an output voltage as a function of supply voltage can be substituted. Also, as will be evident from equation (4), the number of reference load transistors is not limited to 7, nor the multiplier load to 3. For clarity's sake, 20 in the schematics, the arrows at the MOS transistors denote the transistor drain electrode.

**CLAIMS:**

1. An electronic circuit comprising:

- a memory cell (40) for assuming a particular one of two logic states;
 - sense means (20, 14, 41, 48) for determining the particular logic state of the cell;
- characterized in that

5 - the circuit comprises bias means (24, 25) operative to control a sensitivity of the sense means dependent on a supply voltage applied to the circuit so as to render the sensitivity higher with a lower supply voltage than the sensitivity with a higher supply voltage.

2. The electronic circuit of claim 1, wherein:

- the sense means comprises:

10 - a sense load (20) for supplying a sense current (I_{sense}) to the memory cell to create a sense voltage (AMPIN1);

- reference means (14, 41) for creating a reference voltage (AMPIN2) from a reference current (I_{ref});

15 - a comparator (48) having inputs coupled to the memory cell and the reference means for providing an output signal indicative of the particular logic state upon comparing the sense voltage to the reference voltage;

- the bias means is operative to provide a control signal to at least the sense load or the reference means for control of a ratio of the sense current to the reference current.

3. The electronic circuit of claim 2, wherein the reference means comprises:

20 - a reference cell (41) having a specific logic state;

- a reference load (14) coupled to the reference cell via a reference node for supplying the reference current and for creating the reference voltage at the node.

4. The electronic circuit of claim 3, wherein:

25 - the reference load and the sense load form an input branch and an output branch, respectively, of a current mirror that has a current amplification factor between the input branch and the output branch, and wherein the bias means is operative to control the factor dependent on the supply voltage.

5. The circuit of claim 4, wherein:

- the reference load comprises a first plurality of transistors (15) arranged in parallel and



having control electrodes connected to one another and to the reference node;

- the sense load comprises a first transistor (22) and at least a second transistor (21) having conduction channels coupled in parallel to the memory cell and having control electrodes connected to one another and to the reference node;

- 5 - the sense load comprises a third transistor (24) having a conduction channel between the conduction channel of the second transistor and the memory cell, and having a control electrode connected to the bias means.

6. An electronic circuit comprising:

- a memory cell (40) for assuming a particular one of two logic states;
- 10 - a sense load (20) for supplying a sense current (I_{sense}) to create a sense voltage (AMPIN1) across the memory cell;
- a reference cell (41) having a specific logic state;
- a reference load (14) for supplying a reference current (I_{ref}) to create a reference voltage across the reference cell;
- 15 - a differential amplifier (48) coupled to the memory cell and the reference cell for receiving the sense voltage and the reference voltage;
- characterized in that the circuit comprises:
- means (24, 25) operative to control a ratio of the sense current to the reference current depending on a supply voltage applied to the circuit.