

FERROELECTRIC MEMORY DEVICES AND METHOD FOR TESTING THEM

ABSTRACT OF THE DISCLOSURE

A memory cell comprises a ferroelectric capacitor, first main memory cells (C0-C254) are connected to a first bit line (BL), a first reference memory cell (DC0) is connected to a second bit line (/BL), second main memory cells (C1-C255) are connected to the second bit line (/BL), and a second reference memory cell (DC1) is connected to the first bit line (BL). When a first operation mode is selected by a control circuit comprising NAND gates and NOR gates, first main memory cells (C0-C254) and first reference memory cell (DC0) are selected, and when a second operation mode is selected, first main memory cells (C0-C254) and second main memory cells (C1-C255) are selected. Thus, by switching the operation between the two operation modes, a ferroelectric memory device that has stable operation at a low voltage and high integration at a high voltage is provided.

FIGURE 1