RADIO FREQUENCY SWITCH BIASING TOPOLOGIES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Application No. 63/169,053 filed March 31, 2021, entitled RADIO FREQUENCY SWITCH BIASING TOPOLOGIES, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to switching circuits, related devices, and related methods for radio-frequency (RF) applications.

Description of the Related Art

[0003] Switches, including RF and/or Single Pole Double Throw (SPDT) switches, can be important components of RF and/or other circuit applications. When a switch is turned on (i.e., in an ON state), the switch requires a positive gate-to-source voltage (V_{GS}) to minimize on-resistance (R_{ON}) of the switch. When a switch is turned off (i.e., in an OFF state), the switch requires a negative V_{GS} to minimize off-capacitance (C_{OFF}) and/or non-linearity.

SUMMARY

[0004] In accordance with an aspect, the present disclosure relates to a switching circuit comprising a first series switch coupled to a first output port. The first series switch includes a first field-effect transistor (FET), a second FET, a third FET, a fourth FET, a fifth FET, and a sixth FET. The switching circuit further comprises a second series switch coupled to a second output port and coupling circuitry configured to couple a gate of the fifth FET and a gate of the sixth FET to a first node, a source of the fifth FET and a drain of the sixth FET to a second node, a source of the first FET and a drain of the second FET to a third node, a gate of the first FET and a drain of the fifth FET to a fourth node, a gate of the second FET and a source of the sixth FET to a fifth node, the fourth node and the fifth node to a first gate

voltage, and the first node to a second gate voltage that is different than the first gate voltage.

[0005] In some embodiments, the switching circuit further comprises a first shunt switch. The coupling circuitry may be further configured to couple the first output port between the first series switch and the first shunt switch.

[0006] The switching circuit may further comprise a second shunt switch. In some embodiments, the coupling circuitry is further configured to couple the second output port between the second series switch and the second shunt switch.

[0007] In some embodiments, the first shunt switch comprises four series-connected FETs. The second shunt switch may comprise four series-connected FETs.

[0008] The second series switch may comprise four series-connected FETs. In some embodiments, the first series switch further comprises a seventh FET and an eighth FET.

[0009] In some embodiments, the first gate voltage is configured to be approximately 0 V while the second gate voltage is positive. The second gate voltage may be configured to be approximately 0 V while the first gate voltage is positive.

[0010] An aspect of the present disclosure relate to a wireless device comprising a first series switch coupled to a first output port. The first series switch includes a first field-effect transistor (FET), a second FET, a third FET, a fourth FET, a fifth FET, and a sixth FET. The wireless device further comprises a second series switch coupled to a second output port and coupling circuitry configured to couple the fifth FET to the first FET, the fifth FET to the sixth FET, the first FET to the second FET, the first FET and the second FET to a first gate voltage, and the fifth FET and the sixth FET to a second gate voltage that is different than the first gate voltage.

[0011] The wireless device may further comprise a first shunt switch. The coupling circuitry may be further configured to couple the first output port between the first series switch and the first shunt switch.

[0012] In some embodiments, the wireless device further comprises a second shunt switch. The coupling circuitry may be further configured to couple the second output port between the second series switch and the second shunt switch.

[0013] The first shunt switch may comprise four series-connected FETs. The second shunt switch may comprise four series-connected FETs. In some embodiments, the second series switch comprises four series-connected FETs.

[0014] In accordance with an aspect of the present disclosure, a semiconductor die comprises a first series switch coupled to a first output port. The first series switch includes a first field-effect transistor (FET), a second FET, a third FET, a fourth FET, a fifth FET, and a sixth FET. The semiconductor die further comprises a second series switch coupled to a second output port and coupling circuitry configured to couple the fifth FET to the first FET, the fifth FET to the sixth FET, the first FET to the second FET, the first FET and the second FET to a first gate voltage, and the fifth FET and the sixth FET to a second gate voltage that is different than the first gate voltage.

[0015] In some embodiments, the semiconductor die further comprises a first shunt switch. The coupling circuitry may be further configured to couple the first output port between the first series switch and the first shunt switch.

[0016] The semiconductor die may further comprise a second shunt switch. The coupling circuitry may be further configured to couple the second output port between the second series switch and the second shunt switch.

[0017] In some embodiments, the first shunt switch comprises four series-connected FETs. The second shunt switch may comprise four series-connected FETs.

[0018] For purposes of summarizing the disclosure, certain aspects, advantages and novel features of the inventions have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the invention. Thus, the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Figure 1 illustrates an example circuit utilizing NVGs to create a negative voltage for one or more switches (e.g., Field-Effect Transistors (FETs)) of the circuit.