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ABSTRACT OF THE DISCLOSURE

Semiconductor Device

In a package of an LOC (Lead On Chip) structure in which inner lead portions are partially arranged over a major face of a semiconductor chip, there is disclosed a technique for thinning the package and speeding up signal transmission.

Specifically, by partially reducing the thicknesses of the signal inner leads arranged over the major face of the semiconductor chip, the thickness of a sealing resin is reduced while ensuring the mechanical strength of the package.

Moreover, the signal inner leads arranged over the major face of the semiconductor chip are arranged at predetermined spacings from the major face of the semiconductor chip. The power supplying inner leads are bonded to the major face of the semiconductor chip, thus providing a package having a reduced parasitic capacitance.

Figure 1