one of the plurality of coils of the powered accessory is adjacent to the one of the plurality of coils of the rail.

In still another alternative embodiment, a method of networking a removable accessory of a weapon to a microcontroller of the weapon is provided, the method including the steps of: inductively transferring data between the accessory and the microcontroller via a first pair of coils exclusively dedicated to data transfer; inductively transferring power to the accessory via another pair of pair of coils exclusively dedicated to power transfer; and wherein the accessory is capable of determining the first pair of coils by magnetizing a pin located on the weapon.

Other aspects and features of embodiments of the invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Other features, advantages and details appear, by way of example only, in the following description of embodiments, the description referring to the drawings in which:

FIG. 1 is a perspective view of an inductively powering rail mounted on a MIL-STD-1913 rail;

FIG. 2 is cross section vertical view of a primary U-Core and a secondary U-Core;

FIG. 3 is a longitudinal cross section side view of an accessory mounted to an inductively powering rail;

FIG. 4 is a block diagram of the components of one embodiment of an inductively powered rail system;

FIG. 5 is a block diagram of a primary Printed Circuit Board (PCB) contained within an inductively powering rail;

FIG. 6 is a block diagram of a PCB contained within an accessory;

FIG. 7 is a block diagram of the components of a master controller;

FIG. 8 is a flow chart of the steps of connecting an accessory to an inductively powering rail;

FIG. 9 is a flow chart of the steps for managing power usage;

FIG. 10 is a flow chart of the steps for determining voltage and temperature of the system;

FIG. 11 is a perspective view of a portion of a rail of a networked powered data system (NPDS) in accordance with an embodiment of the present invention;

FIGS. 12A-12C ~~and 12B~~ are cross-sectional views of an accessory mounted to a networked powered data system (NPDS);

FIGS. 13A and 13B are perspective views of an upper receiver with rails of the networked powered data system (NPDS) mounted thereto;

FIGS. 13C and 13D illustrate alternative embodiments of the upper receiver illustrated in FIGS. 13A and 13B;

FIGS. 14A and 14B are perspective views of rails of the networked powered data system (NPDS);

FIGS. 14C and 14D illustrate alternative embodiments of the rails illustrated in FIGS. 14A and 14B;

FIGS; 15A-15C illustrate the mounting an the rails of the networked powered data system (NPDS);

FIGS. 15D-15F illustrate alternative embodiments of the rails illustrated in FIGS. 15A-15C;

FIG. 16 is schematic illustration of power and data transfer between components of the networked powered data system (NPDS);

FIG. 17 is schematic illustration of a circuit for inductive power transfer in accordance with one exemplary embodiment of the present invention;

FIG. 18 is a perspective view of a portion of a weapon with the networked powered data system (NPDS) of one embodiment of the present invention;

FIG. 18A is a perspective view of a portion of a weapon with the networked powered data system (NPDS) according to an alternative embodiment of the present invention;

FIGS. 19A-19D are various views of a component for inductively coupling power and data between an upper receiver and a lower receiver of a weapon used with the networked powered data system (NPDS);

enable signal. The first D Flip Flop 176 latches the content of the Multiplexer 172 and the second D Flip-Flop 177 latches the value of D Flip-Flop 177 if a decision is made to enable or disable a slot.

Hall effect transistor 164 detects when an accessory is connected to inductively powering rail 14 and enables MOSFET driver 160.

Referring now to FIG. 6 a block diagram of a PCB contained within an accessory such as 42 is shown generally as 52 Feature 180 refers to the primary U-Core 26 and the secondary U-Core 50, establishing a power connection between inductively powering rail 14 and accessory 42. High power ramp circuitry182 slowly ramps the voltage up to high power load when power is turned on. This is necessary as some accessories such as those that utilize XEON bulbs when turned on have low resistance and they draw excessive current. High power load 184 is an accessory that draws more than on the order of two watts of power.

Full wave rectifier and DC/DC Converter 186 rectifies the power from U-Cores 180 and converts it to a low power load 188, for an accessory such as a night vision scope. Pulse shaper 190 clamps the pulse fiam the U-Cores 180 so that it is within the acceptable ranges for microcontroller 98 and utilizes FSK via path 192 to provide a modified pulse to microcontroller 98 Microcontroller 98 utilizes a Zigbee component 198 via Universal Asynchronous Receiver Transmitter component (UART 196) to communicate between an accessory 42 and master controller 72. The types of information ~~thar~~ that may be communicated would include asking the accessory for information about itself, instructing the accessory to enter low power mode or to transfer power.

Referring now to FIG. 7, a block diagram of the components of a master controller 72 is shown (see FIG. 1) Conductive power is provided from battery 78 via conductive power path 82. Hot swap controller 74 slowly connects the load to the inductively powering rail 14 to reduce the amount of in rush current during power up. This also allows for the limiting of the amount of current that can be drawn. Feature 200 is a 3.3v DC/DC switcher, which converts the battery voltage to 3.3V to be used by the master CPU 76.

Current sense circuitry 202 measures the amount of the current being used by the system 70 and feeds that information back to the master CPU 76. Master controller 72

axially insert the wedge members, a pair of complimentary securement screws 495 are used to provide the axial insertion force as they are inserted into the rail by engaging a complimentary threaded opening of the rail 414, wherein they contact and axially slide the wedge members 493 as the screw is inserted into the threaded opening.

Referring now to FIGS. 15D-F, alternative non-limiting configurations of bridges 487 are illustrated, in this embodiment, bridges 487 are attached to the rails by a mechanical means such as screws or any other equivalent device.

With reference now to FIG. 16, as discussed generally above the accessories 42~~, 94, 96~~ and the master CPU 76 can communicate with one another in several different manners. For example, and as also described above, the master CPU 76 can vary the frequency that power or another signal is provided to the accessories 42~~, 94, 96~~ to provide information (data) to them. Similarly, the accessories 42~~, 94, 96~~ can communicate data to the master CPU 76 by utilizing load modulation. As discussed above, such communication can occur on the same cores (referred to below as "core pairs") as are used to provide power or can occur on separate coils. Indeed, as described above, in one embodiment, one in every three coils is dedicated to data transmission.

FIG. 16 illustrates three different communication channels shown as a low speed channel 502, a medium speed channel 504 and a high speed channel 506. The low speed channel 502 extends from and allows communication between the master CPU 76 and any of the accessories 42~~, 94, 96~~. The low speed channel 502 can be driven by a low speed transmitter/receiver 510 in the master CPU 76 that includes selection logic 512 for selecting which of the accessories 42~~, 94, 96~~ to route the communication to.

Each accessory 42~~, 94, 96~~ includes low speed decoding/encoding logic 514 to receive and decode information received over the low speed channel 502. Of course, the low speed decoding/encoding logic 514 can also include the ability to transmit information from the accessories 42~~, 94, 96~~ as described above.

In one embodiment, the low speed channel 502 carries data at or about 100 kB/s. Of course, other speeds could be used. The low speed channel 502 passes through an inductive coil pair 520 (previously identified as primary coil 26 and secondary coil 50 hereinafter referred to as inductive coil pair 520) between each accessory 42~~, 94, 96~~ and the master CPU 76. It shall be understood, however, that the inductive coil pair could be

replaced include a two or more core portions about which the coil pair is wound. In another embodiment, the cores can be omitted and the inductive coil pair can be implemented as an air core transformer. As illustrated, the inductive coil pairs 520 are contained within the inductive powering rail 14. Of course and as illustrated in the previous embodiments, one or more of the coils included in the inductive coil pairs 520 can be displaced from the inductive powering rail 14.

The medium speed channel 504 is connected to the inductive coil pairs 520 and shares them with low speed channel 502. For clarity, branches of the medium speed channel 504 as illustrated in dashed lines. As one of ordinary skill will realize, data can be transferred on both the low speed channel 502 and the medium speed channel at the same time. The medium speed channel 504 is used to transmit data between the accessories 42~~, 94, 96~~.

Both the low and medium speed channels 502, 504 can also be used to transmit data to or receive data from an accessory (e.g. a tether) not physically attached to the inductively powering rail ~~74~~ 14 as illustrated by element 540. The connection between the master CPU 76 can be either direct or though an optional inductive coil pair 520'. In one embodiment, the optional inductive coil pair 520' couples power or data or both to a CPU located in or near a handle portion of a gun.

To allow for communication between accessories over the medium speed channel 504, the master CPU 76 can include routing logic 522 that couples signals from one accessory to another based on information either received on the medium speed channel 504. Of course, in the case where two accessories coupled to the inductively powering rail ~~74~~ 14 are communicating via the medium speed channel 502, the signal can be boosted or otherwise powered to ensure is can drive the inductive coil pairs 520 between the accessories.

In another example, the accessory that is transmitting the data first utilizes the low speed channel 502 to cause the master CPU 76 to set the routing logic 522 to couple the medium speed channel 504 to the desired receiving accessory. Of course, the master CPU 76 itself (or an element coupled to it) can be used to separate low and medium speed communications from one another and provide them to either the low speed

transmitter/receiver 510 or the routing logic 522, respectively. In one embodiment, the medium speed channel 504 carries data at 10 MB/s.

FIG. 16 also illustrates a high speed channel 506. In one embodiment, the high speed channel 506 is formed by an optical data line and runs along at least a portion of the length of the inductively powering rail 14. For clarity, however, the high speed channel 506 is illustrated separated from the inductively powering rail 14. Accessories 42~~, 94, 96~~ can include optical transmitter/receivers 542 for providing signals to and receiving signals from the high speed channel 506. In one embodiment, a high speed signal controller 532 is provided to control data flow along the high speed channel 506. It shall be understood that the high speed signal controller 532 can be located in any location and may be provided, for example, as part of the master CPU 76. In one embodiment, the high speed signal controller 532 is an optical signal controller such as, for example, an optical router.

FIG. 17 illustrates an example of the MOSFET driver 154 coupled to MOSFET and transformer circuitry 156. In general, the MOSFET driver 154 the MOSFET and transformer circuitry 156 to produce an alternating current (AC) output at an output coil 710. The AC output couples power to a receiving coil 712. As such, the output coil 710 and the receiving coil 712 form an inductive coil pair 520. In one embodiment, the receiving coil 712 is located in an accessory as described above.

It shall be understood that it is desirable to achieve efficient power transfer from the output coil 710 to the receiving coil 712 (or vice versa). Utilizing the configuration shown in FIG. 17 has led, in some instances, to a power transfer efficiency of greater than 90%. In addition, it shall be understood, that the accessory could also include such a configuration to allow for power transfer from the receiving coil 712 to the output coil 710. The illustrated MOSFET and transformer circuitry 156 includes an LLC circuit 711 that, in combination with the input and output coils, forms an LLC resonant converter. The LLC circuit 711 includes, as illustrated, a leakage inductor 706, a magnetizing inductor 708 and a capacitor 714 serially connected between input node 740 and ground. The magnetizing inductor 708 is coupled in parallel with the output coil 710. The operation and location of the first and second driving MOSFET's 702, 704 is well known in the art and not discussed further herein. In one embodiment, utilizing an LLC resonant converter as illustrated in FIG. 17 can lead to increased proximity effect losses due to the