

CLAIMS

1. A method of forming an interconnect structure, comprising:
forming a recess within a dielectric layer;
conformally depositing a barrier layer within the recess;
forming a cobalt-infused ruthenium liner above the barrier layer, the cobalt containing ruthenium liner comprising:
a first liner above the barrier layer, the first liner comprising ruthenium; and
a second liner above the first liner, the second liner comprising cobalt, wherein migration of cobalt atoms from the second liner to the first liner form the cobalt-infused ruthenium liner;
depositing a conductive material above the cobalt-infused ruthenium liner to fill the recess; and
forming a capping layer above a top surface of the conductive material, the capping layer comprising cobalt.
2. The method of claim 1, wherein the forming the cobalt-infused ruthenium liner above the barrier layer comprises
conformally depositing the first liner above the barrier layer, the first liner comprising ruthenium;
conformally depositing the second liner above the first liner, the second liner comprising cobalt; and,
conformally depositing a third liner above the second liner, the third liner comprising ruthenium, wherein migration of cobalt atoms from the second liner to the first liner and the third liner form a cobalt-infused ruthenium liner.
3. The method of claim 1 or claim 2, wherein forming the cobalt-infused ruthenium liner reduces a concentration gradient between the capping layer and the cobalt-infused ruthenium liner preventing diffusion of cobalt atoms from the capping layer.
4. The method of claim 1 or claim 2, wherein a thickness of the second liner is less than a thickness of the first liner.
5. The method of claim 1 or claim 2, wherein the thickness of the second liner is greater than the thickness of the first liner.
6. The method of claim 2, wherein a thickness of the second liner is less than a thickness of the third liner.
7. The method of claim 1 or claim 2, wherein the conductive material comprises copper.
8. The method of claim 1 or claim 2, wherein the barrier layer comprises tantalum nitride.

9. The method of claim 1 or claim 2, further comprising conducting a planarization process to remove excess conductive material from the interconnect structure.
10. The method of claim 2, further comprising selectively removing portions of the first liner, portions of the second liner, and portions of the third liner parallel to the dielectric layer from a bottom region of the interconnect structure, wherein remaining portions of the first liner, the second liner, and the third liner remain on sidewalls of the interconnect structure.
11. The method of claim 10, wherein the selectively removing the portions of the first liner, the portions of the second liner, and the portions of the third liner parallel to the dielectric layer from the bottom region of the interconnect structure reduces via resistance.
12. A semiconductor structure, comprising:
an interconnect structure within a dielectric layer, the interconnect structure comprising:
a barrier layer located on a bottom surface and sidewalls of the interconnect structure;
a first liner directly above the barrier layer, the first liner comprises ruthenium;
a second liner directly above the first liner, the second liner comprises cobalt;
a conductive material above the second liner substantially filling the interconnect structure; and
a capping layer directly above the conductive material, the capping layer comprises cobalt, wherein migration of cobalt atoms from the second liner to the first liner reduces a concentration gradient between the capping layer and the first liner that prevents diffusion of cobalt atoms from the capping layer.
13. The semiconductor structure of claim 12, further comprising a third liner above the second liner, the third liner comprising ruthenium, wherein migration of cobalt atoms from the second liner interposed between the first liner and the third liner form a cobalt-infused ruthenium liner that reduces the concentration gradient between the capping layer and the cobalt-infused ruthenium liner and prevents diffusion of cobalt atoms from the capping layer.
14. The semiconductor structure of claim 13, wherein portions of the first liner, portions of the second liner, and portions of the third liner remain on sidewalls of the interconnect structure and a bottom portion of the interconnect structure is covered only by the barrier layer.
15. The semiconductor structure of claim 14, wherein a thickness of the second liner is less than a thickness of the first liner and the third liner.
16. The semiconductor structure of claim 12, wherein the conductive material comprises copper and the barrier layer comprises tantalum nitride.