FLOATING BODY CELL STRUCTURES, DEVICES INCLUDING SAME, AND METHODS FOR FORMING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "SEMICONDUCTOR-METAL-ON-INSULATOR STRUCTURES, METHODS OF FORMING SUCH STRUCTURES, AND SEMICONDUCTOR DEVICES INCLUDING SUCH STRUCTURES" (attorney docket number 2269-9742US); co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "SEMICONDUCTOR DEVICES INCLUDING A DIODE STRUCTURE OVER A CONDUCTIVE STRAP, AND METHODS OF FORMING SUCH SEMICONDUCTOR DEVICES" (attorney docket number 2269-9803US); co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "THYRISTOR-BASED MEMORY CELLS, DEVICES AND SYSTEMS INCLUDING THE SAME AND METHODS FOR FORMING THE SAME" (attorney docket number 2269-9804US); and co-pending U.S. Patent Application Serial No. 12/XXX,XXX filed on even date herewith and titled "SEMICONDUCTOR CELLS, ARRAYS, DEVICES AND SYSTEMS HAVING A BURIED CONDUCTIVE LINE AND METHODS FOR FORMING THE SAME" (attorney docket number 2269-9819US), the disclosure of each of which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

Embodiments of the present invention relate to methods, structures, and devices for increasing memory density and, more specifically, to devices comprising multi-gate floating body cell structures, devices including such structures, and methods for forming such devices.

BACKGROUND

A dynamic random access memory (DRAM) cell, including a transistor and a capacitor, has a small cell size and a high operation speed. However, capacitor integration and scaling hamper reduction of DRAM cell area. For each DRAM memory generation, a constant capacitance value is targeted and requires a complicated stack or a deep-trench

capacitor that leads to additional process steps and lessens compatibility with conventional, complementary metal oxide semiconductor (CMOS) structures.

In order to solve scaling problems, an alternative solution has been proposed where the conventional storage capacitor is replaced by a thin-film body of a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET). The memory storage mechanism for such a structure is based on the threshold voltage shift produced by majority carrier excess (accumulation) or deficit (depletion) in a floating-body. The cell utilizes the floating-body effect to store charge under the channel of an SOI transistor, which changes the transistor's threshold voltage, as a storage element. Since there is no body contact to instantly adjust a majority charge carrier concentration, equilibrium is established only after a relatively "long" period of time, which renders SOI memories attractive in terms of retention and refresh time.

As floating body cell size becomes smaller, the volume of the floating body decreases and the area between the source and the drain becomes closer, less charge is stored in the floating body resulting in charge loss being swept out by a forward bias effect caused by Shockley-Read Hall (SRH) recombination. Such charge loss may result in a decrease or loss of charge retention in the cell. In order to prevent this phenomenon in the conventional construction, the thickness of the SOI substrate is reduced as the cell size becomes smaller. However, as the thickness of the SOI substrate is reduced, the amount of charge accumulated in the floating body is decreased and the cell may be more susceptible to noise during operation. That is, the floating body effect is decreased, reducing the operating margin of the device.

There is a need for methods, structures and devices for increasing density and reliability in floating body transistors.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIGS. 1-3 illustrate perspective views of a portion of a floating body cell device in accordance with embodiments of the present disclosure;

FIGS. 4-14 illustrate cross-sectional, perspective and top plan views of a portion of a floating body cell structure during various stages of fabrication in accordance with the embodiments of the present disclosure illustrated in FIGS. 1-3;

FIG. 15 illustrates a perspective view of a portion of a floating body cell device in accordance with another embodiment of the present disclosure;

FIGS. 16-19 illustrate cross-sectional and perspective views of a portion of a floating body cell structure during various stages of fabrication in accordance with the embodiment of the present disclosure illustrated in FIG. 15;

FIGS. 20-22 illustrate electrical circuit diagrams, each representing a portion of a floating body cell device in accordance with embodiments of the present disclosure; and

FIG. 23 illustrates a simplified block diagram of a system implemented according to one or more embodiments described herein.

DETAILED DESCRIPTION

A multi-gate floating body cell structure, a device including such a structure and methods for forming such a structure are disclosed. Such structures include, for example, at least one floating body cell disposed on a back gate and another gate associated with the at least one floating body cell. The another gate may be disposed within the at least one floating body or on sidewalls thereof. The structures and devices may be used in numerous semiconductor devices, such as, dynamic random access memory (DRAM), zero capacitor random access memory (Z-RAM), and embedded dynamic random access memory (eDRAM). The structures and devices may further be used in a system such as, central processing units (CPUs), a system-on-a-chip (SOC), sensors, imagers, micro electro-mechanical systems (MEMS) and nano electro-mechanical systems (NEMS). Methods of forming such structures include forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a wafer, removing a portion of the semiconductive material to form a plurality of floating bodies protruding from a surface of the base material, removing another portion of the semiconductive material to form a void in each of the plurality of floating bodies, exposing the plurality of floating bodies to at least one dopant to form a source region and a drain region in upper regions of each of the plurality of floating bodies and forming a gate associated with at least one of the plurality of floating bodies.

The structures formed in accordance with the various embodiments of the present disclosure include a plurality of floating body cells, each of which is disposed on a back gate and is associated with another gate. Each of the floating body cells of the plurality may include a source region and drain region spaced apart from the back gate by a volume of semiconductive material and a channel coupled by the back gate. The volume of semiconductive material between the back gate electrode and each of the source region and the drain region may substantially increase charge storage within the floating body cells, minimizing signal fluctuation. Additionally, the back gate may function as a capacitor in the device and, thus, provides longer retention time and increased memory density by reducing the area required by the device. The back gate may be formed as a local back gate, each of which may be independently biased, or as a global back gate. For example, a local back gate may be desired for programming and cell operation purposes. As configured, charge is stored

at the bottom of the floating body cell near the back gate and is, thus, isolated from the source region and the drain region. Accordingly, charge loss during operation is minimized providing longer retention, improved reliability and decreased disturbance.

The structures and devices formed in accordance with various embodiments of the present disclosure may be stacked with a variety of memory devices, such as a complementary metal-oxide semiconductor (CMOS) device. Integrating the structures and devices formed in accordance with various embodiments of the present disclosure may reduce the cell size and provide increased cache memory density.

The following description provides specific details, such as material types and processing conditions, in order to provide a thorough description of embodiments of the present disclosure and implementation thereof. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details and in conjunction with conventional fabrication techniques. In addition, the description provided herein does not form a complete process flow for manufacturing a semiconductor device including the floating body cell structure. Only those process acts and structures necessary to understand the embodiments of the present invention are described in detail herein. Additional acts to form a complete semiconductor device including the floating body cell structure according to an embodiment of the invention may be performed by conventional techniques.

The materials described herein may be formed by any suitable technique including, but not limited to, spin coating, blanket coating, chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition ("PECVD"), atomic layer deposition ("ALD"), plasma enhanced ALD, or physical vapor deposition ("PVD"). Alternatively, materials may be grown *in situ*. A technique suitable for depositing or growing a particular material may be selected by a person of ordinary skill in the art. While the materials described and illustrated herein may be formed as layers, the materials are not limited thereto and may be formed in other three-dimensional configurations.

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the invention.

However, other embodiments may be utilized, and structural, logical, and electrical changes may be made without departing from the scope of the invention. The illustrations presented herein are not meant to be actual views of any particular system, logic device, memory cell, or floating body cell structure, but are merely idealized representations that are employed to describe the embodiments of the present invention. The drawings presented herein are not necessarily drawn to scale. Additionally, elements common between drawings may retain the same numerical designation.

FIGS. 1-3 are perspective views illustrating embodiments of floating body cell structures 100, 101 and 103 that include an array of floating body cells 104, the details of forming such are described in detail below. In some embodiments, the floating body cell structure 100 may be used to form a vertical multi-gate floating body cell device. Each floating body cell 104 in the array may include a volume of semiconductive material 102. The volume of semiconductor material 102 may includes pillars 108 defined a void 110, such as a u-shaped trench. An upper portion of the pillars 108 of each volume of semiconductive material 102 may be doped differently than remaining portions thereof to form a source region 112 and a drain region 114. By way of non-limiting example, the source region 112 and the drain region 114 may be doped with an n-type material, and the remaining portions of the volume of semiconductive material 102 may be doped with a p-type material. The source region 112 and drain region 114 may, respectively, be electrically coupled to an access line, such as common source line 116 and a data/sense line, such as bit line 118, as will be described in further detail. By way of non-limiting example, a contact plug 119 may be disposed between at least one of the source region 112 and the drain region 114 and the associated common source line 116 or bit line 118. Although the contact plug 119 is shown in FIG. 1 as being disposed between the drain regions 114 and the bit lines 118, the contact plug 119 may additionally, or alternatively, be disposed between the source regions 112 and the common source lines 116.

As a non-limiting example, each of the floating body cells 104 may be aligned with one another in an array that includes a plurality of rows extending in a first direction X and a plurality of columns extending in a second direction Y. The floating body cell structures 100, 101 and 103 shown in FIGS. 1-3 each include two (2) rows and three (3) columns. However, as configured, the floating body cell structures 100, 101 and 103 may include any number of

rows and columns. Additionally, the rows of floating body cells 104 aligned in the first direction X may be substantially perpendicular the columns of floating body cells 104 aligned in the second direction Y.

The floating body cells 104 may be disposed on a back gate 123 that may include, for example, a dielectric material 126, a conductive material 124 and an amorphous silicon material 128. For ease of description, conductive material 124 will hereinafter be referred to as back gate electrode 124 and the dielectric material 126 will hereinafter be referred to as back gate dielectric 126. The floating body cells 104 may each be electrically coupled to the back gate 123. Optionally, each of the back gate electrodes 124 may include a metal 127 and a doped region 125. The back gate electrodes 124 may be formed from, for example, a titanium-rich titanium nitride material, such as metal mode titanium nitride (MMTiN), a tantalum nitride material or a tantalum silicide material. The back gate dielectric 126 and the metal 127 form a metal-insulator-metal (MIM) structure that may function as a capacitor in the floating body cell structures 100, 101 and 103. Increased capacitance may be obtained by optimizing at least one of the work function of the metal 127 and the dielectric constant (k-value) of the back gate dielectric 126, and the thicknesses of the back gate dielectric 126 and the metal 127. Increasing capacitance in this manner may provide increased retention times in the floating body structures 100, 101 and 103.

The back gate electrode 124 may overlie an amorphous silicon material 128 disposed on an electrically insulative material 130, which may be formed on, for example, a wafer (not shown). In some embodiments, the back gate 123 of each of the floating body cells 104 may be configured as a local back gate, having sidewalls continuous and aligned with those of the floating body cells 104, as shown in FIGS. 1 and 2. A single floating body cell 104 may be disposed on the back gate 123 or, optionally, multiple floating body cells 104 may be disposed on the back gate 123. The back gate 123 may be patterned as a plurality of local back gates that may be independently biased during operation of the cell or may be patterned as a global back gate. For example, as shown in FIG.1, the back gate 123 may be a local back gate that extends in the first direction X along at least one of the rows and the plurality of floating body cells 104 aligned in that row may be disposed thereon. In other embodiments, as shown in FIG. 2, the back gate 123 may be a local back gate that extends in the second direction Y along at least one of the columns and the plurality of floating body cells 104

arranged in that column may be disposed thereon. As a non-limiting example, each of the back gates 123 may be aligned substantially parallel to an overlying one of the bit lines 118. In additional embodiments, as shown in FIG. 3, the back gate 123 of the floating body cell structure 100 may be a global back gate upon which the plurality of floating body cells 104, aligned in both the first direction X and the second direction Y, may be disposed.

A conductive element 132 may be disposed within the void 110 of each floating body cells 104. For the ease of description, the conductive element 132 is hereinafter referred to as buried gate electrode 132. Another dielectric material 134 may be disposed between the buried gate electrode 132 and the semiconductive material exposed within the void 110 in the floating body cell 104. For the ease of description, the dielectric material 134 is hereinafter referred to as buried gate dielectric 134. The buried gate dielectric 134 may, optionally, terminate below or at the respective interfaces between the channel region 106 of each of the floating body cells 104 and the source region 112 and the drain region 114 in the upper portions of the pillars 108. Electromagnetic fields emanating from the buried gate electrode 132 may establish a channel through the associated floating body cell 104, which enables a current to flow from the source region 112 to the drain region 114.

During use and operation of floating body cell 104, the majority carrier is stored at a location within the floating body cells 104 isolated from each of the buried gate electrode 132, the source region 112 and the drain region 114. As a result, charge retention and reliability may be enhanced compared to conventional floating body cell structures. As configured, a thickness of the volume of semiconductive material 102 may be varied to further distance the location of the stored charge from the buried gate electrode 132, the source region 112 and the drain region 114, as described in greater detail herein. Moreover, as configured, the volume of semiconductive material 102 may be formed to have a larger storage volume in comparison to a floating body of conventional structures. This enables increased charge storage within the floating body cell 104 and, therefore, may minimize signal fluctuation due to lost charge. As a result, floating body cell 104 may provide an enhanced signal, longer retention and increased reliability in comparison to conventional structures.

In some embodiments, the floating body cell structures 100, 101 and 103 may be superposed with and/or integrated with other memory elements (not shown), such as a CMOS

device, to form a multi-level semiconductor structure. The floating body cell structures 100, 101 and 103 may be operably coupled to at least one memory device to form a system, such as a central processing unit (CPU) and a system-on-a-chip (SOC) or multiple tiers of the floating body cell structures 100, 101 and 103 may be vertically stacked over one another to increase density.

With reference to FIGS. 4-14, a method of forming floating body cell structures 100, 101 and 103 including a plurality of floating body cells 104, such as those shown in FIGS. 1-3, will now be described, wherein like elements are designated by like numerals. Referring to FIG. 4, a semiconductor structure 140 may be provided that includes a semiconductive material 142 overlying and contacting the back gate dielectric 126, the back gate dielectric 126 overlying and contacting the back gate contact 124, the back gate electrode 124 overlying and contacting the amorphous silicon material 128, and the amorphous silicon material 128 overlying and contacting the electrically insulative material 130. The semiconductor structure 140 may, optionally, include the doped region 125 and the metal 127, as shown in broken lines. In some embodiments, the electrically insulative material 130 may be formed over a handle wafer 144. As used herein, the term "wafer" means any structure that includes a semiconductor type material including, for example, silicon, germanium, gallium arsenide, indium phosphide, and other III-V or II-VI type semiconductive materials. Wafers include, for example, not only conventional wafers but also other bulk semiconductor substrates such as, by way of non-limiting example, silicon-on-insulator (SOI) type substrates, silicon-on-sapphire (SOS) type substrates, and epitaxial layers of silicon supported by another material. Furthermore, when reference is made to a "wafer" in the following description, previous process steps may have been utilized to at least partially form elements or components of a circuit or device in or over a surface of the wafer. In some embodiments, the electrically insulative material 130 may be disposed over memory elements (not shown), such as a complementary metal oxide semiconductor structure (CMOS) device, formed in or on the handle wafer 144. The electrically insulative material 130 may include, for example, a buried oxide (BOX) material.

The semiconductor structure 140 may be formed, for example, by transferring the amorphous silicon material 128, the back gate contact 124, the back gate dielectric 126 and the semiconductive material 142 to the electrically insulative material 130 overlying the

handle wafer 144 by a process described herein using a modification of so-called SMART-CUT® layer transfer technology. Such processes are described in detail in, for example, U.S. Patent No. RE 39,484 to Bruel, U.S. Patent No. 6,303,468 to Aspar et al., U.S. Patent No. 6,335,258 to Aspar et al., U.S. Patent No. 6,756,286 to Moriceau et al., U.S. Patent No. 6,809,044 to Aspar et al., U.S. Patent No. 6,946,365 to Aspar et al., and U.S. Patent Application Publication No. 2006/0099776 to Dupont. However, other processes suitable for manufacturing the semiconductor substrate 140 may also be used. In conventional implementation of the SMART-CUT® layer transfer technology, donor wafers and acceptor wafers are bonded together using a high temperature anneal. The temperature used to bond the donor and acceptor wafers is from about 1000°C to about 1300°C. However, due to the presence of the back gate contact 123, it may be advantageous to fabricate the semiconductor structure 140 at decreased temperatures to prevent thermal damage to the back gate contact 123. Accordingly, as described herein, the semiconductor structure 140 may be formed using substantially reduced temperatures in comparison to those required by conventional SMART-CUT® layer transfer technology.

Referring to FIG. 5, a workpiece 146 may be formed by respectively depositing the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 over the semiconductive material 142, which may comprise a portion of, for example, a donor wafer. Optionally, the workpiece 146 may include the metal 127 and the doped region 125. The doped region 125 may be formed using conventional methods, such as an ion implantation process or a high temperature diffusion process and may have a thickness between about 10 nm and about 50 nm. The metal 127, if present, may comprise a titanium nitride material, such as metal mode titanium nitride (MMTiN), a titanium silicide material, a tantalum nitride material or a tungsten silicide material. The metal 127 may be formed over and in contact with the doped region 125 using a CVD process, a PVD process, a sputtering process or a plating process and may have a thickness between about 10 nm to about 30 nm. The back gate dielectric 126 may include, for example, an oxide material, a high k dielectric material or a nitride material and may be formed over and in contact with the semiconductive material 142 or the metal 127, if present, using a CVD process or by decomposing tetraethyl orthosilicate (TEOS). As a non-limiting example, the back gate dielectric 126 may have a thickness of from about 20 Å to about 70 Å. The back gate electrode 124 may include a

conductive material, such as a metal material. The conductive material may be titanium nitride material, a titanium silicide material, a tungsten silicide material or a tantalum nitride material and may be formed over and in contact with the back gate dielectric 126 using a CVD process, a PVD process, a sputtering process or a plating process. By way of non-limiting example, the back gate electrode 124 may have a thickness of from about 100 Å to about 600 Å. The amorphous silicon material 128 may be formed over and in contact with the back gate dielectric 126 using, for example, a PVD process or a CVD process. As a non-limiting example, the amorphous silicon material 128 may have a thickness of from about 100 Å to about 400 Å.

An atomic species may be implanted into the semiconductive material 142 to form a transfer region 150. The atomic species may be hydrogen ions, ions of rare gases, also termed inert or noble gases, or ions of fluorine. The atomic species may be implanted into the semiconductive material 142 to form an implanted zone 152, which is shown in the semiconductive material 142 in broken lines. The atomic species may be implanted into the semiconductive material 142 prior to formation of one or all of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 thereon or after formation of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 thereon. As known in the art, the depth at which the ions are implanted into the semiconductive material 142 is at least partially a function of the energy with which the ions are implanted into the semiconductive material 142. The implanted zone 152 may be formed at a desired depth in the semiconductive material 142, which is dependent on parameters, such as implant dose and energy of the atomic species, as known in the art. A depth D of the implanted zone 152 within the semiconductor structure 142 may correspond to a desired thickness and/or volume of the floating body cells 104 shown in FIGS. 1-3. The volume of the floating bodies 102 and the amount of charge that may be stored therein may be increased by increasing the depth D and, thus, the thickness of the semiconductive material 142. Furthermore, by increasing the thickness of the floating body cells 104, the charge stored therein may be further isolated from conductive elements of the floating body cell structures 100, 101 and 103 (i.e., the buried gate electrode 132, the source regions 112 and drain regions 114). By isolating the stored charge from the conductive elements, charge loss may be decreased and, thus, the floating body cells 104 may provide increased retention and

improved reliability. As a non-limiting example, the atomic species may be implanted into the semiconductive material 142 with an energy selected to form the implanted zone 152 at a depth D of between about 100 nm and about 350 nm (about 1000 Å to about 3500 Å).

The implanted zone 152 includes a layer of microbubbles or microcavities comprising the implanted ion species, and provides a weakened structure within the semiconductive material 142. The semiconductive material 142 may then be thermally treated at a temperature above that at which implantation is effected to effect crystalline rearrangement in the wafer and coalescence of the microbubbles or microcavities. Optionally, the attachment surface (not shown) may be formed by exposing the major surface of the amorphous silicon material 128 of the semiconductive material 142 to a reactive ion etching (RIE) plasma including an inert gas (e.g., argon, oxygen, or nitrogen) to form a plasma-activated material, or by exposing the surface to a dilute ammonia hydroxide or hydrogen fluoride solution. Forming an attachment surface on the amorphous silicon material 128 may increase the kinetics of a subsequent bonding act with the electrically insulative material 130 overlying the handle wafer 144, due to the increased mobility of the ionic species (e.g., hydrogen).

As shown in FIG. 6, the workpiece 146 may be superposed on the electrically insulative material 130 overlying the handle wafer 144 so that the electrically insulative material 130 is in contact with the amorphous silicon material 128 of the workpiece 146. The amorphous silicon material 128 of the workpiece 146 may be bonded to the electrically insulative material 130. By way of non-limiting example, the amorphous silicon material 126 and the electrically insulative material 130 may also be bonded without heat at ambient temperature (from about 20°C to about 25°C). Pressure may also be applied to at least one of the workpiece 146 and the handle wafer 144 to bond the amorphous silicon material 128 to the electrically insulative material 130. As another non-limiting example, the amorphous silicon material 126 may be bonded to the insulator material 104 by heating the semiconductor structure 140 to a temperature of less than about 600°C, such as from about 300°C to about 400°C. If the electrically insulative material 130 is formed from silicon dioxide, silicon-oxide bonds may form between the amorphous silicon material 128 and the insulator material 130. Because the back gate electrode 124 may be formed of a metal or other heat sensitive material, the temperature to which the semiconductor structure 140 is exposed may be less than the melting point of the back gate contact 124.

To form the semiconductor structure 140 shown in FIG. 4, the transfer region 150 may be removed from the semiconductive material 142, along the implanted zone shown in FIG. 6. The transfer region 150 may be removed by techniques known in the art, such as by applying a shear force to the implanted zone 152 or by applying heat or a jet gas stream at the implanted zone 152. The atomic species in the implanted zone 152 produce a weakened region in the semiconductive material 142 of the workpiece 146, which is susceptible to cleavage.

The back gate dielectric 126, the back gate contact 124, and the amorphous silicon material 128 and a portion of the semiconductive material 142 below the implanted zone 152 may remain bonded to the electrically insulative material 130 to form the semiconductor structure 140 shown in FIG. 4. After separation of the semiconductive material 142, an exposed surface 154 thereof may be undesirably rough. To remedy this deficiency, the exposed surface 154 of the semiconductive material 142 may be smoothed to a desired degree in order to facilitate further processing as described, according to techniques known in the art, for example, one or more of grinding, wet etching, and CMP.

FIG. 7 shows the semiconductor structure 140 of FIG. 4 after a mask material 156 has been deposited on the semiconductive material 142 and patterned to form apertures through which surfaces 154 of the semiconductive material 142 are exposed. The mask material 156 may include, for example, a photoresist material, an oxide material, transparent carbon or amorphous carbon. Methods of forming and patterning the mask material 156 are known in the art and, therefore, are not described in detail herein. For the sake of simplicity, the handle wafer 144 underlying the electrically insulative material 130 has been omitted from the remaining figures.

As shown in FIG. 8A, portions of the semiconductive material 142 exposed through the apertures in the mask material 156 may be removed to form trenches 158 between remaining portions of the semiconductive material 142. The remaining portions of the mask material 156 may then be removed. By way of non-limiting example, the trenches 158 may be formed extending through the semiconductive material 142 in the second direction Y. A reactive ion etching (RIE) process to selectively remove the semiconductive material 142 with respect to the mask material 156 and the back gate dielectric 126. In some embodiments, as shown in FIG. 8B, after removing the portions of the semiconductive

material 142, portions of each of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 may be removed *in situ* through the same mask material 156, to form an individual or single back gate 123 such as that shown in the floating body cell structure 101 of FIG. 2. FIG. 2 shows continuous 124, 126, 128 portions of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 may be removed using, for example, an anisotropic reactive ion (i.e., plasma) etching process, to expose the underlying electrically insulative material 130. For example, if the back gate dielectric 126 is formed from silicon dioxide, a reactive ion etching (RIE) process using a nitrogen trifluoride (NF_3)-based gas, a chlorine (Cl)-based gas or a bromide (Br)-based gas may be performed to selectively remove the back gate 123 from the silicon dioxide with respect to the mask material 156. If the back gate electrode 124 is titanium nitride, an anisotropic etching process using a tetrafluoromethane (CF_4) gas, a mixture of a bromine-containing gas and a fluorine-containing gas or a mixture of a fluorine-containing gas and a chlorine-containing gas to remove the titanium nitride with respect to the mask material 156. If the amorphous silicon material 128 is amorphous polysilicon, an anisotropic etching process using a mixture of a fluorine-containing gas and a chlorine-containing gas may be used to remove the amorphous silicon material with respect to the mask material 156. In other embodiments, the trenches 158 may be formed using a conventional pitch-doubling process, by techniques known in the art.

FIG. 9 shows the semiconductor structure 140 after depositing a fill material 160 in the trenches 158. While FIG. 9 shows trenches 158 extending through the back gate dielectric 126 , the back gate contact 124, and the amorphous silicon material 128, the channels 128 to be filled may be as shown in FIG. 8A. By way of non-limiting example, the fill material 160 may include a dielectric material such as an oxide material or a nitride material, and may be deposited using a chemical vapor deposition process or a spin-on dielectric process.

FIGS. 10-13 are cross-sectional views of the semiconductor structure 140 shown in FIG. 9, taken along section line 9-9, after a sacrificial mask material 162 has been deposited thereover and a plurality of openings 164 have been formed. The sacrificial mask material 162 may be formed over the semiconductive material 142 and the fill material (not shown) and the plurality of openings 164 may be formed by removing portions of the sacrificial mask

material 162 and the semiconductive material 142. Each of the plurality of openings 164 may be formed extending in the second direction Y. As a non-limiting example, the sacrificial mask material 162 may be formed from an amorphous silicon material or a dielectric material using a CVD process. By way of non-limiting example, the openings 164 may be formed by providing a photoresist material (not shown) over the sacrificial mask material 162 and removing portions of the photoresist material overlying regions of sacrificial mask material 162 and the semiconductive material 142 that are to be removed. An anisotropic etching process (e.g., a dry reactive ion or plasma etching process) may then be used to etch the regions of the sacrificial mask material 162 and the semiconductive material 142 exposed through the photoresist material to form openings 164 that expose regions of the sacrificial mask material 162. For example, if the sacrificial mask material 162 and the semiconductive material 142 are formed from polysilicon, a reactive ion etching process using a fluorine (Fl)-based gas may be performed to selectively remove the amorphous silicon material, forming the openings 164 between portions of the semiconductive material 142. As a non-limiting example, the openings 164 may be formed to have a dimension D1 of 0.5F and the remaining portions of the semiconductive material 142 may have a dimension D2 of 1.5F. Additionally, the back gates 123, as shown in FIG. 1, may be formed by removing a portion of each of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 130 after removing the semiconductive material 142 such that the openings 164 extend through each of these materials leaving the back gate 123 intact. After forming the openings 164, the remaining photoresist material may be removed using a conventional ashing process. The openings 164 may also be formed using a conventional pitch-doubling process, by techniques known in the art.

As shown in FIG. 11, another fill material 166 such as an oxide material or a nitride material may be deposited in the openings 164. By way of non-limiting example, the fill material 166 may be deposited using a CVD process, a PECVD process or spin-on dielectric process. Thus, the semiconductive material 142 is completely physically isolated from the surrounding environment.

As shown in FIG. 12, a portion of each of the sacrificial material 162 and the semiconductive material 142 may be removed to form the voids 110 in the semiconductive material 142. If the semiconductive material 142 is formed from a crystalline silicon

material, a plasma including a mixture of sulfur hexafluoride (SF_6) gas, oxygen gas and helium (He) gas, or a mixture of sulfur hexafluoride gas and trifluoromethane (CHF_3) gas, may be introduced to the semiconductor structure 140 to form the voids 110. FIG. 11 depicts the voids 110 as having a u-shaped profile; however, voids having various other profiles may also be formed, as will be recognized by one of ordinary skill in the art.

FIG. 13 shows the semiconductor structure 140 after the buried gate electrodes 132 have been formed in each of the voids 110. As a non-limiting example, a CMP process may be used to remove portions of the fill material 166 and the sacrificial material 162 so that an upper surface 168 of the semiconductor structure 140 is substantially planar. The buried gate electrodes 132 may be formed from a conductive material such as, tungsten, titanium nitride or tantalum nitride, and may be deposited using a conventional CVD process, PVD process or ALD process. By way of non-limiting example, the conductive material may be formed over the semiconductor structure 140 and removed after deposition using a conventional CMP process, RIE process or wet etching process to form the buried gate electrodes 132. The buried gate dielectric 134 may be deposited over sidewalls of the semiconductive material 142 exposed in each of the voids 110 before forming the buried gate electrodes 132.

FIG. 14 shows the semiconductor structure 140 after forming the buried gate electrodes 132 in the voids 110 and another fill material 163 thereover. As shown in FIG. 14, source regions 112 and drain regions 114 may be formed in exposed regions of the pillars 108 of the volume of semiconductive material 102. The source regions 112 and drain regions 114 may include a silicon material that is doped with an n-type dopant, such as phosphorous or arsenic, (i.e., n-type silicon material). Exposed portions of the semiconductive material 142 may be doped using conventional methods, such as an ion implantation process or plasma ion process or a high temperature diffusion process. The source regions 112 and the drain regions 114 may be spaced apart from the back gate electrode 124 by the semiconductive material 142. As another example, a thin film of a n-type material (not shown) may be deposited over surfaces of the semiconductor structure 140 and a thermal anneal may be performed during which n-type dopants migrate into the semiconductive material 142 to form n-type silicon for the source regions 112 and drain regions 114. The source regions 112 and drain regions 114 may, optionally, be formed before forming the buried gate electrodes 132.

Referring back to FIGS. 1-3, after forming the source regions 112 and the drain

regions 114, the common source lines 116 may be formed over the source regions 112 aligned in each of the rows and the bit lines 118 may be formed over the drain regions 114 aligned in each of the columns. In some embodiments, the common source lines 116 and the bit lines 118 may be formed by depositing a conductive reactive material over the semiconductor structure 100, 100 or 103 and pattering the conductive material to form substantially straight and substantially parallel conductive lines. For example, the common source lines 116 may be formed in the direction X, each of the common sources lines 116 disposed above and substantially parallel to one of the buried gate electrodes 132. The bit lines 118 may be formed extending in the direction Y. Optionally, the contact plug 119 may be formed on at least one of the drain regions 114 and the source regions 112 to elevate that contact before forming the associated common source line 116 or bit line 118. For example, the contact plug 119 may be formed by depositing and patterning a doped amorphous silicon material. Optionally, the contact plug 119 may be replaced by a metal material, such as titanium nitride/tungsten, or the contact plug may be filled with the conductive reactive material during formation of the conductive lines.

FIG. 15 is a perspective view illustrating another embodiment of a floating body cell structure 200 that includes a plurality of floating body cells 104, the details of forming such will be described in detail. For the purposes of illustrating the floating body cells 104, a portion of the gate 170 has been removed, as shown in broken lines. In some embodiments, the floating body cell structure 200 may be used to form a vertical multi-gate floating body cell device. Each floating body cell 104 in the floating body cell structure 200 may include a floating body cell 104 formed from a volume of semiconductive material that includes a channel region 106 extending between pillars 108, which are separated by a void 110, such as, a u-shaped trench, as described with respect to FIGS. 1-3. The source regions 112 and the drain regions 114 may be formed in the upper regions of the pillars 108 and may, respectively, be electrically coupled to an access line, such as common source line 116 and a data/sense line, such as bit line 118. By way of non-limiting example, the common source line 116 and the bit line 118 may, respectively, be formed directly on the source regions 112 and the drain regions 114, as shown in FIG. 18. Additionally, a contact plug 119 may be disposed between the source regions 112 and the associated common source line 116 to elevate the contact or between the drain regions 114 and the associated bit line 118.

The floating body cells 104 may be arranged as described with respect to FIGS. 1-3, wherein the floating body cells 104 are aligned in a plurality of rows in the first direction X and the plurality of columns in the second direction Y substantially perpendicular to the first direction X. FIG. 4 shows the back gate 123 as a local back gate disposed under rows of floating body cells 104 and extending in a direction parallel to floating body cells 104. The sidewalls of the back gate 123 are shown as being continuous and aligned with those of the floating body cells 104. In other embodiments, the back gate 123 may be configured as described with respect to FIGS. 2 and 3.

At least one conductive element 170 may be disposed on opposite vertical surfaces (i.e., sidewalls) of each of the floating body cells 104. For the ease of description, the conductive element 170 is hereinafter referred to as gate 170. Another dielectric material 172 may be disposed between the gate 170 and the sidewalls of the floating body cells 104. For the ease of description, the dielectric material 172 is hereinafter referred to as gate dielectric 172. Each of the floating body cells 104 of the floating body cell structure 200 may be electrically coupled to the back gate 123 and the gates 170 disposed on two sidewalls of the floating body cells 104 so that the floating body cell 104 includes three gates, or may be electrically coupled to the back gate 123 and the gate 170 disposed on a single sidewall of the floating body cells 104 so that the floating body cell 104 includes two gates. Electromagnetic fields emanating from the gates 170 may establish a channel through the associated floating body 104, which enables a current to flow from the source region 112 to the drain region 114.

FIGS. 16-20 illustrate embodiments of a method of forming the floating body cell structure 200 shown in FIG. 15. Referring to FIG. 16, a semiconductor structure 240 that includes an array of floating body cells 104, each including a volume of semiconductive material 102 disposed on the back gate 123 may be formed using methods such as those described with respect to FIGS. 4-12. The back gate 123 may include back gate dielectric 126, back gate electrode 124 and amorphous silicon material 128 and may be disposed on an electrically insulative material 130 overlying a wafer (not shown). As previously described, other logic elements (not shown), such as a complementary metal oxide semiconductor structure (CMOS) device, may be formed in or on the wafer. Although the trenches 158 are illustrated as terminating within the electrically insulative material 130, the trenches 158 may, optionally, be formed to terminate on the back gate dielectric 126, such as

those described with respect to FIG. 8A.

FIGS. 17A1-17B2 are cross-sectional views of the semiconductor structure 140 shown in FIG. 16, taken along section line 16-16. After forming the trenches 158, the gates 170 may be formed on sidewalls of the floating body cells 104, as described with respect to FIGS. 17A1-17B2. As shown in FIG. 17A1, a gate dielectric material 172 and a conductive material 174 may be formed over semiconductor structure 240. By way of non-limiting example, the gate dielectric material 172 may be an oxide material, a nitride material or a high k dielectric material formed using, for example, a chemical vapor deposition process or a thermal oxidation process. For example, if the gate dielectric material 172 is silicon dioxide, the semiconductor structure 240 may be exposed to an oxygen gas at a temperature of from about 900°C to about 1175°C to form the silicon dioxide on sidewalls of the floating body cells 104. The conductive material 174 may then be formed over the gate dielectric material 172. As a non-limiting example, the conductive material 174 may be formed from titanium nitride, tantalum nitride or tungsten and may be deposited using a chemical vapor deposition process. Referring to FIG. 17A2, an anisotropic dry etching process or a wet etching process may be performed to remove portions of the conductive material 174 and the gate dielectric material 172 to form the gates 170.

In other embodiments, the gates 170 may be formed on the sidewalls of the floating body cells 104 as shown with respect to FIGS. 17B1 and 17B2. Referring to FIG. 17B1, after forming the gate dielectric material 172 over the semiconductive material 142, the remaining portions of the trenches 158 between regions of the semiconductive material 142 may be filled with the conductive material 174 and the conductive material 174 may be recessed back to a desired thickness. By way of non-limiting example, the conductive material 174 may be formed from titanium nitride, tantalum nitride or tungsten and may be deposited using a chemical vapor deposition process. Spacers 176 including a dielectric material may be formed on sidewalls of the gate dielectric material 172 above the conductive material 174 using a conventional spacer etching process. Referring to FIG. 17B2, an anisotropic etching process may be performed to remove a portion of the conductive material 174 to form the gates 170. After forming the gates 170, the spacers 176 may be removed using, for example, a conventional selective etching process.

FIGS. 18A and 18B are top down views of the semiconductor structure 240 shown in

FIGS. 17A2 and 17B2 illustrating the configuration of the gates 170. The gates 170 may be formed to electrically connect pluralities of the floating body cells 104 with one another. As a non-limiting example, the gates 170 may extend along the columns of floating body cells 104 in direction Y. As shown in FIG. 18A, each of the gates 170 may substantially circumscribe the plurality of floating body cells 104 in a single one of the columns, vertical surfaces (i.e., sidewalls) of each of the floating body cells 104 being contacted by the gate 170. Referring to FIG. 18B, another embodiment is shown wherein the gates 170 are configured in a comb-like structure extending along at least one of the rows in a direction X and terminating at or near an end thereof, each of the gates 170 being disposed on opposite sidewalls of the floating body cells 104 in the row. Contacts 178 may be electrically coupled to each of the gates 170, for example, at a terminal portion thereof, so that the gates 170 are independently connected. Accordingly, as shown in FIGS. 18A and 18B, the gates 170 may be configured to form single-gate, dual-gate and triple-gate floating body cells 104.

As shown in FIG. 19, after forming the gates 170, source regions 112 and drain regions 114 may be formed in the upper portion of the pillars 108 of floating body cells 104 by exposing the semiconductor structure 240 to an n-type dopant or a p-type dopant, as described with respect to FIG. 14. The common source lines 116 may then be formed over the source regions 112 of the floating body cells 104 and the bit lines 118 may be formed over the drain regions 114 of the floating body cells 104 to form the semiconductor structure 240 shown in FIG. 18. The common source lines 116 and bit lines 118 may be formed by depositing a conductive material and pattering the conductive material to form conductive lines extending in the first direction X, substantially perpendicular to the gates 170. Since the common source lines 116 and bit lines 118 are parallel to another, the common source lines 116 and bit lines 118 may be formed using a conventional damascene process. For example, a sacrificial dielectric material (not shown) may be deposited over the semiconductor structure 240 and a pattern of apertures may be formed therein in locations at which the common source lines 116 and bit lines 118 are to be formed using a conventional lithographic process. A conductive material may be deposited over the semiconductor structure 240 to fill the apertures and a chemical mechanical polishing process may be used to remove a portion of the conductive material overlying the dielectric material to form the common source lines 116 and bit lines 118. Optionally, a doped material (not shown) may be formed on at least one

of the source regions 112 and drain regions 114 before forming the associated common source line 116 or bit line 118.

FIGS. 20-22 are electrical circuit diagrams, each of which illustrates a floating body cell structure that includes a plurality of floating body cells, such as those described with respect to FIGS. 1-3 and 15. As shown in FIG. 20, the floating body cell structure 300 may include a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a global back gate 123, such as the back gate 123 shown in FIG. 2. The global back gate 123 and the gate 132 may each be operably coupled to a bias voltage enabling the floating body cells 104 associated with the global back gate 123 to be simultaneously biased.

FIG. 21 illustrates a floating body cell structure 400 including a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a local back gate 123. The local back gates 123 may have a comb-like configuration, such as that shown in FIG. 18B, to provide two distinct addresses for each of the local back gates 123.

FIG. 22 illustrates a floating body cell structure 500 including a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a local back gate 123, such as the back gates 123 shown in FIGS. 2 and 15. Each of the local back gates 123 may be operably coupled to a bias voltage that may be used to individually bias each of the back gates 123.

It should be noted that, during the various stages of fabrication, the floating body cell structures 101, 102 and 103, respectively shown in FIGS. 1 through 3, may be integrated or vertically stacked with other semiconductor structures having a similar structure or with a memory element or device, such as a CMOS device. For example, the CMOS device may be formed over or beneath one of the floating body cell structures 101, 102 or 103 to form a multi-level semiconductor structure, which provides a substantially reduced dies size. The floating body cell structures 101, 102 and 103 may be stacked over another floating body cell structure, memory or logic using, for example, a modification of the so-called SMART-CUT® layer transfer technology as described with respect to FIGS. 4-6.

FIG. 23 illustrates a simplified block diagram of an electronic system 2300 implemented according to one or more embodiments described herein. The electronic system 2300 includes at least one input device 2302, at least one output device 2304, a

memory access device, such as one or more processors 2306, such as a system-on-chip (SOC), a central processing unit (CPU), processors and the like that may, and one or more memory devices 2308. The memory devices 2308 include at least one embodiment of the devices or methods described herein. The electronic system 2300 may be part of a number of computing, processing, and consumer products. As non-limiting examples, some of these products may include personal computers, handheld devices, cameras, phones, wireless devices, displays, chip sets, set top boxes, games, and vehicles.

CONCLUSION

In some embodiments, the present invention includes floating body cell structures, devices including such structures and method for forming such structures. The floating body cell structures may include a back gate, at least one floating body and another gate associated with the at least one floating body. The at least one floating body may include a semiconductive material and may extend from the back gate to a source region and a drain region. The source region and the drain region may be spaced apart from the back gate by the at least one floating body. The at least one floating body may include a void in the semiconductive material, each of the source region and the drain region disposed opposite the back gate. The another gate may be disposed within the void in the at least one floating body to form a double-gate floating body cell structure or may be disposed on at least one surface of the at least one floating body to form a triple-gate floating body cell structure. A gate dielectric may be disposed between the back gate and the at least one floating body and an amorphous silicon material underlying the back gate and disposed over a wafer. The back gate may be a local back gate comprising sidewalls continuous and aligned with sidewalls of the at least one floating body or a global back gate in which a plurality of floating body cells are disposed in an array. The floating body cell structure may further include a bit line electrically coupled to the back gate and operably coupled to a bias voltage for independently biasing the back gate. The floating body cell structure may further include a common source line electrically coupling the source region of the at least one floating body cell to a source region of at least another floating body and a bit line electrically coupling the drain region of the at least one floating body cell to a drain region of the at least another floating body.

In additional embodiments, the present invention includes a floating body cell device

that includes a plurality of floating bodies, each comprising a semiconductive material and extending from a back gate to a source region and a drain region and another gate associated with the plurality of floating bodies and operably coupled to a voltage source and a common source line electrically coupling the source regions of the plurality of floating bodies and a bit line electrically coupling the drain regions of the plurality of floating bodies. The device may be integrated in at least one of a dynamic random access memory, a zero capacitor random access memory, a central processing unit, a system-on-a-chip and embedded dynamic random access memory integrated therewith. The plurality of floating bodies may be aligned in a first direction to form a plurality of rows and a second direction substantially perpendicular to the first direction to form a plurality of columns.

In yet further embodiments, a floating body cell device includes a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, at least one back gate associated with the plurality of the floating bodies and at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source. Each of the floating bodies of the plurality of floating bodies may include a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region. The at least one back gate may include a conductive material disposed over an amorphous silicon material on an electrically insulative material. The at least another gate may include a conductive material disposed on each of the plurality of floating bodies that may extend, for example, in the first direction, electrically coupling the plurality of floating bodies in at least one of the plurality of rows. The at least another gate may include a conductive material disposed within the u-shaped trench and, for example, may extend in the second direction, electrically coupling the plurality of floating bodies in at least one of the plurality of columns. The at least one back gate may be configured to be biased independent of the another gate. The floating body cell structure may be disposed over and integrated with a memory device, such as a CMOS device, or may be vertically stacked in a number of tiers to increase density.

In yet further embodiments, the present invention includes methods of forming a floating body cell device that include forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a wafer,

removing a portion of the semiconductive material to form a plurality of floating bodies protruding from a surface of the base, removing another portion of the semiconductive material to form a void in each of the plurality of floating bodies, exposing the plurality of floating bodies to at least one dopant to form a source region and a drain region in upper regions of each of the plurality of floating bodies and forming a gate associated with at least one of the plurality of floating bodies. The base may be formed by forming a donor wafer comprising a dielectric material, a gate material and an amorphous silicon material overlying a crystalline silicon wafer, implanting ions a predetermined depth into the crystalline silicon wafer, attaching the amorphous silicon material of the donor wafer to an electrically insulative material overlying a handle wafer; and separating a portion of the donor wafer to leave a portion of the crystalline silicon wafer so that the dielectric material, the gate material, and the amorphous silicon material overlying a surface of the electrically insulative material of the handle wafer.

In yet further embodiments, the present invention includes a system that includes at least one memory device and at least one floating body cell device operably coupled to the at least one memory device. The at least one floating body cell device may include an array of floating bodies, each of which includes a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region, at least one back gate associated with the array of the floating bodies and at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source. The system may include at least one of a central processing unit and a system-on-a-chip. The at least one memory device may include at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory. The at least one memory device and the at least one floating body cell device may be superposed with one another within the system.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the scope of the invention as defined by the following appended claims and their legal equivalents.

CLAIMS

What is claimed is:

1. A floating body cell structure, comprising:

a back gate;

at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region; and

another gate associated with the at least one floating body.

2. The floating body cell structure of claim 1, wherein the source region and the drain region are spaced apart from the back gate by the at least one floating body.

3. The floating body cell structure of claim 1, wherein the at least one floating body comprises a void in the semiconductive material, each of the source region and the drain region disposed opposite the back gate.

4. The floating body cell structure of claim 3, wherein the another gate is disposed within the void in the at least one floating body.

5. The floating body cell structure of claim 1, wherein the another gate is disposed on at least one surface of the at least one floating body to form a triple-gate floating body cell structure.

6. The floating body cell structure of claim 1, wherein the back gate comprises a local back gate comprising sidewalls continuous and aligned with sidewalls of the at least one floating body.

7. The floating body cell structure of claim 1, wherein the at least one floating body comprises a plurality of floating bodies disposed on a single back gate in an array.

8. The floating body cell structure of claim 1, further comprising a bit line operably coupled to a bias voltage for independently biasing the back gate.

9. The floating body cell structure of claim 1, further comprising a common source line electrically coupling the source region of the at least one floating body cell to a source region of at least another floating body and a bit line electrically coupling the drain region of the at least one floating body cell to a drain region of the at least another floating body.

10. A floating body cell device, comprising:

a back gate;

a plurality of floating bodies, each comprising a semiconductive material and extending from the back gate to a source region and a drain region;

another gate associated with the plurality of floating bodies and operably coupled to a voltage source; and

a common source line electrically coupling the source regions of the plurality of floating bodies and a bit line electrically coupling the drain regions of the plurality of floating

bodies.

11. The floating body cell device of claim 10, further comprising at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory integrated therewith.

12. The floating body cell device of claim 10, wherein the plurality of floating bodies are aligned in a first direction to form a plurality of rows and a second direction substantially perpendicular to the first direction to form a plurality of columns.

13. A floating body cell device, comprising:

a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, each floating body comprising:

a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate associated with the plurality of the floating bodies; and

at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source.

14. The floating body cell device of claim 13, wherein the at least one back gate comprises a conductive material disposed over an amorphous silicon material on an electrically insulative material.

15. The floating body cell device of claim 13, wherein the at least another gate comprises a conductive material disposed on each of the plurality of floating bodies.

16. The floating body cell device of claim 15, wherein the conductive material extends in the first direction, electrically coupling the plurality of floating bodies in at least one of the plurality of rows.

17. The floating body cell device of claim 13, wherein the at least another gate comprises a conductive material disposed within the u-shaped trench.

18. The floating body cell device of claim 17, wherein the conductive material extends in the second direction, electrically coupling the plurality of floating bodies in at least one of the plurality of columns.

19. The floating body cell device of claim 13, wherein the at least one back gate is configured to be biased independent of the at least another gate.

20. The floating body cell device of claim 13, wherein the floating body cell structure is vertically stacked with at least one other logic device.

21. A method of forming a floating body cell device, comprising:

forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a wafer;

removing a portion of the semiconductive material to form a plurality of floating bodies protruding from a surface of the base;

removing another portion of the semiconductive material to form a void in each of the plurality of floating bodies;

exposing the plurality of floating bodies to at least one dopant to form a source region and a drain region in upper regions of each of the plurality of floating bodies; and

forming a gate associated with at least one of the plurality of floating bodies.

22. The method of claim 21, wherein forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a substrate comprises:

forming a donor wafer comprising a dielectric material, a gate material and an amorphous silicon material overlying a crystalline silicon wafer;

implanting ions a predetermined depth into the crystalline silicon wafer;

attaching the amorphous silicon material of the donor wafer to an electrically insulative material overlying a handle wafer; and

separating a portion of the donor wafer to leave a portion of the crystalline silicon wafer, the dielectric material, the gate material, and the amorphous silicon material overlying a surface of the electrically insulative material of the handle wafer.

23. The method of claim 21, wherein removing a portion of the semiconductive material to form the plurality of floating bodies protruding from a surface of the base further comprises removing a portion of the dielectric material, the gate material and the amorphous silicon material to form the plurality of floating bodies, each floating body disposed on an electrically insulative material overlying the wafer.

24. The method of claim 21, wherein forming a gate associated with at least one of the plurality of floating bodies comprises depositing a conductive material within the void of each of the plurality of floating bodies.

25. The method of claim 21, wherein forming a gate associated with at least one of the plurality of floating bodies comprises forming a conductive structure on at least one surface of each of the plurality of floating bodies.

26. A system, comprising:

at least one memory device; and

at least one floating body cell device operably coupled to the at least one memory device and comprising:

an array of floating bodies, each floating body of the array comprising a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate associated with the array of floating bodies; and

at least another gate associated with the array of floating bodies and operably coupled to a voltage source.

27. The system of claim 26, wherein the system comprises at least one of a central processing unit and a system-on-a-chip.

28. The system of claim 26, wherein the at least one memory device comprises at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory.

29. The system of claim 26, wherein the at least one memory device and the at least one floating body cell device are superposed with one another.

30. The system of claim 26, wherein the array of floating bodies includes a plurality of floating bodies aligned in a first direction and aligned in a second direction substantially perpendicular the first direction.

FLOATING BODY CELL STRUCTURES, DEVICES INCLUDING SAME, AND METHODS FOR FORMING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent is related to co-pending U.S. Patent Application Serial No. 12/715,704 filed on March 2, 2010, and titled "SEMICONDUCTOR-METAL-ON-INSULATOR STRUCTURES, METHODS OF FORMING SUCH STRUCTURES, AND SEMICONDUCTOR DEVICES INCLUDING SUCH STRUCTURES"; co-pending U.S. Patent Application Serial No. 12/715,843 filed on March 2, 2010, and titled "FLOATING BODY CELL STRUCTURES, DEVICES INCLUDING SAME, AND METHODS FOR FORMING SAME"; co-pending U.S. Patent Application Serial No. 12/715,743 filed on March 2, 2010, and titled "SEMICONDUCTOR DEVICES INCLUDING A DIODE STRUCTURE OVER A CONDUCTIVE STRAP, AND METHODS OF FORMING SUCH SEMICONDUCTOR DEVICES"; and co-pending U.S. Patent Application Serial No. 12/715,922 filed on March 2, 2010, and titled "SEMICONDUCTOR CELLS, ARRAYS, DEVICES AND SYSTEMS HAVING A BURIED CONDUCTIVE LINE AND METHODS FOR FORMING THE SAME", the disclosures of which are incorporated herein by reference.

TECHNICAL FIELD

Embodiments of the present invention relate to methods, structures, and devices for increasing memory density and, more specifically, to devices comprising multi-gate floating body cell structures, devices including such structures, and methods for forming such devices.

BACKGROUND

A dynamic random access memory (DRAM) cell, including a transistor and a capacitor, has a small cell size and a high operation speed. However, capacitor integration and scaling hamper reduction of DRAM cell area. For each DRAM memory generation, a constant capacitance value is targeted and requires a complicated stack or a deep-trench

capacitor that leads to additional process steps and lessens compatibility with conventional, complementary metal oxide semiconductor (CMOS) structures.

In order to solve scaling problems, an alternative solution has been proposed where the conventional storage capacitor is replaced by a thin-film body of a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET). The memory storage mechanism for such a structure is based on the threshold voltage shift produced by majority carrier excess (accumulation) or deficit (depletion) in a floating-body. The cell utilizes the floating-body effect to store charge under the channel of an SOI transistor, which changes the transistor's threshold voltage, as a storage element. Since there is no body contact to instantly adjust a majority charge carrier concentration, equilibrium is established only after a relatively "long" period of time, which renders SOI memories attractive in terms of retention and refresh time.

As floating body cell size becomes smaller, the volume of the floating body decreases and the area between the source and the drain becomes closer, less charge is stored in the floating body resulting in charge loss being swept out by a forward bias effect caused by Shockley-Read Hall (SRH) recombination. Such charge loss may result in a decrease or loss of charge retention in the cell. In order to prevent this phenomenon in the conventional construction, the thickness of the SOI substrate is reduced as the cell size becomes smaller. However, as the thickness of the SOI substrate is reduced, the amount of charge accumulated in the floating body is decreased and the cell may be more susceptible to noise during operation. That is, the floating body effect is decreased, reducing the operating margin of the device.

There is a need for methods, structures and devices for increasing density and reliability in floating body transistors.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIGS. 1-3 illustrate perspective views of a portion of a floating body cell device in accordance with embodiments of the present disclosure;

FIGS. 4-14 illustrate cross-sectional, perspective and top plan views of a portion of a floating body cell structure during various stages of fabrication in accordance with the embodiments of the present disclosure illustrated in FIGS. 1-3;

FIG. 15 illustrates a perspective view of a portion of a floating body cell device in accordance with another embodiment of the present disclosure;

FIGS. 16-19 illustrate cross-sectional and perspective views of a portion of a floating body cell structure during various stages of fabrication in accordance with the embodiment of the present disclosure illustrated in FIG. 15;

FIGS. 20-22 illustrate electrical circuit diagrams, each representing a portion of a floating body cell device in accordance with embodiments of the present disclosure; and

FIG. 23 illustrates a simplified block diagram of a system implemented according to one or more embodiments described herein.

DETAILED DESCRIPTION

A multi-gate floating body cell structure, a device including such a structure and methods for forming such a structure are disclosed. Such structures include, for example, at least one floating body cell disposed on a back gate and another gate associated with the at least one floating body cell. The another gate may be disposed within the at least one floating body or on sidewalls thereof. The structures and devices may be used in numerous semiconductor devices, such as, dynamic random access memory (DRAM), zero capacitor random access memory (Z-RAM), and embedded dynamic random access memory (eDRAM). The structures and devices may further be used in a system such as, central processing units (CPUs), a system-on-a-chip (SOC), sensors, imagers, micro electro-mechanical systems (MEMS) and nano electro-mechanical systems (NEMS). Methods of forming such structures include forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a wafer, removing a portion of the semiconductive material to form a plurality of floating bodies protruding from a surface of the base material, removing another portion of the semiconductive material to form a void in each of the plurality of floating bodies, exposing the plurality of floating bodies to at least one dopant to form a source region and a drain region in upper regions of each of the plurality of floating bodies and forming a gate associated with at least one of the plurality of floating bodies.

The structures formed in accordance with the various embodiments of the present disclosure include a plurality of floating body cells, each of which is disposed on a back gate and is associated with another gate. Each of the floating body cells of the plurality may include a source region and drain region spaced apart from the back gate by a volume of semiconductive material and a channel coupled by the back gate. The volume of semiconductive material between the back gate electrode and each of the source region and the drain region may substantially increase charge storage within the floating body cells, minimizing signal fluctuation. Additionally, the back gate may function as a capacitor in the device and, thus, provides longer retention time and increased memory density by reducing the area required by the device. The back gate may be formed as a local back gate, each of which may be independently biased, or as a global back gate. For example, a local back gate may be desired for programming and cell operation purposes. As configured, charge is stored

at the bottom of the floating body cell near the back gate and is, thus, isolated from the source region and the drain region. Accordingly, charge loss during operation is minimized providing longer retention, improved reliability and decreased disturbance.

The structures and devices formed in accordance with various embodiments of the present disclosure may be stacked with a variety of memory devices, such as a complementary metal-oxide semiconductor (CMOS) device. Integrating the structures and devices formed in accordance with various embodiments of the present disclosure may reduce the cell size and provide increased cache memory density.

The following description provides specific details, such as material types and processing conditions, in order to provide a thorough description of embodiments of the present disclosure and implementation thereof. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details and in conjunction with conventional fabrication techniques. In addition, the description provided herein does not form a complete process flow for manufacturing a semiconductor device including the floating body cell structure. Only those process acts and structures necessary to understand the embodiments of the present invention are described in detail herein. Additional acts to form a complete semiconductor device including the floating body cell structure according to an embodiment of the invention may be performed by conventional techniques.

The materials described herein may be formed by any suitable technique including, but not limited to, spin coating, blanket coating, chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition ("PECVD"), atomic layer deposition ("ALD"), plasma enhanced ALD, or physical vapor deposition ("PVD"). Alternatively, materials may be grown *in situ*. A technique suitable for depositing or growing a particular material may be selected by a person of ordinary skill in the art. While the materials described and illustrated herein may be formed as layers, the materials are not limited thereto and may be formed in other three-dimensional configurations.

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the invention.

However, other embodiments may be utilized, and structural, logical, and electrical changes may be made without departing from the scope of the invention. The illustrations presented herein are not meant to be actual views of any particular system, logic device, memory cell, or floating body cell structure, but are merely idealized representations that are employed to describe the embodiments of the present invention. The drawings presented herein are not necessarily drawn to scale. Additionally, elements common between drawings may retain the same numerical designation.

FIGS. 1-3 are perspective views illustrating embodiments of floating body cell structures 100, 101 and 103 that include an array of floating body cells 104, the details of forming such are described in detail below. In some embodiments, the floating body cell structure 100 may be used to form a vertical multi-gate floating body cell device. Each floating body cell 104 in the array may include a volume of semiconductive material 102. The volume of semiconductor material 102 may includes pillars 108 defined a void 110, such as a u-shaped trench. An upper portion of the pillars 108 of each volume of semiconductive material 102 may be doped differently than remaining portions thereof to form a source region 112 and a drain region 114. By way of non-limiting example, the source region 112 and the drain region 114 may be doped with an n-type material, and the remaining portions of the volume of semiconductive material 102 may be doped with a p-type material. The source region 112 and drain region 114 may, respectively, be electrically coupled to an access line, such as common source line 116 and a data/sense line, such as bit line 118, as will be described in further detail. By way of non-limiting example, a contact plug 119 may be disposed between at least one of the source region 112 and the drain region 114 and the associated common source line 116 or bit line 118. Although the contact plug 119 is shown in FIG. 1 as being disposed between the drain regions 114 and the bit lines 118, the contact plug 119 may additionally, or alternatively, be disposed between the source regions 112 and the common source lines 116.

As a non-limiting example, each of the floating body cells 104 may be aligned with one another in an array that includes a plurality of rows extending in a first direction X and a plurality of columns extending in a second direction Y. The floating body cell structures 100, 101 and 103 shown in FIGS. 1-3 each include two (2) rows and three (3) columns. However, as configured, the floating body cell structures 100, 101 and 103 may include any number of

rows and columns. Additionally, the rows of floating body cells 104 aligned in the first direction X may be substantially perpendicular the columns of floating body cells 104 aligned in the second direction Y.

The floating body cells 104 may be disposed on a back gate 123 that may include, for example, a dielectric material 126, a conductive material 124 and an amorphous silicon material 128. For ease of description, conductive material 124 will hereinafter be referred to as back gate electrode 124 and the dielectric material 126 will hereinafter be referred to as back gate dielectric 126. The floating body cells 104 may each be electrically coupled to the back gate 123. Optionally, each of the back gate electrodes 124 may include a metal 127 and a doped region 125. The back gate electrodes 124 may be formed from, for example, a titanium-rich titanium nitride material, such as metal mode titanium nitride (MMTiN), a tantalum nitride material or a tantalum silicide material. The back gate dielectric 126 and the metal 127 form a metal-insulator-metal (MIM) structure that may function as a capacitor in the floating body cell structures 100, 101 and 103. Increased capacitance may be obtained by optimizing at least one of the work function of the metal 127 and the dielectric constant (k-value) of the back gate dielectric 126, and the thicknesses of the back gate dielectric 126 and the metal 127. Increasing capacitance in this manner may provide increased retention times in the floating body structures 100, 101 and 103.

The back gate electrode 124 may overlie an amorphous silicon material 128 disposed on an electrically insulative material 130, which may be formed on, for example, a wafer (not shown). In some embodiments, the back gate 123 of each of the floating body cells 104 may be configured as a local back gate, having sidewalls continuous and aligned with those of the floating body cells 104, as shown in FIGS. 1 and 2. A single floating body cell 104 may be disposed on the back gate 123 or, optionally, multiple floating body cells 104 may be disposed on the back gate 123. The back gate 123 may be patterned as a plurality of local back gates that may be independently biased during operation of the cell or may be patterned as a global back gate. For example, as shown in FIG.1, the back gate 123 may be a local back gate that extends in the first direction X along at least one of the rows and the plurality of floating body cells 104 aligned in that row may be disposed thereon. In other embodiments, as shown in FIG. 2, the back gate 123 may be a local back gate that extends in the second direction Y along at least one of the columns and the plurality of floating body cells 104

arranged in that column may be disposed thereon. As a non-limiting example, each of the back gates 123 may be aligned substantially parallel to an overlying one of the bit lines 118. In additional embodiments, as shown in FIG. 3, the back gate 123 of the floating body cell structure 100 may be a global back gate upon which the plurality of floating body cells 104, aligned in both the first direction X and the second direction Y, may be disposed.

A conductive element 132 may be disposed within the void 110 of each floating body cells 104. For the ease of description, the conductive element 132 is hereinafter referred to as buried gate electrode 132. Another dielectric material 134 may be disposed between the buried gate electrode 132 and the semiconductive material exposed within the void 110 in the floating body cell 104. For the ease of description, the dielectric material 134 is hereinafter referred to as buried gate dielectric 134. The buried gate dielectric 134 may, optionally, terminate below or at the respective interfaces between the channel region 106 of each of the floating body cells 104 and the source region 112 and the drain region 114 in the upper portions of the pillars 108. Electromagnetic fields emanating from the buried gate electrode 132 may establish a channel through the associated floating body cell 104, which enables a current to flow from the source region 112 to the drain region 114.

During use and operation of floating body cell 104, the majority carrier is stored at a location within the floating body cells 104 isolated from each of the buried gate electrode 132, the source region 112 and the drain region 114. As a result, charge retention and reliability may be enhanced compared to conventional floating body cell structures. As configured, a thickness of the volume of semiconductive material 102 may be varied to further distance the location of the stored charge from the buried gate electrode 132, the source region 112 and the drain region 114, as described in greater detail herein. Moreover, as configured, the volume of semiconductive material 102 may be formed to have a larger storage volume in comparison to a floating body of conventional structures. This enables increased charge storage within the floating body cell 104 and, therefore, may minimize signal fluctuation due to lost charge. As a result, floating body cell 104 may provide an enhanced signal, longer retention and increased reliability in comparison to conventional structures.

In some embodiments, the floating body cell structures 100, 101 and 103 may be superposed with and/or integrated with other memory elements (not shown), such as a CMOS

device, to form a multi-level semiconductor structure. The floating body cell structures 100, 101 and 103 may be operably coupled to at least one memory device to form a system, such as a central processing unit (CPU) and a system-on-a-chip (SOC) or multiple tiers of the floating body cell structures 100, 101 and 103 may be vertically stacked over one another to increase density.

With reference to FIGS. 4-14, a method of forming floating body cell structures 100, 101 and 103 including a plurality of floating body cells 104, such as those shown in FIGS. 1-3, will now be described, wherein like elements are designated by like numerals. Referring to FIG. 4, a semiconductor structure 140 may be provided that includes a semiconductive material 142 overlying and contacting the back gate dielectric 126, the back gate dielectric 126 overlying and contacting the back gate contact 124, the back gate electrode 124 overlying and contacting the amorphous silicon material 128, and the amorphous silicon material 128 overlying and contacting the electrically insulative material 130. The semiconductor structure 140 may, optionally, include the doped region 125 and the metal 127, as shown in broken lines. In some embodiments, the electrically insulative material 130 may be formed over a handle wafer 144. As used herein, the term "wafer" means any structure that includes a semiconductor type material including, for example, silicon, germanium, gallium arsenide, indium phosphide, and other III-V or II-VI type semiconductive materials. Wafers include, for example, not only conventional wafers but also other bulk semiconductor substrates such as, by way of non-limiting example, silicon-on-insulator (SOI) type substrates, silicon-on-sapphire (SOS) type substrates, and epitaxial layers of silicon supported by another material. Furthermore, when reference is made to a "wafer" in the following description, previous process steps may have been utilized to at least partially form elements or components of a circuit or device in or over a surface of the wafer. In some embodiments, the electrically insulative material 130 may be disposed over memory elements (not shown), such as a complementary metal oxide semiconductor structure (CMOS) device, formed in or on the handle wafer 144. The electrically insulative material 130 may include, for example, a buried oxide (BOX) material.

The semiconductor structure 140 may be formed, for example, by transferring the amorphous silicon material 128, the back gate contact 124, the back gate dielectric 126 and the semiconductive material 142 to the electrically insulative material 130 overlying the handle wafer 144 by a process described herein using a modification of so-called SMART-CUT® layer transfer technology. Such processes are described in detail in, for example, U.S. Patent No. RE 39,484 to Bruel, U.S. Patent No. 6,303,468 to Aspar et al., U.S. Patent No. 6,335,258 to Aspar et al., U.S. Patent No. 6,756,286 to Moriceau et al., U.S. Patent No. 6,809,044 to Aspar et al., U.S. Patent No. 6,946,365 to Aspar et al., and U.S. Patent Application Publication No. 2006/0099776 to Dupont. However, other processes suitable for manufacturing the semiconductor substrate 140 may also be used. In conventional implementation of the SMART-CUT® layer transfer technology, donor wafers and acceptor wafers are bonded together using a high temperature anneal. The temperature used to bond the donor and acceptor wafers is from about 1000°C to about 1300°C. However, due to the presence of the back gate contact 124, it may be advantageous to fabricate the semiconductor structure 140 at decreased temperatures to prevent thermal damage to the back gate contact 124. Accordingly, as described herein, the semiconductor structure 140 may be formed using substantially reduced temperatures in comparison to those required by conventional SMART-CUT® layer transfer technology.

Referring to FIG. 5, a workpiece 146 may be formed by respectively depositing the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 over the semiconductive material 142, which may comprise a portion of, for example, a donor wafer. Optionally, the workpiece 146 may include the metal 127 and the doped region 125. The doped region 125 may be formed using conventional methods, such as an ion implantation process or a high temperature diffusion process and may have a thickness between about 10 nm and about 50 nm. The metal 127, if present, may comprise a titanium nitride material, such as metal mode titanium nitride (MMTiN), a titanium silicide material, a tantalum nitride material or a tungsten silicide material. The metal 127 may be formed over and in contact with the doped region 125 using a CVD process, a PVD process, a sputtering process or a plating process and may have a thickness between about 10 nm to about 30 nm. The back gate dielectric 126 may include, for example, an oxide material, a high k dielectric material or a nitride material and may be formed over and in contact with the semiconductive material 142 or the metal 127, if present, using a CVD process or by decomposing tetraethyl orthosilicate (TEOS). As a non-limiting example, the back gate dielectric 126 may have a thickness of from about 20 Å to about 70 Å. The back gate electrode 124 may include a

conductive material, such as a metal material. The conductive material may be titanium nitride material, a titanium silicide material, a tungsten silicide material or a tantalum nitride material and may be formed over and in contact with the back gate dielectric 126 using a CVD process, a PVD process, a sputtering process or a plating process. By way of non-limiting example, the back gate electrode 124 may have a thickness of from about 100 Å to about 600 Å. The amorphous silicon material 128 may be formed over and in contact with the back gate dielectric 126 using, for example, a PVD process or a CVD process. As a non-limiting example, the amorphous silicon material 128 may have a thickness of from about 100 Å to about 400 Å.

An atomic species may be implanted into the semiconductive material 142 to form a transfer region 150. The atomic species may be hydrogen ions, ions of rare gases, also termed inert or noble gases, or ions of fluorine. The atomic species may be implanted into the semiconductive material 142 to form an implanted zone 152, which is shown in the semiconductive material 142 in broken lines. The atomic species may be implanted into the semiconductive material 142 prior to formation of one or all of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 thereon or after formation of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 thereon. As known in the art, the depth at which the ions are implanted into the semiconductive material 142 is at least partially a function of the energy with which the ions are implanted into the semiconductive material 142. The implanted zone 152 may be formed at a desired depth in the semiconductive material 142, which is dependent on parameters, such as implant dose and energy of the atomic species, as known in the art. A depth D of the implanted zone 152 within the semiconductor structure 142 may correspond to a desired thickness and/or volume of the floating body cells 104 shown in FIGS. 1-3. The volume of the floating bodies 102 and the amount of charge that may be stored therein may be increased by increasing the depth D and, thus, the thickness of the semiconductive material 142. Furthermore, by increasing the thickness of the floating body cells 104, the charge stored therein may be further isolated from conductive elements of the floating body cell structures 100, 101 and 103 (i.e., the buried gate electrode 132, the source regions 112 and drain regions 114). By isolating the stored charge from the conductive elements, charge loss may be decreased and, thus, the floating body cells 104 may provide increased retention and

improved reliability. As a non-limiting example, the atomic species may be implanted into the semiconductive material 142 with an energy selected to form the implanted zone 152 at a depth D of between about 100 nm and about 350 nm (about 1000 Å to about 3500 Å).

The implanted zone 152 includes a layer of microbubbles or microcavities comprising the implanted ion species, and provides a weakened structure within the semiconductive material 142. The semiconductive material 142 may then be thermally treated at a temperature above that at which implantation is effected to effect crystalline rearrangement in the wafer and coalescence of the microbubbles or microcavities. Optionally, the attachment surface (not shown) may be formed by exposing the major surface of the amorphous silicon material 128 of the semiconductive material 142 to a reactive ion etching (RIE) plasma including an inert gas (e.g., argon, oxygen, or nitrogen) to form a plasma-activated material, or by exposing the surface to a dilute ammonia hydroxide or hydrogen fluoride solution. Forming an attachment surface on the amorphous silicon material 128 may increase the kinetics of a subsequent bonding act with the electrically insulative material 130 overlying the handle wafer 144, due to the increased mobility of the ionic species (e.g., hydrogen).

As shown in FIG. 6, the workpiece 146 may be superposed on the electrically insulative material 130 overlying the handle wafer 144 so that the electrically insulative material 130 is in contact with the amorphous silicon material 128 of the workpiece 146. The amorphous silicon material 128 of the workpiece 146 may be bonded to the electrically insulative material 130. By way of non-limiting example, the amorphous silicon material 128 and the electrically insulative material 130 may also be bonded without heat at ambient temperature (from about 20°C to about 25°C). Pressure may also be applied to at least one of the workpiece 146 and the handle wafer 144 to bond the amorphous silicon material 128 to the electrically insulative material 130. As another non-limiting example, the amorphous silicon material 128 may be bonded to the insulator material 104 by heating the semiconductor structure 140 to a temperature of less than about 600°C, such as from about 300°C to about 400°C. If the electrically insulative material 130 is formed from silicon dioxide, silicon-oxide bonds may form between the amorphous silicon material 128 and the insulator material 130. Because the back gate electrode 124 may be formed of a metal or other heat sensitive material, the temperature to which the semiconductor structure 140 is exposed may be less than the melting point of the back gate contact 124.

To form the semiconductor structure 140 shown in FIG. 4, the transfer region 150 may be removed from the semiconductive material 142, along the implanted zone shown in FIG. 6. The transfer region 150 may be removed by techniques known in the art, such as by applying a shear force to the implanted zone 152 or by applying heat or a jet gas stream at the implanted zone 152. The atomic species in the implanted zone 152 produce a weakened region in the semiconductive material 142 of the workpiece 146, which is susceptible to cleavage.

The back gate dielectric 126, the back gate contact 124, and the amorphous silicon material 128 and a portion of the semiconductive material 142 below the implanted zone 152 may remain bonded to the electrically insulative material 130 to form the semiconductor structure 140 shown in FIG. 4. After separation of the semiconductive material 142, an exposed surface 154 thereof may be undesirably rough. To remedy this deficiency, the exposed surface 154 of the semiconductive material 142 may be smoothed to a desired degree in order to facilitate further processing as described, according to techniques known in the art, for example, one or more of grinding, wet etching, and CMP.

FIG. 7 shows the semiconductor structure 140 of FIG. 4 after a mask material 156 has been deposited on the semiconductive material 142 and patterned to form apertures through which surfaces 154 of the semiconductive material 142 are exposed. The mask material 156 may include, for example, a photoresist material, an oxide material, transparent carbon or amorphous carbon. Methods of forming and patterning the mask material 156 are known in the art and, therefore, are not described in detail herein. For the sake of simplicity, the handle wafer 144 underlying the electrically insulative material 130 has been omitted from the remaining figures.

As shown in FIG. 8A, portions of the semiconductive material 142 exposed through the apertures in the mask material 156 may be removed to form trenches 158 between remaining portions of the semiconductive material 142. The remaining portions of the mask material 156 may then be removed. By way of non-limiting example, the trenches 158 may be formed extending through the semiconductive material 142 in the second direction Y. A reactive ion etching (RIE) process to selectively remove the semiconductive material 142 with respect to the mask material 156 and the back gate dielectric 126. In some embodiments, as shown in FIG. 8B, after removing the portions of the semiconductive

material 142, portions of each of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 may be removed *in situ* through the same mask material 156, to form an individual or single back gate 123 such as that shown in the floating body cell structure 101 of FIG. 2. FIG. 2 shows continuous 124, 126, 128 portions of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 may be removed using, for example, an anisotropic reactive ion (i.e., plasma) etching process, to expose the underlying electrically insulative material 130. For example, if the back gate dielectric 126 is formed from silicon dioxide, a reactive ion etching (RIE) process using a nitrogen trifluoride (NF_3)-based gas, a chlorine (Cl)-based gas or a bromide (Br)-based gas may be performed to selectively remove the back gate 123 from the silicon dioxide with respect to the mask material 156. If the back gate electrode 124 is titanium nitride, an anisotropic etching process using a tetrafluoromethane (CF_4) gas, a mixture of a bromine-containing gas and a fluorine-containing gas or a mixture of a fluorine-containing gas and a chlorine-containing gas to remove the titanium nitride with respect to the mask material 156. If the amorphous silicon material 128 is amorphous polysilicon, an anisotropic etching process using a mixture of a fluorine-containing gas and a chlorine-containing gas may be used to remove the amorphous silicon material with respect to the mask material 156. In other embodiments, the trenches 158 may be formed using a conventional pitch-doubling process, by techniques known in the art.

FIG. 9 shows the semiconductor structure 140 after depositing a fill material 160 in the trenches 158. While FIG. 9 shows trenches 158 extending through the back gate dielectric 126 , the back gate contact 124, and the amorphous silicon material 128, the channels 128 to be filled may be as shown in FIG. 8A. By way of non-limiting example, the fill material 160 may include a dielectric material such as an oxide material or a nitride material, and may be deposited using a chemical vapor deposition process or a spin-on dielectric process.

FIGS. 10-13 are cross-sectional views of the semiconductor structure 140 shown in FIG. 9, taken along section line 9-9, after a sacrificial mask material 162 has been deposited thereover and a plurality of openings 164 have been formed. The sacrificial mask material 162 may be formed over the semiconductive material 142 and the fill material (not shown) and the plurality of openings 164 may be formed by removing portions of the sacrificial mask material 162 and the semiconductive

material 142. Each of the plurality of openings 164 may be formed extending in the second direction Y. As a non-limiting example, the sacrificial mask material 162 may be formed from an amorphous silicon material or a dielectric material using a CVD process. By way of non-limiting example, the openings 164 may be formed by providing a photoresist material (not shown) over the sacrificial mask material 162 and removing portions of the photoresist material overlying regions of sacrificial mask material 162 and the semiconductive material 142 that are to be removed. An anisotropic etching process (e.g., a dry reactive ion or plasma etching process) may then be used to etch the regions of the sacrificial mask material 162 and the semiconductive material 142 exposed through the photoresist material to form openings 164 that expose regions of the sacrificial mask material 162. For example, if the sacrificial mask material 162 and the semiconductive material 142 are formed from polysilicon, a reactive ion etching process using a fluorine (Fl)-based gas may be performed to selectively remove the amorphous silicon material, forming the openings 164 between portions of the semiconductive material 142. As a non-limiting example, the openings 164 may be formed to have a dimension D1 of 0.5F and the remaining portions of the semiconductive material 142 may have a dimension D2 of 1.5F. Additionally, the back gates 123, as shown in FIG. 1, may be formed by removing a portion of each of the back gate dielectric 126, the back gate electrode 124 and the amorphous silicon material 128 after removing the semiconductive material 142 such that the openings 164 extend through each of these materials leaving the back gate 123 intact. After forming the openings 164, the remaining photoresist material may be removed using a conventional ashing process. The openings 164 may also be formed using a conventional pitch-doubling process, by techniques known in the art.

As shown in FIG. 11, another fill material 166 such as an oxide material or a nitride material may be deposited in the openings 164. By way of non-limiting example, the fill material 166 may be deposited using a CVD process, a PECVD process or spin-on dielectric process. Thus, the semiconductive material 142 is completely physically isolated from the surrounding environment.

As shown in FIG. 12, a portion of each of the sacrificial material 162 and the semiconductive material 142 may be removed to form the voids 110 in the semiconductive material 142. If the semiconductive material 142 is formed from a crystalline silicon

material, a plasma including a mixture of sulfur hexafluoride (SF_6) gas, oxygen gas and helium (He) gas, or a mixture of sulfur hexafluoride gas and trifluoromethane (CHF_3) gas, may be introduced to the semiconductor structure 140 to form the voids 110. FIG. 11 depicts the voids 110 as having a u-shaped profile; however, voids having various other profiles may also be formed, as will be recognized by one of ordinary skill in the art.

FIG. 13 shows the semiconductor structure 140 after the buried gate electrodes 132 have been formed in each of the voids 110. As a non-limiting example, a CMP process may be used to remove portions of the fill material 166 and the sacrificial material 162 so that an upper surface 168 of the semiconductor structure 140 is substantially planar. The buried gate electrodes 132 may be formed from a conductive material such as, tungsten, titanium nitride or tantalum nitride, and may be deposited using a conventional CVD process, PVD process or ALD process. By way of non-limiting example, the conductive material may be formed over the semiconductor structure 140 and removed after deposition using a conventional CMP process, RIE process or wet etching process to form the buried gate electrodes 132. The buried gate dielectric 134 may be deposited over sidewalls of the semiconductive material 142 exposed in each of the voids 110 before forming the buried gate electrodes 132.

FIG. 14 shows the semiconductor structure 140 after forming the buried gate electrodes 132 in the voids 110 and another fill material 163 thereover. As shown in FIG. 14, source regions 112 and drain regions 114 may be formed in exposed regions of the pillars 108 of the volume of semiconductive material 102. The source regions 112 and drain regions 114 may include a silicon material that is doped with an n-type dopant, such as phosphorous or arsenic, (i.e., n-type silicon material). Exposed portions of the semiconductive material 142 may be doped using conventional methods, such as an ion implantation process or plasma ion process or a high temperature diffusion process. The source regions 112 and the drain regions 114 may be spaced apart from the back gate electrode 124 by the semiconductive material 142. As another example, a thin film of a n-type material (not shown) may be deposited over surfaces of the semiconductor structure 140 and a thermal anneal may be performed during which n-type dopants migrate into the semiconductive material 142 to form n-type silicon for the source regions 112 and drain regions 114. The source regions 112 and drain regions 114 may, optionally, be formed before forming the buried gate electrodes 132.

Referring back to FIGS. 1-3, after forming the source regions 112 and the drain regions 114, the common source lines 116 may be formed over the source regions 112 aligned in each of the rows and the bit lines 118 may be formed over the drain regions 114 aligned in each of the columns. In some embodiments, the common source lines 116 and the bit lines 118 may be formed by depositing a conductive reactive material over the semiconductor structure 100, 101 or 103 and pattering the conductive material to form substantially straight and substantially parallel conductive lines. For example, the common source lines 116 may be formed in the direction X, each of the common sources lines 116 disposed above and substantially parallel to one of the buried gate electrodes 132. The bit lines 118 may be formed extending in the direction Y. Optionally, the contact plug 119 may be formed on at least one of the drain regions 114 and the source regions 112 to elevate that contact before forming the associated common source line 116 or bit line 118. For example, the contact plug 119 may be formed by depositing and patterning a doped amorphous silicon material. Optionally, the contact plug 119 may be replaced by a metal material, such as titanium nitride/tungsten, or the contact plug may be filled with the conductive reactive material during formation of the conductive lines.

FIG. 15 is a perspective view illustrating another embodiment of a floating body cell structure 200 that includes a plurality of floating body cells 104, the details of forming such will be described in detail. For the purposes of illustrating the floating body cells 104, a portion of the gate 170 has been removed, as shown in broken lines. In some embodiments, the floating body cell structure 200 may be used to form a vertical multi-gate floating body cell device. Each floating body cell 104 in the floating body cell structure 200 may include a floating body cell 104 formed from a volume of semiconductive material that includes a channel region 106 extending between pillars 108, which are separated by a void 110, such as, a u-shaped trench, as described with respect to FIGS. 1-3. The source regions 112 and the drain regions 114 may be formed in the upper regions of the pillars 108 and may, respectively, be electrically coupled to an access line, such as common source line 116 and a data/sense line, such as bit line 118. By way of non-limiting example, the common source line 116 and the bit line 118 may, respectively, be formed directly on the source regions 112 and the drain regions 114, as shown in FIG. 18. Additionally, a contact plug 119 may be disposed between the source regions 112 and the associated common source line 116 to elevate the contact or between the drain regions 114 and the associated bit line 118.

The floating body cells 104 may be arranged as described with respect to FIGS. 1-3, wherein the floating body cells 104 are aligned in a plurality of rows in the first direction X and the plurality of columns in the second direction Y substantially perpendicular to the first direction X. FIG. 4 shows the back gate 123 as a local back gate disposed under rows of floating body cells 104 and extending in a direction parallel to floating body cells 104. The sidewalls of the back gate 123 are shown as being continuous and aligned with those of the floating body cells 104. In other embodiments, the back gate 123 may be configured as described with respect to FIGS. 2 and 3.

At least one conductive element 170 may be disposed on opposite vertical surfaces (i.e., sidewalls) of each of the floating body cells 104. For the ease of description, the conductive element 170 is hereinafter referred to as gate 170. Another dielectric material 172 may be disposed between the gate 170 and the sidewalls of the floating body cells 104. For the ease of description, the dielectric material 172 is hereinafter referred to as gate dielectric 172. Each of the floating body cells 104 of the floating body cell structure 200 may be electrically coupled to the back gate 123 and the gates 170 disposed on two sidewalls of the floating body cells 104 so that the floating body cell 104 includes three gates, or may be electrically coupled to the back gate 123 and the gate 170 disposed on a single sidewall of the floating body cells 104 so that the floating body cell 104 includes two gates. Electromagnetic fields emanating from the gates 170 may establish a channel through the associated floating body 104, which enables a current to flow from the source region 112 to the drain region 114.

FIGS. 16-20 illustrate embodiments of a method of forming the floating body cell structure 200 shown in FIG. 15. Referring to FIG. 16, a semiconductor structure 240 that includes an array of floating body cells 104, each including a volume of semiconductive material 102 disposed on the back gate 123 may be formed using methods such as those described with respect to FIGS. 4-12. The back gate 123 may include back gate dielectric 126, back gate electrode 124 and amorphous silicon material 128 and may be disposed on an electrically insulative material 130 overlying a wafer (not shown). As previously described, other logic elements (not shown), such as a complementary metal oxide semiconductor structure (CMOS) device, may be formed in or on the wafer. Although the trenches 158 are illustrated as terminating within the electrically insulative material 130, the trenches 158 may, optionally, be formed to terminate on the back gate dielectric 126, such as

those described with respect to FIG. 8A.

FIGS. 17A1-17B2 are cross-sectional views of the semiconductor structure 140 shown in FIG. 16, taken along section line 16-16. After forming the trenches 158, the gates 170 may be formed on sidewalls of the floating body cells 104, as described with respect to FIGS. 17A1-17B2. As shown in FIG. 17A1, a gate dielectric material 172 and a conductive material 174 may be formed over semiconductor structure 240. By way of non-limiting example, the gate dielectric material 172 may be an oxide material, a nitride material or a high k dielectric material formed using, for example, a chemical vapor deposition process or a thermal oxidation process. For example, if the gate dielectric material 172 is silicon dioxide, the semiconductor structure 240 may be exposed to an oxygen gas at a temperature of from about 900°C to about 1175°C to form the silicon dioxide on sidewalls of the floating body cells 104. The conductive material 174 may then be formed over the gate dielectric material 172. As a non-limiting example, the conductive material 174 may be formed from titanium nitride, tantalum nitride or tungsten and may be deposited using a chemical vapor deposition process. Referring to FIG. 17A2, an anisotropic dry etching process or a wet etching process may be performed to remove portions of the conductive material 174 and the gate dielectric material 172 to form the gates 170.

In other embodiments, the gates 170 may be formed on the sidewalls of the floating body cells 104 as shown with respect to FIGS. 17B1 and 17B2. Referring to FIG. 17B1, after forming the gate dielectric material 172 over the semiconductive material 142, the remaining portions of the trenches 158 between regions of the semiconductive material 142 may be filled with the conductive material 174 and the conductive material 174 may be recessed back to a desired thickness. By way of non-limiting example, the conductive material 174 may be formed from titanium nitride, tantalum nitride or tungsten and may be deposited using a chemical vapor deposition process. Spacers 176 including a dielectric material may be formed on sidewalls of the gate dielectric material 172 above the conductive material 174 using a conventional spacer etching process. Referring to FIG. 17B2, an anisotropic etching process may be performed to remove a portion of the conductive material 174 to form the gates 170. After forming the gates 170, the spacers 176 may be removed using, for example, a conventional selective etching process.

FIGS. 18A and 18B are top down views of the semiconductor structure 240 shown in

FIGS. 17A2 and 17B2 illustrating the configuration of the gates 170. The gates 170 may be formed to electrically connect pluralities of the floating body cells 104 with one another. As a non-limiting example, the gates 170 may extend along the columns of floating body cells 104 in direction Y. As shown in FIG. 18A, each of the gates 170 may substantially circumscribe the plurality of floating body cells 104 in a single one of the columns, vertical surfaces (i.e., sidewalls) of each of the floating body cells 104 being contacted by the gate 170. Referring to FIG. 18B, another embodiment is shown wherein the gates 170 are configured in a comb-like structure extending along at least one of the rows in a direction X and terminating at or near an end thereof, each of the gates 170 being disposed on opposite sidewalls of the floating body cells 104 in the row. Contacts 178 may be electrically coupled to each of the gates 170, for example, at a terminal portion thereof, so that the gates 170 are independently connected. Accordingly, as shown in FIGS. 18A and 18B, the gates 170 may be configured to form single-gate, dual-gate and triple-gate floating body cells 104.

As shown in FIG. 19, after forming the gates 170, source regions 112 and drain regions 114 may be formed in the upper portion of the pillars 108 of floating body cells 104 by exposing the semiconductor structure 240 to an n-type dopant or a p-type dopant, as described with respect to FIG. 14. The common source lines 116 may then be formed over the source regions 112 of the floating body cells 104 and the bit lines 118 may be formed over the drain regions 114 of the floating body cells 104 to form the semiconductor structure 240 shown in FIG. 18. The common source lines 116 and bit lines 118 may be formed by depositing a conductive material and pattering the conductive material to form conductive lines extending in the first direction X, substantially perpendicular to the gates 170. Since the common source lines 116 and bit lines 118 are parallel to another, the common source lines 116 and bit lines 118 may be formed using a conventional damascene process. For example, a sacrificial dielectric material (not shown) may be deposited over the semiconductor structure 240 and a pattern of apertures may be formed therein in locations at which the common source lines 116 and bit lines 118 are to be formed using a conventional lithographic process. A conductive material may be deposited over the semiconductor structure 240 to fill the apertures and a chemical mechanical polishing process may be used to remove a portion of the conductive material overlying the dielectric material to form the common source lines 116 and bit lines 118. Optionally, a doped material (not shown) may be formed on at least one

of the source regions 112 and drain regions 114 before forming the associated common source line 116 or bit line 118.

FIGS. 20-22 are electrical circuit diagrams, each of which illustrates a floating body cell structure that includes a plurality of floating body cells, such as those described with respect to FIGS. 1-3 and 15. As shown in FIG. 20, the floating body cell structure 300 may include a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a global back gate 123, such as the back gate 123 shown in FIG. 2. The global back gate 123 and the gate 132 may each be operably coupled to a bias voltage enabling the floating body cells 104 associated with the global back gate 123 to be simultaneously biased.

FIG. 21 illustrates a floating body cell structure 400 including a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a local back gate 123. The local back gates 123 may have a comb-like configuration, such as that shown in FIG. 18B, to provide two distinct addresses for each of the local back gates 123.

FIG. 22 illustrates a floating body cell structure 500 including a plurality of floating body cells 104, each of which is electrically coupled to a gate 132, a bit line 118 and a local back gate 123, such as the back gates 123 shown in FIGS. 2 and 15. Each of the local back gates 123 may be operably coupled to a bias voltage that may be used to individually bias each of the back gates 123.

It should be noted that, during the various stages of fabrication, the floating body cell structures 101, 102 and 103, respectively shown in FIGS. 1 through 3, may be integrated or vertically stacked with other semiconductor structures having a similar structure or with a memory element or device, such as a CMOS device. For example, the CMOS device may be formed over or beneath one of the floating body cell structures 101, 102 or 103 to form a multi-level semiconductor structure, which provides a substantially reduced dics size. The floating body cell structures 101, 102 and 103 may be stacked over another floating body cell structure, memory or logic using, for example, a modification of the so-called SMART-CUT® layer transfer technology as described with respect to FIGS. 4-6.

FIG. 23 illustrates a simplified block diagram of an electronic system 2300 implemented according to one or more embodiments described herein. The electronic system 2300 includes at least one input device 2302, at least one output device 2304, a

memory access device, such as one or more processors 2306, such as a system-on-chip (SOC), a central processing unit (CPU), processors and the like that may, and one or more memory devices 2308. The memory devices 2308 include at least one embodiment of the devices or methods described herein. The electronic system 2300 may be part of a number of computing, processing, and consumer products. As non-limiting examples, some of these products may include personal computers, handheld devices, cameras, phones, wireless devices, displays, chip sets, set top boxes, games, and vehicles.

CONCLUSION

In some embodiments, the present invention includes floating body cell structures, devices including such structures and method for forming such structures. The floating body cell structures may include a back gate, at least one floating body and another gate associated with the at least one floating body. The at least one floating body may include a semiconductive material and may extend from the back gate to a source region and a drain region. The source region and the drain region may be spaced apart from the back gate by the at least one floating body. The at least one floating body may include a void in the semiconductive material, each of the source region and the drain region disposed opposite the back gate. The another gate may be disposed within the void in the at least one floating body to form a double-gate floating body cell structure or may be disposed on at least one surface of the at least one floating body to form a triple-gate floating body cell structure. A gate dielectric may be disposed between the back gate and the at least one floating body and an amorphous silicon material underlying the back gate and disposed over a wafer. The back gate may be a local back gate comprising sidewalls continuous and aligned with sidewalls of the at least one floating body or a global back gate in which a plurality of floating body cells are disposed in an array. The floating body cell structure may further include a bit line electrically coupled to the back gate and operably coupled to a bias voltage for independently biasing the back gate. The floating body cell structure may further include a common source line electrically coupling the source region of the at least one floating body cell to a source region of at least another floating body and a bit line electrically coupling the drain region of the at least one floating body cell to a drain region of the at least another floating body.

In additional embodiments, the present invention includes a floating body cell device

that includes a plurality of floating bodies, each comprising a semiconductive material and extending from a back gate to a source region and a drain region and another gate associated with the plurality of floating bodies and operably coupled to a voltage source and a common source line electrically coupling the source regions of the plurality of floating bodies and a bit line electrically coupling the drain regions of the plurality of floating bodies. The device may be integrated in at least one of a dynamic random access memory, a zero capacitor random access memory, a central processing unit, a system-on-a-chip and embedded dynamic random access memory integrated therewith. The plurality of floating bodies may be aligned in a first direction to form a plurality of rows and a second direction substantially perpendicular to the first direction to form a plurality of columns.

In yet further embodiments, a floating body cell device includes a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, at least one back gate associated with the plurality of the floating bodies and at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source. Each of the floating bodies of the plurality of floating bodies may include a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region. The at least one back gate may include a conductive material disposed over an amorphous silicon material on an electrically insulative material. The at least another gate may include a conductive material disposed on each of the plurality of floating bodies that may extend, for example, in the first direction, electrically coupling the plurality of floating bodies in at least one of the plurality of rows. The at least another gate may include a conductive material disposed within the u-shaped trench and, for example, may extend in the second direction, electrically coupling the plurality of floating bodies in at least one of the plurality of columns. The at least one back gate may be configured to be biased independent of the another gate. The floating body cell structure may be disposed over and integrated with a memory device, such as a CMOS device, or may be vertically stacked in a number of tiers to increase density.

In yet further embodiments, the present invention includes methods of forming a floating body cell device that include forming a base comprising a semiconductive material, a dielectric material, a gate material, and an amorphous silicon material overlying a wafer,

removing a portion of the semiconductive material to form a plurality of floating bodies protruding from a surface of the base, removing another portion of the semiconductive material to form a void in each of the plurality of floating bodies, exposing the plurality of floating bodies to at least one dopant to form a source region and a drain region in upper regions of each of the plurality of floating bodies and forming a gate associated with at least one of the plurality of floating bodies. The base may be formed by forming a donor wafer comprising a dielectric material, a gate material and an amorphous silicon material overlying a crystalline silicon wafer, implanting ions a predetermined depth into the crystalline silicon wafer, attaching the amorphous silicon material of the donor wafer to an electrically insulative material overlying a handle wafer; and separating a portion of the donor wafer to leave a portion of the crystalline silicon wafer so that the dielectric material, the gate material, and the amorphous silicon material overlying a surface of the electrically insulative material of the handle wafer.

In yet further embodiments, the present invention includes a system that includes at least one memory device and at least one floating body cell device operably coupled to the at least one memory device. The at least one floating body cell device may include an array of floating bodies, each of which includes a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region, at least one back gate associated with the array of the floating bodies and at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source. The system may include at least one of a central processing unit and a system-on-a-chip. The at least one memory device may include at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory. The at least one memory device and the at least one floating body cell device may be superposed with one another within the system.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the scope of the invention as defined by the following appended claims and their legal equivalents.

What is claimed is:

1. A floating body cell structure, comprising:

a back gate comprising a conductive metal compound; at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region; and another gate associated with the at least one floating body.

2. The floating body cell structure of claim 1, wherein the source region and the drain region are spaced apart from the back gate by the at least one floating body.

3. The floating body cell structure of claim 1, wherein the at least one floating body comprises a void in the semiconductive material, each of the source region and the drain region disposed on opposite sides of the void.

4. The floating body cell structure of claim 3, wherein the another gate is disposed within the void in the at least one floating body.

5. The floating body cell structure of claim 1, wherein the another gate is disposed on at least one surface of the at least one floating body to form a triple-gate floating body cell structure.

6. The floating body cell structure of claim 1, wherein the at least one floating body comprises a plurality of floating bodies disposed on a single back gate in an array.

7. The floating body cell structure of claim 1, further comprising a common source line electrically coupling the source region of the at least one floating body cell to a source region of at least another floating body and a bit line electrically coupling the drain region of the at least one floating body cell to a drain region of the at least another floating body.

8. The floating body cell structure of claim 1 comprising a dielectric between the conductive metal compound and the floating body.

9. The floating body cell structure of claim 8 comprising metal between the dielectric and the floating body.

10. The floating body cell structure of claim 9 comprising a doped region between the metal and the floating body.

11. A floating body cell structure, comprising:

a back gate, the back gate comprising a local back gate comprising sidewalls continuous and aligned with sidewalls of the at least one floating body;

at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region; and

another gate associated with the at least one floating body.

12. The floating body cell structure of claim 11 wherein the another gate has sidewalls, the continuous and aligned sidewalls of the local back gate and at least one floating body being parallel the another gate sidewalls.

13. The floating body cell structure of claim 11 wherein the another gate has sidewalls, the continuous and aligned sidewalls of the local back gate and at least one floating body being perpendicular the another gate sidewalls.

14. A floating body cell structure, comprising:

a back gate;

at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region;

another gate associated with the at least one floating body; and

a bit line operably coupled to a bias voltage for independently biasing the back gate.

15. A floating body cell device, comprising:

a back gate comprising a conductive metal compound;

a plurality of floating bodies, each comprising a semiconductive material and extending from the back gate to a source region and a drain region;

another gate associated with the plurality of floating bodies and operably coupled to a voltage source; and a common source line electrically coupling the source regions of the plurality of floating bodies and a bit line electrically coupling the drain regions of the plurality of floating bodies.

16. The floating body cell device of claim 15, further comprising at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory integrated therewith.

17. The floating body cell device of claim 15, wherein the plurality of floating bodies are aligned in a first direction to form a plurality of rows and a second direction substantially perpendicular to the first

direction to form a plurality of columns.

18. A floating body cell device, comprising:

a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, each floating body comprising:

a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate comprising a conductive metal compound associated with the plurality of the floating bodies; and

at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source.

19. The floating body cell device of claim 18, wherein the at least another gate comprises a conductive material disposed on each of the plurality of floating bodies.

20. The floating body cell device of claim 19, wherein the conductive material extends in the first direction, electrically coupling the plurality of floating bodies in at least one of the plurality of rows.

21. The floating body cell device of claim 18, wherein the at least another gate comprises a conductive material disposed within the u-shaped trench.

22. The floating body cell device of claim 21, wherein the conductive material extends in the second direction, electrically coupling the plurality of floating bodies in at least one of the plurality of columns.

23. The floating body cell device of claim 18, wherein the at least one back gate is configured to be biased independent of the at least another gate.

24. A floating body cell device, comprising:

a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, each floating body comprising:

a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate associated with the plurality of the floating bodies, the at least one back gate comprising a conductive material disposed over an amorphous silicon material on an electrically

insulative material; and at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source.

25. A floating body cell device, comprising:

a plurality of floating bodies aligned in a first direction to form a plurality of rows and aligned in a second direction substantially perpendicular to the first direction to form a plurality of columns, each floating body comprising: a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate associated with the plurality of the floating bodies;

at least another gate associated with the plurality of floating bodies and operably coupled to a voltage source; and the floating body cell being vertically stacked with at least one other logic device.

26. A system, comprising:

at least one memory device; and

at least one floating body cell device operably coupled to the at least one memory device and comprising:

an array of floating bodies, each floating body of the array comprising a volume of semiconductive material having pillars extending from a base portion thereof and separated by a u-shaped trench, an upper portion of each of the pillars comprising a doped region;

at least one back gate comprising a conductive metal compound associated with the array of floating bodies; and at least another gate associated with the array of floating bodies and operably coupled to a voltage source.

27. The system of claim 26, wherein the system comprises at least one of a central processing unit and a system-on-a-chip.

28. The system of claim 26, wherein the at least one memory device comprises at least one of a dynamic random access memory, a zero capacitor random access memory, and an embedded dynamic random access memory.

29. The system of claim 26, wherein the at least one memory device and the at least one floating body cell device are superposed with one another.

30. The system of claim 26, wherein the array of floating bodies includes a plurality of floating bodies aligned in a first direction and aligned in a second direction substantially perpendicular the first

direction.

31. A floating body cell structure, comprising: a dielectric;

amorphous silicon over and contacting the dielectric;

a back gate over and contacting the amorphous silicon; at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region; and another gate associated with the at least one floating body.

32. The floating body cell structure of claim 31 comprising a dielectric between the conductive metal compound and the floating body.

33. The floating body cell structure of claim 32 comprising metal between the dielectric and the floating body.

34. The floating body cell structure of claim 33 comprising a doped region between the metal and the floating body.

35. A floating body cell structure, comprising: a back gate;

at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region;

a dielectric between the back gate and the floating body; metal between the dielectric and the floating body; and another gate associated with the at least one floating body.

36. The floating body cell structure of claim 35 comprising a doped region between the metal and the floating body.

37. A floating body cell structure, comprising:

a back gate;

at least one floating body comprising a semiconductive material and extending from the back gate to a source region and a drain region; and

another gate associated with the at least one floating body, the another gate being disposed on at least one surface of the at least one floating body to form a triple-gate floating body cell structure.