

WHAT IS CLAIMED IS:

1. A vertical memory device, comprising:

a substrate including a cell array region and a staircase region at least partially surrounding the cell array region;

a plurality of gate electrodes spaced apart from each other in each of first and third directions within the cell array region and the staircase region of the substrate, wherein each of the plurality of gate electrodes extends in a second direction, wherein the first direction is substantially perpendicular to an upper surface of the substrate, wherein the third direction is substantially parallel to the upper surface of the substrate, and wherein the second direction is substantially parallel to the upper surface of the substrate and crosses the third direction;

a channel extending in the first direction within the cell array region of the substrate, wherein the channel extends through at least one of the plurality of gate electrodes; and

a mold disposed adjacent to a first stair structure in the third direction within the staircase region, the mold contacting a sidewall of the first stair structure,

wherein end portions in the second direction of the plurality of gate electrodes form the first stair structure on the staircase region of the substrate,

wherein the first stair structure includes a plurality of first steps, a second step, and a third step, sequentially disposed in the third direction, and

wherein each of the plurality of first steps has a first length in the third direction, wherein the second step has a second length in the third direction that is greater than the first length, and wherein the third step has a third length in the third direction that is greater than the second length, and

wherein the mold includes first and second insulation patterns alternately and

repeatedly stacked in the first direction.

2. The vertical memory device of claim 1, wherein each of the plurality of first steps, the second step, and the third step are sequentially arranged in the first direction from a lowermost level toward an uppermost level.

3. The vertical memory device of claim 1 or claim 2, wherein the first stair structure includes the plurality of first steps, the second step, the third step, and a fourth step, sequentially arranged in the third direction, and

wherein a fourth length of the fourth step in the third direction is greater than the third length.

4. The vertical memory device of any one of claims 1 to 3, wherein the first stair structure includes three first steps.

5. The vertical memory device of claim 4, wherein a plurality of first stair structures, including the first stair structure, is disposed in the second direction at different levels, respectively.

6. The vertical memory device of any one of claims 1 to 5, further comprising a plurality of first contact plugs, a second contact plug, and a third contact plug disposed on upper surfaces of a corresponding one of the plurality of first steps, the second step, and the third step, respectively.

7. The vertical memory device of claim 6, wherein a distance between the second and third contact plugs in the third direction is greater than a distance between ones

of the plurality of first contact plugs in the third direction, the ones of the plurality of first contact plugs being adjacent to each other in the third direction.

8. The vertical memory device of claim 7, wherein a distance between the second contact plug and one of the plurality of first contact plugs adjacent thereto is substantially the same as the distance between the ones of the plurality of first contact plugs.

9. The vertical memory device of claim 1, wherein each of the first insulation patterns includes a nitride and has a lower surface that is substantially coplanar with a lower surface of a corresponding element of the first to third steps.

10. The vertical memory device of claim 9, wherein an upper surface of each of the first insulation patterns is lower than an upper surface of the corresponding element of the first to third steps.

11. The vertical memory device of any one of claims 1 to 10, further comprising a second stair structure, wherein the first and second stair structures are symmetric with respect to the mold in the third direction.

12. The vertical memory device of any one of claims 1 to 11, further comprising a base pattern disposed on the substrate,

wherein the plurality of gate electrodes, the channel, and the mold are formed on the base pattern.

13. The vertical memory device of claim 12, further comprising:

a circuit pattern disposed between the substrate and the base pattern; and

a through via extending through the mold and the base pattern to be electrically connected to the circuit pattern.

14. A vertical memory device, comprising:

a substrate including a cell array region and a staircase region at least partially surrounding the cell array region;

a plurality of gate electrodes spaced apart from each other in each of first and third directions within the cell array region and the staircase region of the substrate, wherein each of the plurality of gate electrodes extends in a second direction, wherein the first direction is substantially perpendicular to an upper surface of the substrate, wherein the third direction is substantially parallel to the upper surface of the substrate, and wherein the second direction is substantially parallel to the upper surface of the substrate and crosses the third direction; and

a channel extending in the first direction within the cell array region of the substrate, wherein the channel extends through at least one of the plurality of gate electrodes,

wherein end portions in the second direction of the plurality of gate electrodes form first and second stair structures on the staircase region of the substrate, wherein each of the first and second stair structures has steps, and wherein the first and second stair structures are symmetric with each other in the third direction,

wherein a mold is disposed between the first and second stair structures within the staircase region, wherein the mold contacts sidewalls of the first and second stair structures and includes an insulating material, and

wherein the mold includes first and second insulation patterns alternately and repeatedly stacked in the first direction.

15. The vertical memory device of claim 14, wherein the mold extends in the second direction on the staircase region of the substrate and contacts sidewalls of the plurality of gate electrodes in the second direction.

16. The vertical memory device of claim 14 or claim 15,
wherein each of the first insulation patterns has a lower surface that is substantially coplanar with a lower surface of a corresponding gate electrode of the plurality of gate electrodes, in the second direction, and substantially coplanar with a lower surface of a corresponding step of the steps, in the third direction.

17. A vertical memory device, comprising:
a substrate including a cell array region and a staircase region at least partially surrounding the cell array region;
a plurality of gate electrodes spaced apart from each other in each of first and third directions within the cell array region and the staircase region of the substrate, wherein each of the plurality of gate electrodes extends in a second direction, wherein the first direction is substantially perpendicular to an upper surface of the substrate, wherein the third direction is substantially parallel to the upper surface of the substrate, and wherein the second direction is substantially parallel to the upper surface of the substrate and crosses the third direction; and
a channel extending in the first direction within the cell array region of the substrate, wherein the channel extends through at least one of the plurality of gate electrodes,
wherein end portions in the second direction of the plurality of gate electrodes forms a stair structure on the staircase region of the substrate,

wherein the stair structure includes first to sixth step layers sequentially stacked in the first direction, wherein the first to sixth step layers have lengths in the third direction gradually decreasing from a lowermost one toward an uppermost one thereof,

wherein each of the first and second step layers includes end portions of four gate electrodes, of the plurality of gate electrodes, disposed in the third direction, wherein each of the third and fourth step layers includes end portions of three gate electrodes, of the plurality of gate electrodes, disposed in the third direction, wherein the fifth step layer includes end portions of two gate electrodes, of the plurality of gate electrodes, disposed in the third direction, and wherein the sixth step layer includes an end portion of one gate electrode of the plurality of gate electrodes,

wherein a mold is disposed adjacent to the stair structure in the third direction within the staircase region, the mold contacting a sidewall of the stair structure, and

wherein the mold includes first and second insulation patterns alternately and repeatedly stacked in the first direction.

18. The vertical memory device of claim 17, wherein the first to sixth step layers include first to sixth steps, respectively, not covered by upper step layers, and

wherein at least one of the first to sixth step layers has a length in the third direction that is different from those of other ones of the first to sixth step layers.