METHOD FOR REDUCING THE TRAP DENSITY IN A SEMICONDUCTOR WAFER

FIELD OF THE INVENTION

The invention generally concerns the control of the trap interface density in a multilayer semiconductor wafer.

The invention can thus be used for controlling the trap interface density in SOI wafers – but it also applies to any kind of multilayer wafer made with materials selected from the semiconductor materials ("semiconductor wafers").

And the invention finds a particularly advantageous application in the control of the trap interface density in a multilayer semiconductor wafer obtained by a transfer method.

DEFINITIONS

It is specified that in this text the term « transfer method" refers to a method for manufacturing multilayer semiconductor wafers, and implying a transfer step during which :

- a top (or "donor") wafer is bonded on a base wafer (also called "handle", or "receiver" wafer),
- at least part of the top wafer remains with the base wafer after the bonding.

A transfer method can be carried out e.g. according to the following methods :

- the Smart-Cut™ method (it is specified that a general description of this method can be found e.g. in Jean-Pierre Colinge – "Silicon On Insulator Technologies « Materials to VLSI »", Kluwer Academic Publisher, 2nd edition),
- the ELTRAN™ method,

- etc...

The Dit is the parameter which characterizes the trap interface density – which is defined as the density of electrical traps located at an interface between two layers of a multilayer structure (e.g. the interface between the buried oxide layer – BOX – and the surface active layer of a SOI structure). In this text Dit and "trap interface density" are understood as equivalent.

This density is generally expressed in count of traps per ($eV.cm^2$) – i.e. in $\#/eV.cm^2$ – and typical values for the interface BOX/active layer in a SOI are 10^{12} $\#/eV.cm^2$. Dit can be measured using e.g. pseudo MOSFET measurement techniques.

The "active layer" of a multilayer semiconductor wafer is the layer in which components shall be created – this layer being generally electrically isolated from the rest of the wafer. The active layer is generally a surface layer of the wafer.

BACKGROUND OF THE INVENTION

Dit is an important parameter since it has an influence on the mobility of electrical carriers in the layers of the multilayer wafer. As an example, Dit at a BOX/active layer interface of a SOI has an influence on the carrier mobility of the active layer – the carrier mobility being in turn a parameter which influences the electrical performance of the wafer.

It is thus desired to control the value of the Dit at a given interface of a multilayer wafer (e.g. the BOX/active layer interface of a SOI wafer), in order to influence the electrical performance of the wafer (and the performance of the devices that will be formed on the wafer).

More precisely, in the perspective of increasing the mobility of electrical carriers in the active layer of a multilayer semiconductor wafer, it can be desired to minimize the value of the Dit at the interface between the active layer and the adjacent underlying layer in the wafer (it has been shown that a lower Dit at this interface is associated with a higher mobility).

In the case of a typical SOI wafer comprising an active layer (e.g. in Si) covering an insulating layer (e.g. an oxide layer), this would mean that it is desired to reduce the Dit at the interface between the active layer and the oxide layer,

It is specified that in this text we shall refer to "SOI-type wafers" as multilayer wafers comprising :

- a support layer (e.g. bulk Si for a classical SOI),
- an active layer located in the surface region of the wafer (e.g. a thin film of Si – but possibly other types of films such as SiGe, Ge, or others),
- and a buried insulating layer between these two layers (e.g. a buried oxide layer).

It can also be desired to reduce the variability of the values of the Dit among the multilayer wafers of a group of wafers – i.e. a group of wafers manufactured under the same conditions in a wafer manufacturing facility.

It is already known to carry out a low temperature thermal treatment on a SOI wafer in order to reduce Dit and its variability in the wafer. Such thermal treatment can be carried out at a temperature up to 600°C for a duration between 30 and 120 min. in an atmosphere which is neutral, or contains only a small amount of hydrogen (e.g. 2% H_2 in a N_2 or Ar atmosphere).

Such treatment is referred to as a "Forming Gas Anneal" (FGA). It is mentioned e.g. in the communication "Oxide charges induced by plasma activation for wafer bonding" – Scholberg-Henriksen and al. , Sensors and Actuators A 102 (2002), 99-105, Elsevier.

It is generally observed that when a FGA treatment is carried out on a wafer comprising more than one layer, such treatment allows a reduction of the Dit at the first interface located under the surface of the wafer ("interface being here understood as the delimitation between two adjacent layers).

In this respect, the above-mentioned article discloses a reduction of the Dit at the interface between a capping oxide layer which covers the surface of a bulk Si wafer, and the underlying bulk Si layer.

One could contemplate carrying out a FGA treatment for reducing the Dit at the interface between the active layer and its underlying layer in a SOI-type wafer (for a "classical" SOI this interface is defined between the active layer and the underlying oxide layer).

For that purpose one would not contemplate the option of performing the FGA treatment on the wafer when it is still covered by a capping oxide layer (it is reminded that such a capping layer is usually present over the surface of the wafer towards the end of the manufacturing process, and that this capping oxide layer is removed at the end of the process).

Indeed, the above-mentioned article teaches that a FGA carried out on a Si layer covered by a capping oxide reduces the Dit at the interface between the capping oxide and the underlying Si layer, and the expected result of a FGA carried out on a SOI-type structure still covered by its capping oxide would be a reduction of the Dit at the interface between the capping oxide layer and the underlying active layer (and not a reduction of the Dit at the interface between the active layer and the underlying layer – which is desired).

Moreover, during intermediate phases of manufacturing, a multilayer wafer is generally covered by a capping oxide layer having a thickness from 100 to 3000 angströms (e.g. 2000 angströms). And tests conducted by the applicant have shown that a FGA carried out on a SOI wafer covered with such oxide layer of 2000 angströms (FGA in a Ar atmosphere containing 2% H2, for 90 min. at 450°C) has no effect on the Dit at the interface between the active layer and the underlying buried oxide layer. Therefore, this option does in any case not appear as a solution.

The option which could then be contemplated would be to carry out a FGA treatment after all manufacturing steps have been carried out on the SOI-type wafer – including the steps of removing the capping oxide on the wafer.

But such treatment would mean adding another lengthy treatment at the end of the manufacturing process of the wafer, which is of course not desired.

Still another option that one could contemplate would be carrying out a FGA treatment during early stages of the manufacturing of a SOI-type wafer.

For example, such early FGA could be carried out on a "top" substrate to be used in a Smart-Cut™ method, before the bonding of the top substrate with a base substrate. It is reminded that a Smart-Cut™ method implies the bonding of a top substrate with a base substrate).

This could indeed allow reducing Dit at the interface between a layer of the top substrate which is to be used to make the active layer of the SOI-type wafer, and an adjacent insulating (e.g. oxide) layer which is to provide the buried insulating layer of the SOI-type wafer.

But Dit is a parameter which is temperature-sensitive, and the subsequent treatments which would then be applied to the wafer (bonding, transfer, stabilization, ...) would comprise high temperature treatments which would degrade the values of Dit obtained through the early FGA.

Thus, there is a need for a method which allows reducing the Dit and its variability in a multilayer wafer, without requiring a significant additional processing time of the wafer.

The goal of the invention is to fulfil this need.

In order to reach this goal, the invention proposes a method for reducing the trap density at an interface between an active layer of a multilayer semiconductor wafer and an insulating layer buried within said multilayer wafer under said active layer, said method comprising carrying out in a controlled atmosphere a high temperature thermal treatment to said multilayer wafer,

said thermal treatment comprising an oxidation phase carried out in a controlled atmosphere comprising at least an oxidizing species at an oxidation temperature, and resulting in a capping of the surface of said wafer with a capping oxide layer,

said method further comprising after said thermal treatment a deoxidation operation to remove said capping oxide layer created during said oxidation phase,

characterized in that during said thermal treatment and after said oxidation phase said controlled atmosphere is controlled so as to comprise in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired.

Preferred but non-limiting aspects of such a method are the following :

- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out immediately after said oxidation phase,
- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out as a high temperature treatment applied to said multilayer wafer and no other high temperature treatment is carried out afterwards on said multilayer wafer,
- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out before said deoxidation operation,
- said species which can migrate into the depth of said wafer is hydrogen and/or helium,
- said species which can migrate into the depth of said wafer is hydrogen,
- said final phase said controlled atmosphere is composed of at least 1% H_2 in a generally neutral atmosphere,

- said final phase said controlled atmosphere is composed of 4 % H_2 in a generally neutral atmosphere,
- said oxidizing species of said oxidation phase comprises oxygen,
- said oxidation temperature is between 800 and 1000°C,
- said oxidation temperature is 950°C,
- said oxidation temperature is selected so as to generate a capping oxide layer having a thickness between 1000 and 3000 angströms,
- said oxidation temperature is selected so as to generate a capping oxide layer having a thickness of 2000 angströms,
- said thermal treatment further comprises after said oxidation phase a stabilization phase comprising a thermal annealing carried out in a generally neutral atmosphere and during which a bonded interface of said multilayer wafer is stabilized,
- said thermal annealing of said stabilization phase is carried out at a temperature substantially greater than said oxidation temperature,
- said thermal annealing of said stabilization phase is carried out at a temperature between 950 and 1200°C,
- said thermal annealing of said stabilization phase is carried out at a temperature of 1100°C,
- said thermal annealing of said stabilization phase is carried out at a temperature substantially equal to said oxidation temperature,
- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during said stabilization phase,
- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during a ramp-down following said stabilization phase,

- said ramp-down ends with a boat-out temperature and no other high temperature treatment is carried out on said multilayer wafer before said deoxidation operation,

- said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during a ramp-down following said oxidation phase,

- said ramp-down ends with a boat-out temperature and no other high temperature treatment is carried out on said multilayer wafer before said deoxidation operation,

- said multilayer wafer has been obtained by a transfer method,

- said transfer method comprises implanting a donor substrate with at least one species in order to create in said donor substrate an embrittlement zone,

- said transfer method is a Smart-Cut™ type method,

- said multilayer wafer is a SOI,

- the boat out temperature is 450°C,

- the method is carried out on batches of multilayer wafers, and the boat out temperature can vary among the batches while obtaining a substantially constant value of the trap density for the wafers of all batches,

- for the batches, said boat-out temperatures can have the following values : 450 – 600 – 750°C,

- the active layer of said multilayer semiconductor wafer is a Si layer,

- the active layer of said multilayer semiconductor wafer is a strained Si layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, goals and advantages of the invention shall be apparent in the following description, made in reference to the drawing on which :

- Figure 1a – 1c are three graphs illustrating the temperature vs. time evolution during three respective thermal treatments carried out on a multilayer wafer according to three respective options for carrying out a method according to the invention,
- Figure 2 is a graph illustrating :
  - the Dit reduction obtained by a thermal treatment as mentioned above, by comparison with a thermal treatment carried out as it is already known, and
  - the stability of Dit values for treatments associated with different boat out temperatures.

DESCRIPTION OF PREFERRED EMBODIMENTS

General aspects

The invention is carried out on the basis of a high temperature thermal treatment for oxidizing the surface of a multilayer wafer made of semiconductor materials of the SOI-type, such as e.g. a SOI. This high temperature treatment thus comprises an oxidation phase.

And this thermal treatment can (optionally) further comprise a stabilization phase for stabilizing a bonded interface between two layers of the multilayer wafer. This bonded interface can in particular result from the bonding of two substrates in an earlier transfer method (e.g. a Smart-Cut™ type method – it is specified that a description of the general aspects of such method can be found e.g. in "Silicon-On-Insulator technology : Materials to VLSI, 2nd edition, Jean-Pierre Colinge, Kluwer Academic Publishers) for building the multilayer wafer.

In all cases, the invention is carried out as a "high temperature treatment" applied to the multilayer wafer. It is specified that in this description "high temperature treatment" of a wafer refers to a thermal

treatment comprising the exposure of said wafer to a temperature of at least 950°C.

The thermal treatment which comprises an oxidation phase creates on the surface of the multilayer wafer a capping oxide layer which has a thickness which is typically between 1000 and 3000 angströms (e.g. 2000 angströms).

And this thermal treatment shall be followed by a deoxidation operation in order to remove said capping oxide layer and produce a finished multilayer wafer. This deoxidation operation can comprise a chemical treatment (e.g. HF etching, ...) and/or other types of treatments (high temperature treatments being excluded for this deoxidation operation).

The multilayer wafer (which we will simply refer to as "the wafer") already comprises the layers that it will incorporate when it shall be finished. This wafer has been obtained by any method known in the art.

In particular, the wafer can have been obtained by a transfer method – which implies the bonding of at least a layer from a donor (or "top") substrate onto a receiving (or "base") substrate, thus creating a bonded interface.

Such transfer method can in particular be a method implying implanting a donor substrate with at least one species in order to create in said donor substrate an embrittlement zone. Such method can be e.g. a Smart-Cut™ type method.

The method according to the invention allows to reduce the trap density at an interface between an active layer of the wafer and an insulating layer buried within said multilayer wafer under said active layer.

The active layer is located in the surface region of the wafer. It can be made of Si, or in other materials (such as SiGe, Ge, ...). The material of this layer can be strained.

In this respect it is specified that the invention is not limited to applications on wafers such as Silicon On Insulator wafers, but concerns any kind of wafer comprising a thin active layer of material on a substrate and for which electrical properties have to be optimized.

And it is specified that the term "buried" insulating layer refers to a layer which is buried under the active layer of the wafer but which is not necessarily itself covering a support layer – even if this is the case for a wafer such as a SOI.

The buried insulating layer can be e.g. a buried oxide layer. It is located immediately under the active layer.

As mentioned above, the trap density at the interface is typically represented by the parameter Dit.

Controlled atmosphere

General aspects

For carrying out the high temperature thermal treatment, the wafer is placed in an annealing chamber. The atmosphere in this chamber is controlled – and as will be seen it is selectively controlled so as to respect different specifications during different phases of the thermal treatment.

More precisely, in the case of the invention during the thermal treatment and after the oxidation phase the controlled atmosphere is controlled so as to comprise in a generally neutral atmosphere at least a species whose ions can migrate into the depth of the wafer down to the interface where reduction of the trap density is desired (interface between the active layer and the buried insulating layer).

Practically speaking, the high temperature thermal treatment of the invention which is carried out on the wafers comprise :

- A starting phase comprising :
  - an entry step carried out at a boat in temperature (which is typically between 450 and 750°C - e.g. 600°C, and which is typically the same as the final boat out temperature), followed by
  - a first ramp-up to increase the temperature from the boat in temperature up to an oxidation temperature,

- An oxidation phase carried out at said oxidation temperature, resulting in a capping of said wafer with an oxide layer,
- Optionally, a stabilization phase after the oxidation phase. This stabilization phase is carried out at a stabilization temperature, either :
  - At a stabilization temperature substantially greater that the oxidation temperature (option 1 – the respective options shall be further described in reference to figures 1a-1c) – and in this case the stabilization phase begins with a temperature ramp-up from the oxidation temperature up to a stabilization temperature, or
  - At a stabilization temperature substantially equal to the oxidation temperature (option 2),
  - It is also possible that the thermal treatment comprises no stabilization phase (option 3).
- A final phase comprising :
  - a temperature ramp-down to bring temperature down to a boat out temperature,
  - an ending step carried out at a boat out temperature.

During the starting phase, the atmosphere is neutral (i.e. it is compose of a neutral gas such as N_2 or Ar).

The oxidation phase is typically carried out in a controlled atmosphere containing an oxidizing species such as oxygen, at an oxidation temperature between 800 and 1000°C (typically 950°C).

Such an oxidation phase generates a capping oxide layer of 1000 to 3000 angströms (e.g. 2000 angströms) on the surface of the wafer – and the temperature and the duration of this phase is adapted as a function of the thickness desired for the capping oxide.

The stabilization phase is typically carried out in a controlled atmosphere which is neutral. However, as will be further exposed this atmosphere can be controlled so as to contain a controlled proportion of a species whose ions can migrate down to the interface at which reduction of the trap density is desired.

Controlled atmosphere for reducing the Dit

Some details are provided herebelow concerning the control atmosphere with species whose ions can migrate down to the interface at which reduction of the trap density is desired (whatever the option selected for carrying out the invention).

Said species can be H and/or He. In a preferred embodiment, said species is hydrogen. And the proportion of e.g. hydrogen in the generally neutral atmosphere should be over 1%.

The generally neutral atmosphere in which such species are injected in a controlled proportion is typically composed of Ar and/or N_2.

Tests have been conducted with the injection in the controlled atmosphere of the thermal treatment of H2 in an N_2 atmosphere – thus forming a controlled atmosphere composed of 4 % H2 in N_2. Such tests have produced a significant reduction of the Dit at the interface between an active Si layer and the buried oxide layer of a SOI (this aspect shall be further commented in reference to figure 2).

This specific control of the atmosphere with a controlled proportion of species such as He or H_2 injected into a generally neutral atmosphere is carried out before the deoxidation operation. It could also be carried out immediately after the oxidation phase.

And it is furthermore preferably carried out as the last high temperature thermal treatment to be undergone by the wafer (since the Dit for which reduction has been obtained would otherwise risk being degraded by further high temperature treatments).

The controlled atmosphere such as described here-above shall simply be referred to as “controlled atmosphere” in the remainder of this text.

Description of three options

Three options for treating multilayer wafers – respectively illustrated by figures 1a to 1c – shall now be further described.

The above comments are applicable to each of these options.

Option 1

Figure 1a illustrates a first option for carrying out the method according to the invention.

In this option, the oxidation phase is followed by a stabilization phase, carried out at a temperature substantially greater that the oxidation temperature.

More precisely, the stabilization temperature is between 950 and 1200°C – a typical value being 1100°C.

The stabilization phase aims at stabilizing a bonded interface, as mentioned above. Such stabilization phase is known in the art as being carried out in a purely neutral atmosphere.

In the case of this option of the invention, this stabilization phase is associated to a specific control of the annealing atmosphere in the annealing chamber, with the above mentioned injection of species such as H_2 or He.

The controlled atmosphere is thus established :

- during the stabilization phase itself. In this case the controlled injection is preferably performed only once the stabilization temperature has been reached, and/or
- during the subsequent ramp-down. And if the controlled H_2 atmosphere is established only during the ramp-down (i.e. not during the oxidation), the injection of species such as H_2 or He shall be performed at the beginning of the ramp-down, when the temperature is still in the domain of the "high temperatures" – i.e. above 950°C, in order to have at least the beginning of the ramp-down under the

atmosphere containing a controlled amount of species such as H_2 or He.

Option 2

This option is illustrated in figure 1b.

In this option, the stabilization phase is carried out at a temperature which is substantially equal to the oxidation temperature. The atmosphere is purged from oxidants between the oxidation phase and the stabilization phase.

As for option 1 presented above, the stabilization phase is preferably carried out immediately after the oxidation phase.

In this option the oxidation phase is carried out at a temperature of at least 950°C – and it is also the case for the stabilization phase.

In this option, the beginning of the controlled injection of species such as H_2 or He is preferably performed during the stabilization phase, before the beginning of the ramp-down which follows it.

The controlled atmosphere can then be kept established during the ramp-down (with a purge of the controlled atmosphere before the actual end of the ramp-down in order to eliminate the species such as H_2 or He and to be able to safely open the annealing chamber).

Option 3

This option is illustrated in figure 1c.

In this option there is no stabilization phase after the oxidation phase.

This option can be selected if it is only desired to reduce the thickness of the wafer (the oxidation and the subsequent deoxidation correspond to a sacrificial oxidation), and if no stabilization of a bonded interface is sought.

The controlled injection of species such as H_2 or He in a generally neutral atmosphere is performed during the ramp-down which follows the oxidation phase. And here again the controlled atmosphere is established while the temperature is still in the range of high temperatures. This implies in particular that the oxidation phase is carried out at an oxidation temperature of at least 950°C.

The atmosphere of the annealing chamber must be purged from oxygen before the injection of species such as H_2 or He.

And this injection is performed as early as possible during the ramp-down, in order to have the controlled atmosphere produce its effects at temperatures as high as possible.

Comment on all options

In all embodiments of the invention, it is important to expose the wafer (which in all embodiments has its active layer covered by a capping oxide layer resulting from the oxidation phase) to the controlled atmosphere at temperatures which are in the range of "high temperatures" (i.e. at least 950°C).

The applicant has indeed observed that such exposure allowed to reduce the Dit not only at the first interface encountered in the thickness of a wafer such as a SOI (this first interface being the interface between the capping oxide layer and the active layer it temporarily covers), but also at the interface between the active layer and the underlying oxide layer of the wafer.

This effect can be explained as follows :

- under "high temperatures" the species such as H_2 or He of the controlled atmosphere have enough energy to penetrate the thickness of the wafer down to the desired interface, i.e. the interface between the active layer and the underlying insulating layer,
- while without such specific exposure of the wafer the species would – as in the known processes – not penetrate the thickness of the wafer

deeper than the first interface encountered – i.e. the interface between the capping oxide layer and the underlying active layer).

And in the case where the controlled atmosphere is established only during a ramp-down following a stabilization phase or an oxidation phase, the controlled atmosphere must be established while the temperature is still in the range of high temperatures (as defined in this text).

Effect of the treatment

Reduction of Dit and its variability

Figure 2 shows the reduction of Dit obtained by a treatment as described above, on a SOI wafer obtained by a method based on the Smart-Cut™ technology.

This figure shows the value of the Dit, measured on three groups of identical wafers which have been processed under the same conditions (the three groups corresponding respectively to "run1", "run2" and "run3"), except for the boat-out temperatures which were different for the three runs :

- the boat out temperature was 450°C for the wafers of run1,
- the boat out temperature was 600°C for the wafers of run2,

the boat out temperature was 750°C for the wafers of run3.Figure 2 comprises two curves, each curve being defined by three point (a point for each group or "run") :

- an upper curve shows the Dit measured on wafers having undergone a stabilizing treatment with a purely neutral atmosphere in its final phase, as it is know. This treatment comprised a starting phase followed by an oxidation phase at 950°C and a stabilizing phase at a temperature of about 1100°C,
- a lower curve shows the Dit measured on wafers having undergone a treatment which differed from the stabilizing treatment of the upper

curve only by the control of the atmosphere in association with the stabilizing phase (4% H_2 in a neutral atmosphere such as Ar during and/or immediately after this phase, in high temperatures).

The Dit measurements have been carried out in the same manner for the wafers of the two curves.

This figure shows a significant decrease of the Dit (reduction of about 50%).

It also show a dramatic decrease of the variability of Dit.

The invention allows a significant decrease of the Dit (e.g. at the BOX/active layer interface of a SOI), and of its variability. And this is obtained without requiring any additional processing time, since the stabilizing treatment is required for stabilizing the bonded interface between layers of the wafer.

The invention therefore provides the advantages of FGA treatments, without requiring additional time.

And it is to be noted that using an atmosphere with a species such as hydrogen on a wafer which is covered by a capping oxide layer, in order to decrease Dit, goes against the teachings of the prior art since it has been demonstrated that carrying out a treatment such as a classical FGA on a wafer covered by such a capping oxide layer (of 2000 angströms, as it is the case for the wafers having undergone the oxidation phase described above) has no effect on Dit.

Specific comment on the stability of the results vs. Boat-out temperature

The results of figure 2 furthermore show another interesting aspect resulting from the invention.

The three runs which correspond to the three groups illustrated on this figure indeed correspond to three values of the boat out temperature which are different, as mentioned above.

The resulting values of Dit nevertheless remains substantially equal for the three groups.

This corresponds to a very advantageous robustness of the method according to the invention, since it allows carrying out the invention with a significant freedom on the boat out temperature, while keeping the benefit of a value of Dit which is not only reduced but also stable despite the variability of the boat out temperatures.

It is thus possible to process batches of wafers such as mentioned above according to the invention with substantial modifications of the boat out temperature, and still obtain remarkably homogeneous values of the Dit at the interface (active layer / buried insulating layer) of the processed wafers whatever the batch.

And in this respect it is to be noted that the invention allows to have low values of boat-out temperatures, without degrading the Dit at the interface between the active layer and the underlying insulating layer of a multilayer wafer.

This is an advantage since it has been observed on wafers which were not treated according to the invention that lower valued of boat-out temperatures were much more likely to generate an increased Dit at this interface.

Additional comment on the wafers

As mentioned above, the invention is not limited to the treatment of SOI wafers – even if such wafers correspond to an application of the invention.

As an example, another particular application of the invention is the treatment of wafers of the type "strained Silicon On Insulator" (sSOI).

sSOI wafers comprise a thin strained Si layer (having typically a thickness between 100 and 600 angströms), directly on a buried insulating layer, a support layer being under said buried insulating layer.

Because of the very thin thickness of the strained layer, it is generally not possible to oxidize it in order to perform a high temperature treatment such as a stabilization of a bonding interface.

In order to build such a wafer, a solution is therefore to first deposit a capping oxide layer on the surface layer of a sSOI multilayer wafer which comprises under this surface layer (which is in strained Si) a buried insulating layer.

Such deposition of a capping oxide layer can be made e.g. by TEOS deposition. The capping oxide layer is e.g. a layer of SiO2 having a thickness between 100 and 3000 angströms.

And it is furthermore possible to form an extremely thin thermal oxide layer (native oxide layer or only slightly thicker) on the strained layer before depositing the thicker capping oxide layer.

Once the strained layer has been covered by a capping oxide layer, it is protected from high temperatures and can undergo the method according to the invention.

CLAIMS

1. Method for reducing the trap density at an interface between an active layer of a multilayer semiconductor wafer and an insulating layer buried within said multilayer wafer under said active layer, said method comprising carrying out in a controlled atmosphere a high temperature thermal treatment to said multilayer wafer,

said thermal treatment comprising an oxidation phase carried out in a controlled atmosphere comprising at least an oxidizing species at an oxidation temperature, and resulting in a capping of the surface of said wafer with a capping oxide layer,

said method further comprising after said thermal treatment a deoxidation operation to remove said capping oxide layer created during said oxidation phase,

characterized in that during said thermal treatment and after said oxidation phase said controlled atmosphere is controlled so as to comprise in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired.

2. Method according to the preceding claim characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out immediately after said oxidation phase.

3. Method according to any preceding claim characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out as a high temperature treatment applied to said multilayer wafer and no other high temperature treatment is carried out afterwards on said multilayer wafer.

4. Method according to any preceding claim characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out before said deoxidation operation.

5. Method according to any preceding claim characterized in that said species which can migrate into the depth of said wafer is hydrogen and/or helium.

6. Method according to the preceding claim characterized in that said species which can migrate into the depth of said wafer is hydrogen.

7. Method according to the preceding claim characterized in that during said final phase said controlled atmosphere is composed of at least 1% H_2 in a generally neutral atmosphere.

8. Method according to the preceding claim characterized in that during said final phase said controlled atmosphere is composed of 4 % H_2 in a generally neutral atmosphere.

9. Method according to any preceding claim characterized in that said oxidizing species of said oxidation phase comprises oxygen.

10. Method according to any preceding claim characterized in that said oxidation temperature is between 800 and 1000°C.

11. Method according to the preceding claim characterized in that during said oxidation temperature is 950°C.

12. Method according to any preceding claim characterized in that said oxidation temperature is selected so as to generate a capping oxide layer having a thickness between 1000 and 3000 angströms.

13. Method according to the preceding claim characterized in that during said oxidation temperature is selected so as to generate a capping oxide layer having a thickness of 2000 angströms.

14. Method according to any preceding claim characterized in that said thermal treatment further comprises after said oxidation phase a stabilization phase comprising a thermal annealing carried out in a generally neutral atmosphere and during which a bonded interface of said multilayer wafer is stabilized.

15. Method according to the preceding claim characterized in that said thermal annealing of said stabilization phase is carried out at a temperature substantially greater than said oxidation temperature.

16. Method according to the preceding claim characterized in that said thermal annealing of said stabilization phase is carried out at a temperature between 950 and 1200°C.

17. Method according to the preceding claim characterized in that said thermal annealing of said stabilization phase is carried out at a temperature of 1100°C.

18. Method according to claim 14 characterized in that said thermal annealing of said stabilization phase is carried out at a temperature substantially equal to said oxidation temperature.

19. Method according to any of the claims 14-18 characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during said stabilization phase.

20. Method according to any of the claims 14-18 characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during a ramp-down following said stabilization phase.

21. Method according to the preceding claim characterized in that said ramp-down ends with a boat-out temperature and no other high temperature treatment is carried out on said multilayer wafer before said deoxidation operation.

22. Method according to any of claims 1-13 characterized in that said control of the controlled atmosphere as an atmosphere comprising in a generally neutral atmosphere at least a species whose ions can migrate into the depth of said wafer down to said interface where reduction of the trap density is desired is carried out during a ramp-down following said oxidation phase.

23. Method according to the preceding claim characterized in that said ramp-down ends with a boat-out temperature and no other high

temperature treatment is carried out on said multilayer wafer before said deoxidation operation.

24. Method according to any of the preceding claims characterized in that said multilayer wafer has been obtained by a transfer method.

25. Method according to the preceding claim characterized in that said transfer method comprises implanting a donor substrate with at least one species in order to create in said donor substrate an embrittlement zone.

26. Method according to the preceding claim characterized in that said transfer method is a Smart-Cut™ type method.

27. Method according to any of the preceding claims characterized in that said multilayer wafer is a SOI.

28. Method according to any of the preceding claims characterized in that the boat out temperature is 450°C.

29. Method according to any of the preceding claims carried out on batches of multilayer wafers characterized in that the boat out temperature can vary among the batches while obtaining a substantially constant value of the trap density for the wafers of all batches.

30. Method according to the preceding claim characterized in that said boat-out temperatures can have the following values : 450 – 600 – 750°C.

31. Method according to any preceding claim characterized in that the active layer of said multilayer semiconductor wafer is a Si layer.

32. Method according to the preceding claim characterized in that the active layer of said multilayer semiconductor wafer is a strained Si layer.