IMPROVED BODY CONTACT FET

BACKGROUND

Related Applications

This application claims priority to and the benefit of U.S. Provisional Application No. 63/218,997, filed July 7, 2021, titled IMPROVED BODY CONTACT FET, which is incorporated in its entirety herein by reference.

Field

The present disclosure generally relates to field-effect transistor (FET) devices and more particularly to body contact arrangements for such FET devices.

Description of Related Art

In electronics applications, field-effect transistors (FETs) can be utilized as switches and in amplifiers. Switches can allow, for example, routing of radio-frequency (RF) signals in wireless devices. Amplifiers can amplify signals for transmission or amplify received signals.

FETs with a Metal-Oxide-Silicon (MOS) structure have an insulating oxide layer separating the gate-conductor and the body of the FET. Additionally, in a Silicon on Insulator (SOI) technology, an additional electrically insulating layer is buried under the body region and is termed a buried-oxide (BOX) layer.

In non-body contacted SOI devices, i.e., floating-body devices, the body portion is surrounded by the insulator layer beneath and the insulating layer above. Furthermore, due to the difference in doping type between the body region and the source region and drain region to either side, it becomes difficult to control the voltage of the body region because charges can accumulate within it that are slow to dissipate. One effect of this is that the voltage between the gate and the body region, which determines whether the transistor is on or off, can depend upon the history of the previous states of the transistor. This is known as the “floating-body problem”.

SUMMARY

In one aspect, the present disclosure refers to a field-effect transistor that includes an active region comprising a source region, a drain region, a body

region disposed between the source region and the drain region, a first body extension portion in contact with the body region, a second body extension portion in contact with the body region, and a body contact region in contact with the first extension portion and the second extension portion, and a gate disposed on a top surface of the body region.

In some examples the FET is a silicon on insulator field-effect transistor comprising an insulator layer beneath the active region and a substrate beneath the insulator layer. In some examples the insulator layer is a buried oxide layer.

In some examples the first body extension portion is unitary with the body region. In some examples the second body extension portion is unitary with the body region. In some examples the first body extension portion extends from the body region beneath the source region. In some examples the first body extension portion creates a first body extension layer beneath the source region. In some examples the first body extension portion further extends beneath the body contact region. In some examples the first body extension portion creates a second body extension layer beneath the body contact region.

In some examples the second body extension portion extends from the body region through the source region. In some examples the second body extension portion extends from the body region through the source region along an edge of the source region. In some examples the second body extension portion extends from the body region through the source region along through a middle portion of the source region, such that the source region is disposed on either side or both sides of the second body extension portion. In some examples the second body extension portion extends from the body region through the source region at a mid-point of the source region.

In some examples the gate extends over a top surface of the second body extension portion.

In some examples the FET further comprises a first silicide layer disposed on a top surface of the source region and the body contact region. In some examples the first silicide layer is a self-aligned silicide layer. In some examples the FET further comprises a second silicide layer disposed on a top surface of the drain region. In some examples the second silicide layer is a self-aligned silicide layer.

In some examples the FET is an extended drain field-effect transistor further comprising a drain extension region disposed between an upper portion of the body region and the drain region.

In some examples the active region comprises one or more notches adjacent to the gate. In some examples the second body extension portion comprises a plurality of second body extension sub-portions.

In some examples the body region, the first body extension portion and the second body extension portion comprise a semiconductor having a relatively weak doping of a first type, the body contact region has a relatively strong doping of the first type, and the source region and the drain region have a doping of a second type. In some examples the doping of the first type is N-type and the doping of the second type is P-type. In some examples the doping of the first type is P-type and the doping of the second type is N-type.

In some examples the gate comprises a polysilicon layer disposed on top of an insulator layer. In some examples the gate comprises a metal layer and a polysilicon layer disposed on top of an insulator layer. In some examples the insulator layer is an oxide layer. In some examples, the insulator layer is a layer with high-k dielectrics.

In another aspect, the present disclosure refers to a die comprising a first and second field-effect transistor, the first and second field-effect transistor each comprising an active region comprising a source region, a drain region, a body region disposed between the source region and the drain region, a first body extension portion in contact with the body region, a second body extension portion in contact with the body region, and a body contact region in contact with the first extension portion and the second extension portion, and a gate disposed on a top surface of the body region.

In some examples the first and second field-effect transistors share a common body contact region. In some examples the body region of the first field-effect transistor and the body region of the second field-effect transistor are disposed on opposite sides of the common body contact region. In some examples the first and second field-effect transistors share a common second body extension portion. In some examples the first and second field-effect transistors share a common gate.

In some examples the die further comprises a third field-effect transistor and a fourth field-effect transistor wherein: the first and second field-effect transistors share a first common

body contact region and are disposed on either side of the first common body contact region, the third and fourth field-effect transistors share a second common body contact region and are disposed on either side of the second common body contact region, and the first, second, third and fourth field-effect transistors share a common second body extension portion.

In some examples the first, second, third and fourth field-effect transistors share a common gate. In some examples the common gate has an "H" shape.

In another aspect, the present disclosure refers to a radio-frequency module comprising: a packaging substrate configured to receive a plurality of devices, and a die mounted on the packaging substrate, the die including a field-effect transistor having an active region comprising a source region, a drain region, a body region disposed between the source region and the drain region, a first body extension portion in contact with the body region, a second body extension portion in contact with the body region, and a body contact region in contact with the first extension portion and the second extension portion; and a gate disposed on a top surface of the body region.

In another aspect, the present disclosure refers to a wireless mobile device comprising: one or more antennas; and a radio-frequency module that communicates with the one or more antennas, the radio-frequency module having a die including a field-effect transistor having an active region comprising a source region, a drain region, a body region disposed between the source region and the drain region, a first body extension portion in contact with the body region, a second body extension portion in contact with the body region, and a body contact region in contact with the first extension portion and the second extension portion; and a gate disposed on a top surface of the body region.

Examples disclosed herein address the floating-body problem and other problems. This may be done, in part, by providing devices with an improved body contact. Still other examples, and advantages of these examples are discussed in detail below. Examples disclosed herein may be combined with other examples in any manner consistent with at least one of the principles disclosed herein, and references to "an example," "some examples," "an alternate example," "various examples," "one example" or the like are not necessarily mutually exclusive and are intended to indicate that a particular feature, structure, or characteristic described may be included in at least one example. The appearances of such terms herein are not necessarily all referring to the same example.

BRIEF DESCRIPTION OF THE DRAWINGS

Various aspects of at least one embodiment are discussed below with reference to the accompanying figures, which are not intended to be drawn to scale. The figures are included to provide illustration and a further understanding of the various aspects and embodiments, and are incorporated in and constitute a part of this specification, but are not intended as a definition of the limits of the invention. In the figures, each identical or nearly identical component that is illustrated