CLAIMS

1. A dual reference voltage generator, applied to an equalizer circuit,

wherein the dual reference voltage generator is configured to receive an original code, a first code and a second code, generate a first reference voltage according to the original code and the first code, and generate a second reference voltage according to the original code and the second code, the first reference voltage being different from the second reference voltage;

the dual reference voltage generator comprises: a first processing circuit, a second processing circuit, a first selector, a second selector, a first output buffer circuit, a second output buffer circuit and a voltage divider circuit;

two input terminals of the first processing circuit are configured to respectively receive the first code and the original code, and an output terminal of the first processing circuit is connected to a control terminal of the first selector;

two input terminals of the second processing circuit are configured to respectively receive the second code and the original code, and an output terminal of the second processing circuit is connected to a control terminal of the second selector;

one or more output terminals of the voltage divider circuit are respectively connected to one or more input terminals of the first selector and one or more input terminals of the second selector; and

an output terminal of the first selector is connected to an input terminal of the first output buffer circuit, an output terminal of the second selector is connected to an input terminal of the second output buffer circuit, the first reference voltage is output from an output terminal of the first output buffer circuit, and the second reference voltage is output from an output terminal of the second output buffer circuit.

2. The dual reference voltage generator of claim 1, wherein the voltage divider circuit comprises a plurality of voltage output terminals having output voltages different from one another.

3. The dual reference voltage generator of claim 2, wherein the plurality of voltage output terminals of the voltage divider circuit are respectively connected to a plurality of input terminals of the first selector and a plurality of input terminals of the second selector.

4. The dual reference voltage generator of claim 3, wherein the first selector is configured to select, based on a code output by the first processing circuit, one of a plurality of voltages output from the voltage divider circuit, and output the one of the plurality of voltages to the first output buffer circuit; and the second selector is configured to select, based on a code output by the second processing circuit, a second one of the plurality of voltages output from the voltage divider circuit, and output the second one of the plurality of voltages to the second output buffer circuit.

5. The dual reference voltage generator of claim 4, wherein the first processing circuit comprises an adder for performing addition operation processing on the original code and the first code that are received by the first processing circuit, and outputting a processed code; and

the second processing circuit comprises a subtractor for performing subtraction operation processing on the original code and the second code that are received by the second processing circuit, and outputting a second processed code.

6. The dual reference voltage generator of claim 5, wherein the first processing circuit further comprises a first decoder, an input terminal of the first decoder being connected to an output

terminal of the adder, and an output terminal of the first decoder being connected to the control terminal of the first selector; and

the second processing circuit further comprises a second decoder, an input terminal of the second decoder being connected to an output terminal of the subtractor, and an output terminal of the second decoder being connected to the control terminal of the second selector.

7. The dual reference voltage generator of any one of claims 1 to 6, wherein the first reference voltage is greater than the second reference voltage.

8. The dual reference voltage generator of any one of claims 1 to 6, wherein the first selector and the second selector have a same circuit structure.

9. The dual reference voltage generator of any one of claims 1 to 6, wherein the first output buffer circuit and the second output buffer circuit have a same circuit structure.

10. The dual reference voltage generator of claim 6, wherein the first decoder and the second decoder have a same circuit structure.

11. An equalizer circuit, comprising: a dual reference voltage generator, a first input buffer circuit, a second input buffer circuit and a selecting and sampling circuit,

wherein the dual reference voltage generator is the dual reference voltage generator according to any one of claims 1 to 10, and two different reference voltages output by the dual reference voltage generator serve as input reference voltages of the first input buffer circuit and the second input buffer circuit, respectively;

the first input buffer circuit and the second input buffer circuit are respectively

connected to the selecting and sampling circuit; and

the selecting and sampling circuit is configured to select, according to data previously output by the equalizer circuit, whether to perform data sampling on a data signal output by the first input buffer circuit or a data signal output by the second input buffer circuit, and take sampled data as data currently output by the equalizer circuit.

12. The equalizer circuit of claim 11, wherein when the original code, the first code and the second code that are received by the dual reference voltage generator are all at target values, a voltage margin and a timing margin in an eye diagram corresponding to received data of the equalizer circuit are made to be at maximum values.

13. The equalizer circuit of claim 12, wherein the target values of the original code, the first code and the second code are set by the following operations:

a first operation of setting initial values of the original code, the first code and the second code as 0;

a second operation of adding 1 to the value of the original code, and testing a magnitude of the timing margin in the eye diagram corresponding to the received data of the equalizer circuit;

a third operation of repeatedly performing the second operation until the maximum value of the timing margin is obtained;

a fourth operation of setting the target value of the original code as a value of the original code when the timing margin is at the maximum value;

a fifth operation of respectively adding 1 to the values of the first code and the second code, and testing a magnitude of the voltage margin in the eye diagram corresponding to the received data of the equalizer circuit;

a sixth operation of repeatedly performing the fifth operation until the maximum value

of the voltage margin is obtained; and

a seventh operation of setting the target values of the first code and the second code as values of the first code and the second code when the voltage margin is at the maximum value.

14. A memory, comprising an equalizer circuit according to any one of claims 11 to 13.