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Electronic Circuit Interconnection System Using Virtual Mirror Packages

Background of the Invention

This invention pertains to packages (e.g., chip carriers) that contain integrated circuits or other electronic circuits and, more particularly, to such a package wherein the electrical interconnections (e.g., pins or solder pads) are arranged in a virtual mirror pattern. This invention also pertains to a system for interconnecting multiple virtual mirror packages having common signal lines (e.g., common bus signal lines) by attaching the virtual mirror packages to a substrate (e.g., a printed circuit board) in a arrangement wherein the spacing between adjacent packages approaches zero.

It is well known that the propagation delay between two points (i.e., the time it takes an electrical signal to travel between the two points) increases as the distance between the two points increases. Consequently, one factor that limits the speed of a bus in a computer or other information processing system is the distance between the various components that are coupled to the bus. More specifically, the bus master and slave devices that have the greatest physical separation on the bus is one factor that limits the maximum speed of the bus. Stated another way, for any given bus speed, the maximum physical separation between any bus master and slave device must be less than a predetermined distance, and that predetermined distance gets shorter and shorter as bus speed increases. While the spacing of bus components is not problematic at bus clock frequencies well below 100 MHz, component spacing becomes critical at higher clock frequencies where it becomes imperative to keep component spacing to a minimum.

Figs. 1 and 2 are plan views of prior art computer component interconnection systems wherein five interconnected "nodes" are illustrated. Referring to these figures, components 101, 102, 103 and 104 may be four processors and component 105 may be a memory/host bridge controller. These components are interconnected by bus 106 (Fig.1) or bus 201 (Fig. 2). Components 101-104 typically extend several inches in the "z" direction (out of the paper) and are separated by about two inches to accommodate large heat sinks. Consequently, the large separation of components in the "x" direction, which is required for the heat sinks, and the extension of the components in the "z" direction results in a long "signaling distance" between components, which significantly limits the maximum speed of operation.

One technique for placing bus components close together is to use mirror image components placed on opposite sides of a thin substrate, such as a printed circuit

board. Since mirror image components are only separated by the thickness of the substrate when interconnected in this manner, this technique brings the components very close together. The downside to the use of "true mirror image" components is that they require the manufacturer to stock and test two separate part numbers; one for the standard component and another for its mirror image.

Accordingly, the invention described below allows multiple electronic components to be interconnected very close together, thereby reducing the propagation delay between components and permitting higher speed operation. This invention also permits identical components (for example, multiple CPU's) in identical "virtual mirror" packages to be interconnected on opposite sides of a thin substrate, thereby eliminating the need for two separate "true mirror image" packages. The invention described below also permits large heat sinks to be attached to the components for improved cooling.

Summary of the Invention

Briefly, the invention is a computer or other information handling system that includes a substrate and a first bus having a multiplicity of substantially parallel conductors formed on a first surface of the substrate. A first chip carrier has a multiplicity of pairs of connection points, wherein each pair of connection points comprising electrically interconnected first and second connection points. The set of first connection points is arranged in a first pattern adjacent a first edge of the first chip carrier, and the set of second connection points is arranged in a second pattern adjacent a second edge of the first chip carrier, such that the second pattern is the virtual mirror of the first pattern.

The information handling system also includes a second chip carrier having a multiplicity of pairs of connection points, wherein each pair of connection points comprising electrically interconnected first and second connection points. The set of first connection points is positioned adjacent a first edge of the second chip carrier, and the set of second connection points is positioned adjacent a second edge of the second chip carrier. The pattern of pairs of connection points of the second chip carrier is a virtual mirror of the pattern of pairs of connection points of the first chip carrier. The first and second chip carriers are connected to the first bus on the first surface of the substrate, with the first edge of the second chip carrier being adjacent the second edge of the first chip carrier.

In another embodiment, the invention is a computer or other information handling system including a substrate, a first bus having a multiplicity of substantially parallel conductors formed on a first surface of the substrate, and a second bus having a multiplicity of substantially parallel conductors formed on a second surface of the substrate. Each conductor of the second bus is positioned directly opposite and electrically connected to the corresponding conductor of the first bus. A first chip carrier has a multiplicity of pairs of connection points, wherein each pair of connection points comprises electrically interconnected first and second connection points. The set of first connection points is arranged in a first pattern adjacent a first edge of the first chip carrier, and the set of second connection points is arranged in a second pattern adjacent a second edge of the first chip carrier, such that the second pattern is the virtual mirror of the first pattern. A second chip carrier has a multiplicity of pairs of connection points, wherein each pair of connection points comprises electrically interconnected first and second connection points. The set of first connection points is positioned adjacent a first edge of the second chip carrier, and the set of second connection points is positioned adjacent a second edge of the second chip carrier. The pattern of pairs of connection points of the second chip

carrier is the virtual mirror of the pattern of pairs of connection points of the first chip carrier. The first chip carrier is connected to the first bus on the first surface of the substrate, while the second chip carrier is connected to the second bus on the second surface of the substrate opposite the first chip carrier.

In yet another embodiment, the invention is a virtual mirror chip carrier that includes a multiplicity of pairs of connection points, wherein each pair of connection points comprising electrically interconnected first and second connection points. The set of first connection points is arranged in a first pattern along a first edge of the chip carrier, and the set of second connection points is arranged in a second pattern along a second edge of the chip carrier, such that the second pattern is the virtual mirror of the first pattern.

Brief Description of the Drawings

Fig. 1 is a plan view of a prior art computer component interconnection system.

Fig. 2 is a plan view of another prior art computer component interconnection system.

Fig. 3 is a plan view of a virtual mirror chip carrier package of the current invention.

Fig. 4 is a plan view of another virtual mirror chip carrier package.

Fig. 5 is a plan view of a component interconnection system using virtual mirror packages on one side of a substrate.

Fig. 6 is a plan view of a component interconnection system using virtual mirror packages on two sides of a substrate.

Description of the Illustrative Embodiments

Fig. 3 is a plan view of a chip carrier having connection points arranged in a virtual mirror pattern. Referring to this figure, chip carrier 301 includes five pairs of first and second connection points arranged in two sets; the first set of connection points 302 (consisting of individual points 302a - 302e) being arranged adjacent edge 301a, and the second set of connection points 303 (consisting of individual points 303a - 303e) being arranged adjacent edge 301b, which is directly opposite edge 301a. Conductors 304a-304e in chip carrier 301 electrically connect each connection point of the first set of connection points 302 to a corresponding connection point from the second set of connection points 303, thereby forming five pairs of connection points. For example, connection points 302a and 303a form one pair of connection points, connection points 302b and 303b form another pair of connection points, etc. Preferably, chip carrier 301 is constructed as a well known ball grid array package, although other integrated circuit or electronic circuit packaging may be suitable.

Fig. 4 is a plan view of chip carrier having connection points arranged in a another virtual mirror pattern. Referring to this figure, chip carrier 401 includes ten pairs of first and second connection points arranged in two sets; the first set of connection points 402 (consisting of individual points 402a - 402j) being arranged adjacent edges 401a and 401b, and the second set of connection points 403 (consisting of individual points 403a - 403j) being arranged adjacent edges 401c and 401d. Conductors 404a-404j of chip carrier 401 electrically connect each connection point of the first set of connection points 402 to a corresponding connection point from the

second set of connection points 403, thereby forming ten pairs of connection points. For example, connection points 402a and 403a form one pair of connection points, connection points 402b and 403b form another pair of connection points, etc. Preferably, chip carrier 401 is constructed as a well known ball grid array package, although other integrated circuit or electronic circuit packaging may be suitable.

As it is used to describe an arrangement of pairs of first and second connection points, the term "virtual mirror pattern" means that, if straight lines are drawn to connect the first and second connection points of each pair of connection points, then those straight lines would all be substantially parallel. This concept is illustrated in Fig. 3 wherein imaginary lines 305a-305e are all parallel, and again in Fig. 4 wherein imaginary lines 405a-405j are all parallel. If these lines are substantially parallel, it can also be said that the arrangement of the set of second connection points is the virtual mirror of the set of first connection points. If two chip carriers have the same virtual mirror pattern of pairs of connection points, then their respective pairs of connection points are co-linear when the two chip carriers are placed side-by-side.

This parallel arrangement of the pairs of connection points permits a first set of chip carriers, each having the same virtual mirror pattern of connection points, to be mounted in a straight line, edge-to-edge, and connected to a bus composed of a plurality of parallel conductors formed on a first surface of a substrate. This concept is illustrated in Fig. 5 wherein three virtual mirror chip carrier packages 501-503 are connected, edge-to-edge, to a bus 504 composed of a multiplicity of parallel conductors formed on the surface of a substrate. Note that the spacing between chip carriers 501-503 can be arbitrarily small.

A similar bus of parallel conductors can also be formed on the opposing second surface of the substrate, directly below the corresponding conductors of the bus on the first surface. In the alternative, this second bus does not require the parallel conductors of the first bus. Instead, the conductors of the second bus may simply be comprised of the exposed ends of the vias that connect the first bus on the first surface to the opposing second surface of the substrate. A second set of chip carriers having substantially the same virtual mirror pattern as the first set of chip carriers can then be attached to the bus on the second surface, directly below the chip carriers on the first surface. This concept is illustrated in Fig. 6, wherein three virtual mirror chip carrier packages 601-603 are connected (edge-to-edge, with minimal spacing between the three chip carriers) to a bus 607a composed of a multiplicity of parallel conductors formed on the first surface of a substrate, and three more virtual mirror chip carrier packages 604- 606 are connected to bus 607b directly underneath chip carriers 601-603. Preferably, the conductors of bus 607b on the second surface of the substrate are directly underneath the corresponding conductors of bus 607a on the first side of the substrate, and are interconnected using well known vias.

To attach the second set of chip carriers to the second surface of the substrate, each of the chip carriers of the second set of chip carriers is inverted (relative to the first set of chip carriers) by rotating it 180° about an imaginary axis drawn perpendicular to the aforementioned parallel lines through each pair of connection points. When the chip carriers are inverted in this fashion, each pair of connection points can be lined up with the corresponding conductors of the bus on the second surface of the substrate which, in turn, are lined up directly underneath the corresponding conductors of the bus on the first surface of the substrate. Imaginary axes 306 and 406 are illustrated in Figs. 3 and 4 and chip carriers 301 and 401 can be rotated 180° about these axes to orient the virtual mirror chip carriers for

attachment to the underside of the substrate. This over/under arrangement of two sets of virtual mirror chip carriers allows for simple interconnection between the conductors of the buses on the first and second sides of the substrate. This interconnection between the conductors on the two surfaces of the substrate can be accomplished by using well known "vias" or other surface-to-surface interconnection techniques.

It is preferred, but not required, that the sets of first and second connection points be symmetrical about an imaginary axis. If such symmetry exists, then this imaginary axis is the line that perpendicularly bisects the parallel line segments that can be drawn through each pair of connection points. This concept is illustrated in Fig. 3 wherein imaginary axis 306 perpendicularly bisect the line segments drawn between each pair of connection points (e.g., 302a and 303a, 302b and 303b, etc.). These line segments coincide with lines 305a-305e, but terminate at the connection points. This concept is also illustrated in Fig. 4 wherein imaginary axis 406 perpendicularly bisects the line segments drawn between each pair of connection points (e.g., 402a and 403a, 402b and 403b, etc.) Given two chip carriers having pairs of connection points arranged in the same symmetrical virtual mirror pattern, if the second chip carrier is rotated 180° about its imaginary axis and then placed directly underneath the first chip carrier, then each and every one of the pairs of connection points of the first chip carrier will be positioned directly above the corresponding pair of connection points of the second chip carrier.

It is preferred, but not required, that the parallel lines be equally spaced. When the connection points are equi-spaced, the conductors on the substrate to which the chip carrier is attached can also be equi-spaced. The chip carriers illustrated in Figs. 3 and 4 are examples of equi-spaced, symmetrical virtual mirror patterns.

Note that the term "chip carrier" is used in a broad sense throughout the specification and claims and includes any type of package that can be used to house an integrated circuit chip or other electrical circuit device. The term "substrate" includes printed circuit boards, ceramic substrates (such as those used in thick and thin film hybrid circuits) and other materials and techniques to which electrical components are attached and interconnected. The term "connection point" includes well known pins (such as the type that are inserted into a socket), solder pads and other connection devices that serve to electrically interconnect the chip carrier to conductors on a substrate.

One advantage to the systems described herein is that, because the components are so close together, they can now share pull up resistors (e.g., resistors 505 and 608) or decoupling capacitors (not illustrated). In fact, it is likely that a savings of 75% in the number of decoupling capacitors will be realized by the use of the virtual mirror system of Fig. 6 when compared to the prior art systems of Figs. 1 and 2. This could result in a 100 component reduction in the total number of pull up resistors and decoupling capacitors, when compared to the prior art systems.

Another advantage to the systems of Figs. 5 and 6 is that they are well suited for thermal cooling, since a heat sink or heat pipe can be placed flat across each individual component, or across all components on one surface of the substrate.

The primary advantage of the systems of Figs. 5 and 6 is that a significant increase in bus speed can be achieved simply because the components are closer together.

CLAIMS

I claim as my invention:

1. An information handling system, comprising:
 - a substrate;
 - a first bus having a multiplicity of substantially parallel conductors formed on a first surface of the substrate;
 - a first chip carrier having a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being arranged in a first pattern adjacent a first edge of the first chip carrier, and the set of second connection points being arranged in a second pattern adjacent a second edge of the first chip carrier, such that the second pattern is the virtual mirror of the first pattern;
 - a second chip carrier having a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being positioned adjacent a first edge of the second chip carrier, and the set of second connection points being positioned adjacent a second edge of the second chip carrier, the pattern of pairs of connection points of the second chip carrier being a virtual mirror of the pattern of pairs of connection points of the first chip carrier;
 - the first and second chip carriers being connected to the first bus on the first surface of the substrate, the first edge of the second chip carrier being adjacent the second edge of the first chip carrier.



2. The information handling system of claim 1, further comprising:

a third chip carrier having a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being positioned adjacent a first edge of the third chip carrier, and the set of second connection points being positioned adjacent a second edge of the third chip carrier, the pattern of pairs of connection points of the third chip carrier being a virtual mirror of the pattern of pairs of connection points of the first chip carrier;

the third chip carrier being connected to the first bus on the first surface of the substrate, the second edge of the third chip carrier being adjacent the first edge of the first chip carrier.



3. The information handling system of claim 1, further comprising:

a second bus having a multiplicity of conductors formed on a second surface of the substrate, each conductor of the second bus being positioned opposite and electrically connected to the corresponding conductor of the first bus;

a third chip carrier having a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being positioned adjacent a first edge of the third chip carrier, and the set of second connection points being positioned adjacent a second edge of the third chip carrier, the pattern of pairs of connection points of the third chip carrier being a virtual mirror of the pattern of pairs of connection points of the first chip carrier;

the third chip carrier being connected to the second bus on the second surface of the substrate opposite the first chip carrier.

4. The information handling system of claim 3, further comprising:

a fourth chip carrier having a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being positioned adjacent a first edge of the fourth chip carrier, and the set of second connection points being positioned adjacent a second edge of the fourth chip carrier, the pattern of pairs of connection points of the fourth chip carrier being a virtual mirror of the pattern of pairs of connection points of the first chip carrier;

the fourth chip carrier being connected to the second bus on the second surface of the substrate, the second edge of the fourth chip carrier being adjacent the first edge of the third chip carrier.



5. An information handling system, comprising:
- a substrate;
 - a first bus having a multiplicity of substantially parallel conductors -
formed on a first surface of the substrate;
 - a second bus having a multiplicity of conductors formed on a second
surface of the substrate, each conductor of the second bus being positioned
opposite and electrically connected to the corresponding conductor of the first bus;
 - a first chip carrier having a multiplicity of pairs of connection points,
each pair of connection points comprising electrically interconnected first and second
connection points, the set of first connection points being arranged in a first pattern
adjacent a first edge of the first chip carrier, and the set of second connection points
being arranged in a second pattern adjacent a second edge of the first chip carrier,
such that the second pattern is the virtual mirror of the first pattern;
 - a second chip carrier having a multiplicity of pairs of connection points,
each pair of connection points comprising electrically interconnected first and second
connection points, the set of first connection points being positioned adjacent a first
edge of the second chip carrier, and the set of second connection points being
positioned adjacent a second edge of the second chip carrier, the pattern of pairs of
connection points of the second chip carrier being a virtual mirror of the pattern of
pairs of connection points of the first chip carrier;
 - the first chip carrier being connected to the first bus on the first surface
of the substrate, and the second chip carrier being connected to the second bus on
the second surface of the substrate opposite the first chip carrier.



6. A virtual mirror chip carrier, comprising: a multiplicity of pairs of connection points, each pair of connection points comprising electrically interconnected first and second connection points, the set of first connection points being arranged in a first pattern along a first edge of the chip carrier, and the set of second connection points being arranged in a second pattern along a second edge of the chip carrier, such that the second pattern is the virtual mirror of the first pattern.

7. The virtual mirror chip carrier of claim 6, wherein the first edge of the chip carrier is substantially parallel to the second edge of the chip carrier.

8. The virtual mirror chip carrier of claim 7, wherein the first and second sets of connection points are symmetrical about an imaginary axis that perpendicularly bisects each of imaginary lines that connect the first and second connection points of each pair of connection points.

9. The virtual mirror chip carrier of claim 8, wherein each pair of connection points is equally space apart from the adjacent pair of connection points.

10. The virtual mirror chip carrier of claim 6, wherein the first edge of the chip carrier is adjacent to the second edge of the chip carrier.



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11. The virtual mirror chip carrier of claim 10, wherein the first and second sets of connection points are symmetrical about an imaginary axis that perpendicularly bisects each of imaginary lines that connect the first and second connection points of each pair of connection points.

12. The virtual mirror chip carrier of claim 11, wherein each pair of connection points is equally spaced apart from the adjacent pair of connection points.

13. The virtual mirror chip carrier of claim 6, wherein the first and second sets of connection points are symmetrical about an imaginary axis that perpendicularly bisects each of imaginary lines that connect the first and second connection points of each pair of connection points.

14. The virtual mirror chip carrier of claim 13, wherein each pair of connection points is equally space apart from the adjacent pair of connection points.

