ABSTRACT

A semiconductor memory device, and a method of manufacturing the same, includes a cell region of a substrate including a first stacked structure and a second stacked structure stacked on the first stacked structure, and a contact region of the substrate. The first stacked structure includes at least one lower cell plug pattern and a lower slit pattern extending in a vertical direction. The second stacked structure includes at least one upper cell plug pattern extending in the vertical direction and directly contacting an upper surface of the at least one lower cell plug pattern and an upper slit pattern extending in the vertical direction and directly contacting an upper surface of the lower slit pattern. A lower surface of the upper slit pattern contacting the upper surface of the lower slit pattern has a lower critical dimension than the upper surface of the lower slit pattern.

FIG. 4