DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and processes for packaging microelectronic dice. In particular, the present invention relates to a packaging technology that fabricates build-up layers on encapsulated microelectronic dice and on the encapsulation material which covers the microelectronic dice.

State of the Art: Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As these goals are achieved, microelectronic dice become smaller. Of course, the goal of greater packaging density requires that the entire microelectronic die package be equal to or only slightly larger (about 10% to 30%) than the size of the microelectronic die itself. Such microelectronic die packaging is called a "chip scale packaging" or "CSP".

As shown in FIG. 8, true CSP would involve fabricating build-up layers directly on an active surface 204 of a microelectronic die 202. The build-up layers may include a dielectric layer 206 disposed on the microelectronic die active surface 204. Conductive traces 208 may be formed on the dielectric layer 206, wherein a portion of each conductive trace 208 contacts at least one contact 212 on the microelectronic die active surface 204. External contacts, such as solder balls or conductive pins for contact with an external component (not shown), may be fabricated to electrically contact at least one conductive trace 208. FIG. 8 illustrates the external contacts as solder balls 214 which are surrounded by a solder mask material 216 on the dielectric layer 206. However in such true CSP, the surface area provided by the microelectronic die active surface 204 generally does not provide enough surface for all of the external contacts needed to

contact the external component (not shown) for certain types of microelectronic dice (i.e., logic).

Additional surface area can be provided through the use of an interposer, such as a substrate (substantially rigid material) or a flex component (substantially flexible material). FIG. 9 illustrates a substrate interposer 222 having a microelectronic die 224 attached to and in electrical contact with a first surface 226 of the substrate interposer 222 through small solder balls 228. The small solder balls 228 extend between contacts 232 on the microelectronic die 224 and conductive traces 234 on the substrate interposer first surface 226. The conductive traces 234 are in discrete electrical contact with bond pads 236 on a second surface 238 of the substrate interposer 222 through vias 242 that extend through the substrate interposer 222. External contacts 244 (shown as solder balls) are formed on the bond pads 236. The external contacts 244 are utilized to achieve electrical communication between the microelectronic die 224 and an external electrical system (not shown).

The use of the substrate interposer 222 requires number of processing steps. These processing steps increase the cost of the package. Additionally, even the use of the small solder balls 228 presents crowding problems which can result in shorting between the small solder balls 228 and can present difficulties in inserting underfilling between the microelectronic die 224 and the substrate interposer 222 to prevent contamination and provide mechanical stability.

FIG. 10 illustrates a flex component interposer 252 wherein an active surface 254 of a microelectronic die 256 is attached to a first surface 258 of the flex component interposer 252 with a layer of adhesive 262. The microelectronic die 256 is encapsulated in an encapsulation material 264. Openings are formed in the flex

component interposer 252 by laser abalation through the flex component interposer 252 to contacts 266 on the microelectronic die active surface 254 and to selected metal pads 268 residing within the flex component interposer 252. A conductive material layer is formed over a second surface 272 of the flex component interposer 252 and in the openings. The conductive material layer is patterned with standard photomask/etch processes to form conductive vias 274 and conductive traces 276. External contacts are formed on the conductive traces 276 (shown as solder balls 278 surrounded by a solder mask material 282 proximate the conductive traces 276).

The use of a flex component interposer 252 requires gluing material layers which form the flex component interposer 252 and requires gluing the flex component interposer 252 to the microelectronic die 256. These gluing processes are relatively difficult and increase the cost of the package. Furthermore, the resulting packages have been found to have poor reliability.

Therefore, it would be advantageous to develop new apparatus and techniques to provide additional surface area to form traces for use in CSP applications, while utilizing commercially available, widely practiced semiconductor fabrication techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGs. 1a-1j are side cross-sectional views of a first embodiment of a process of forming a microelectronic package, according to the present invention;

FIGs. 2a-2d are side cross-sectional views of another embodiment of a process of forming a microelectronic package that incorporates a heat dissipation device, according to the present invention;

FIGs. 3a-3f are side cross-sectional views of a method for die alignment, attachment, and molding of a microelectronic package, according to the present invention;

FIGs. 4a-4e are side cross-sectional views of another method for die alignment, attachment, and molding of a microelectronic package, according to the present invention;

FIGs. 5a-5f are side cross-sectional views of still another method for die alignment, attachment, and molding of a microelectronic package, according to the present invention;

FIGs. 6a-6e are side cross-sectional views of an alternate method for die alignment, attachment, and molding of a microelectronic package, according to the present invention;

FIGs. 7a-7e are side cross-sectional views of another alternate method for die alignment, attachment, and molding of a microelectronic package, according to the present invention;

FIG. 8 is a cross-sectional view of a true CSP of a microelectronic device, as known in the art;

FIG. 9 is a cross-sectional view of a CSP of a microelectronic device utilizing a substrate interposer, as known in the art; and

FIG. 10 is a cross-sectional view of a CSP of a microelectronic device utilizing a flex component interposer, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1a-1j, 2a-2d, 3a-3f, 4a-4e, 5a-5f, 6a-6e, and 7a-7e illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate semiconductor assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain the same numeric designation.

The present invention relates to a packaging technology that fabricates build-up layers on an encapsulated microelectronic die and on the encapsulation material that covers the microelectronic die. An exemplary microelectronic package includes a microelectronic die having an active surface and at least one side. An encapsulation material is disposed adjacent the microelectronic die side(s), wherein the encapsulation material includes at least one surface substantially planar to the microelectronic die active surface. A first dielectric material layer may be disposed on at least a portion of the microelectronic die active surface and the encapsulation material surface. At least one conductive trace is then disposed on the first dielectric material layer. The conductive trace(s) is in electrical contact with the microelectronic die active surface. At least one conductive trace extends adjacent the microelectronic die active surface and adjacent the encapsulation material surface.

FIGs. 1a-1j illustrate a first embodiment of a process of forming a microelectronic package of the present invention. As shown in FIG. 1a, a protective film 104 is abutted against an active surface 106 of a microelectronic die 102 to protect the microelectronic die active surface 106 from any contaminants. The microelectronic die active surface 106 has at least one contact 108 disposed thereon. The contacts 108 are in electrical

contact with integrated circuitry (not shown) within the microelectronic die 102. The protective film 104 is preferably a polyimide material and may have a weak adhesive, such as silicone, which attaches to the microelectronic die active surface 106. This adhesive-type film may be applied prior to placing the microelectronic die 102 in a mold or other such equipment used for the encapsulation process. The protective film 104 may also be a non-adhesive film, such as a ETFE (ethylene - tetrafluoroethylene) or Teflon® film, which is held on the microelectronic die active surface 106 by an inner surface of the mold or other such equipment during the encapsulation process.

The microelectronic die 102 is then encapsulated with an encapsulating material 112, such as plastics, resins, epoxies, and the like, as shown in FIG. 1b, that covers a back surface 114 and side(s) 116 of the microelectronic die 102. The encapsulation of the microelectronic die 102 may be achieved by any known process, including but not limited to transfer and compression molding, and dispensing. The encapsulation material 112 provides mechanical rigidity, protects the microelectronic die 102 from contaminants, and provides surface area for the build-up of trace layers.

After encapsulation, the protective film 104 is removed, as shown in FIG. 1c, to expose the microelectronic die active surface 106. As also shown in FIG. 1c, the encapsulation material 112 is preferably molded to form at least one surface 110 which is substantially planar to the microelectronic die active surface 106. The encapsulation material surface 110 will be utilized in further fabrication steps as additional surface area for the formation of build-up layers, such as dielectric material layers and conductive traces.

A first dielectric layer 118, such as epoxy resin, polyimide, bisbenzocyclobutene, and the like, is disposed over the microelectronic die active surface 106, the contacts

108, and the encapsulation material surface 110, as shown in FIG. 1d. The dielectric layers of the present invention are preferably filled epoxy resins available from Ibiden U.S.A. Corp., Santa Clara, California, U.S.A. and Ajinomoto U.S.A., Inc., Paramus, New Jersey, U.S.A. The formation of the first dielectric layer 118 may be achieved by any known process, including but not limited to film lamination, spin coating, roll-coating and spray-on deposition.

As shown in FIG. 1e, a plurality of vias 122 are then formed through the first dielectric layer 118. The plurality of vias 122 may be formed any method known in the art, including but not limited to laser drilling, photolithography, and, if the first dielectric layer 118 is photoactive, forming the plurality of vias 122 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

A plurality of conductive traces 124 is formed on the first dielectric layer 118, as shown in FIG. 1f, wherein a portion of each of the plurality of conductive traces 124 extends into at least one of said plurality of vias 122 to make electrical contact with the contacts 108. The plurality of conductive traces 124 may be made of any applicable conductive material, such as copper, aluminum, and alloys thereof. As shown in FIG. 1f, at least one conductive trace extends adjacent the microelectronic die active surface 106 and adjacent said encapsulation material surface 110.

The plurality of conductive traces 124 may be formed by any known technique, including but not limited to semi-additive plating and photolithographic techniques. An exemplary semi-additive plating technique can involve depositing a seed layer, such as sputter-deposited or electroless-deposited metal on the first dielectric layer 118. A resist layer is then patterned on the seed layer, such as a titanium/copper alloy, followed by electrolytic plating of a layer of metal, such as copper, on the seed layer exposed by

open areas in the patterned resist layer. The patterned resist layer is stripped and portions of the seed layer not having the layer of metal plated thereon is etched away. Other methods of forming the plurality of conductive traces 124 will be apparent to those skilled in the art.

As shown in FIG. 1g, a second dielectric layer 126 is disposed over the plurality of conductive traces 124 and the first dielectric layer 118. The formation of the second dielectric layer 126 may be achieved by any known process, including but not limited to film lamination, roll-coating and spray-on deposition.

As shown in FIG. 1h, a plurality of second vias 128 are then formed through the second dielectric layer 126. The plurality of second vias 128 may be formed any method known in the art, including but not limited to laser drilling and, if the second dielectric layer 126 is photoactive, forming the plurality of second vias 128 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

If the plurality of conductive traces 124 is not capable of placing the plurality of second vias 128 in an appropriate position, then other portions of the conductive traces are formed in the plurality of second vias 128 and on the second dielectric layer 126, another dielectric layer formed thereon, and another plurality of vias is formed in the dielectric layer, such as described in FIG. 1f–1h. The layering of dielectric layers and the formation of conductive traces can be repeated until the vias are in an appropriate position. Thus, portions of a single conductive trace be formed from multiple portions thereof and can reside on different dielectric layers.

A second plurality of conductive traces 132 may be formed, wherein a portion of each of the second plurality of conductive traces 132 extends into at least one of said plurality of second vias 128. The second plurality of conductive traces 132 each include

a landing pad 134 (an enlarged area on the traces demarcated by a dashed line 140), as shown in FIG. 1i.

Once the second plurality of conductive traces 132 and landing pads 134 are formed, they can be used in the formation of conductive interconnects, such as solder bumps, solder balls, pins, and the like, for communication with external components (not shown). For example, a solder mask material 136 can be disposed over the second dielectric layer 126 and the second plurality of conductive traces 132 and landing pads 134. A plurality of vias is then formed in the solder mask material 136 to expose at least a portion of each of the landing pads 134. A plurality of conductive bumps 138, such as solder bumps, can be formed, such as by screen printing solder paste followed by a reflow process or by known plating techniques, on the exposed portion of each of the landing pads 134, as shown in FIG 1j.

FIGs. 2a-2d illustrate another embodiment of the present invention that incorporates a heat dissipation device. As shown in FIG. 2a, a thermally conductive, heat dissipation device, such as heat slug 152 is attached to the microelectronic die back surface 114, preferably with a thermally conductive adhesive (not shown). The heat slug 152 should have a CTE (coefficient of thermal expansion) close to that of the microelectronic die 102 to reduce thermal stresses. For example, for a microelectronic die 102 formed of a silicon material, thermally conductive materials such as molybdenum and aluminum/silicon/carbon alloys would closely match the CTE of the silicon material.

The protective film 104 is abutted against the microelectronic die active surface 106, as shown in FIG. 2b. The protective film 104 may be adhesive or non-adhesive as previously discussed. The microelectronic die 102 and the heat slug 152 are then

encapsulated with an encapsulating material 112, as shown in FIG. 2c, that covers microelectronic die side(s) 116 and side(s) 154 of the heat slug 152. A back surface 156 of the heat slug 152 is preferably not cover with the encapsulating material 112 so that thermal energy drawn into the heat slug 152 from the microelectronic die 102 can be dissipated to the ambient environment from the heat slug back surface 156, or so that an addition heat dissipation device can be attached to the heat slug back surface 156. As illustrated in FIG. 2d, after encapsulation, the protective film 104 is removed and at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124, and landing pads 134 are fabricated, such as described in FIGs. 1c-1i.

The present invention also includes a methods for die alignment, attachment, and molding. FIGs 3a-3f illustrate one such method. The active surfaces 106 of a plurality of microelectronic dice 102 are aligned on and attached to the protective film 104, preferably an adhesive backed foil, which extends between a rigid frame 162, preferably a metal frame, as shown in FIG. 3a. The alignment of the plurality of microelectronic dice 102 may be achieved with fiducial marks (not shown) on the protective film 104. As shown in FIG. 3b, a thermally conductive, heat dissipation device, such as heat slug 164, is then attached with a thermally conductive adhesive to the plurality of microelectronic dice 102. The heat slug 164 may be a solid plate or may have a webbed configuration, as shown in top view in FIG. 3c. After attachment of the heat slug 164 to the plurality of microelectronic dice 102, the encapsulation material 112 is molded around the microelectronic dice 102 and the heat slug 164, as shown in FIG. 3d. After encapsulation, as shown in FIG. 3e, the protective film 104 is removed to expose the active surfaces 106 of the plurality of microelectronic dice 102. As illustrated in FIG. 3e,

at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124 and 132, and landing pads 134 are fabricated, such as described in FIGs. 1c-1i. It is, of course, understood that the plurality of microelectronic dice 102 and its associated portion of the heat slug 164 could be singulated either before or after the fabrication of the various dielectric layers, conductive traces, and conductive pads.

FIGs. 4a-4e illustrate another method for die alignment, attachment, and molding. As shown in FIG. 4a, the back surfaces 114 of a plurality of microelectronic dice 102 are aligned and attached with a thermally conductive adhesive to the heat slug 164. Again, the heat slug 164 may be a solid plate or may have a webbed configuration, as shown in top view in FIG. 3c. The alignment of the plurality of microelectronic dice 102 may be achieved with fiducial marks (not shown) on the heat slug 164. A protective film 104, such as a non-adhesive material, is mounted to a flat plate 166, such as an internal surface of a mold. The protective film 104 is then pressed against the active surfaces 106 of a plurality of microelectronic dice 102, as shown in FIG. 4b. The encapsulation material 112 is molded around the microelectronic dice 102 and the heat slug 164, as shown in FIG. 4c. After encapsulation, as shown in FIG. 4d, the removal of the flat plate 166 also removes the protective film 104 to expose the active surfaces 106 of the plurality of microelectronic dice 102. As illustrated in FIG. 4e, at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124 and 132, and landing pads 134 are fabricated, such as described in FIGs. 1c-1i. Again, it is understood that the plurality of microelectronic dice 102 and its associated portion of the heat slug 164 could be singulated either before or after the fabrication of the various dielectric layers, conductive traces, and conductive pads.

FIGs. 5a-5f illustrate still another method for die alignment, attachment, and molding. As shown in FIG. 5a, the microelectronic die back surface 114 is thinned, such as by grinding, to form a thin microelectronic die 172. The back surfaces 174 of a plurality of thin microelectronic dice 172 are aligned and attached with a thermally conductive adhesive (not shown) to a silicon wafer 176 which acts as heat dissipation device, as shown in FIG. 5b. The alignment of the plurality of thin microelectronic dice 172 may be achieved with fiducial marks (not shown) on the silicon wafer 176. A protective film 104, such as a non-adhesive material, is mounted to a flat plate 166, such as an internal surface of a mold. The protective film 104 is then pressed against the active surfaces 178 of the plurality of microelectronic dice 172, as shown in FIG. 5c. Encapsulation material 112 is molded around the thin microelectronic dice 172 and the silicon wafer 176, as shown in FIG. 5d. After encapsulation, as shown in FIG. 5e, the removal of the flat plate 166 also removes the protective film 104 to expose the active surfaces 178 of the plurality of thin microelectronic dice 172. As illustrated in FIG. 5f, at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124 and 132, and landing pads 134 are fabricated, such as described in FIGs. 1c-1i. Again, it is understood that the plurality of thin microelectronic dice 172 and its associated portion of the silicon wafer 176 could be singulated either before or after the fabrication of the various dielectric layers, conductive traces, and conductive pads.

FIGs. 6a-6e illustrate still another method for die alignment, attachment, and molding. As shown in FIG. 6a, the back surfaces 114 of a plurality of microelectronic dice 102 are aligned on and attached to a first protective film 182, preferably an adhesive backed foil, which extends between a rigid frame 162, preferably a metal frame, as

shown in FIG. 3a. The alignment of the plurality of microelectronic dice 102 may be achieved with fiducial marks (not shown) on the first protective film 182. A second protective film 184, such as a non-adhesive material, is mounted to a flat plate 166, such as an internal surface of a mold. The second protective film 184 is then pressed against the active surfaces 106 of a plurality of microelectronic dice 102, as shown in FIG. 6b. The encapsulation material 112 is molded around the microelectronic dice 102, as shown in FIG. 6c. After encapsulation, as shown in FIG. 6d, the removal of the flat plate 166 also removes the second protective film 184 to expose the active surfaces 106 of the plurality of microelectronic dice 102. As illustrated in FIG. 6e, at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124 and 132, and landing pads 134 are fabricated, such as described in FIGs. 1c-1i. Furthermore, as also shown in FIG. 6d, the first protective film 182 is removed to expose the microelectronic die back surfaces 114. The exposed microelectronic die back surfaces 114 may then be attached to heat dissipation devices. Again, it is understood that the plurality of microelectronic dice 102 could be singulated either before or after the fabrication of the various dielectric layers, conductive traces, and conductive pads.

FIGs. 7a-7e illustrate still yet another method for die alignment, attachment, and molding. As shown in FIG. 7a, a plurality of heat slugs 152 is attached to the back surfaces 114 of a plurality of microelectronic dice 102, preferably with a thermally conductive adhesive (not shown). The back surfaces 156 of a plurality of heats slugs 152 are aligned on and attached to a first protective film 182, preferably an adhesive backed foil, which extends between a rigid frame 162, preferably a metal frame. The alignment may be achieved with fiducial marks (not shown) on the first protective film 182. As shown in FIG. 7b, a second protective film 184, such as a non-adhesive

material, is mounted to a flat plate 166, such as an internal surface of a mold. The second protective film 184 is then pressed against the active surfaces 106 of a plurality of microelectronic dice 102. The encapsulation material 112 is molded around the microelectronic dice 102, as shown in FIG. 7c. After encapsulation, as shown in FIG. 7d, the first protective film 182 is removed and the removal of the flat plate 166 also removes the second protective film 184 to expose the active surfaces 106 of the plurality of microelectronic dice 102. As illustrated in FIG. 7e, at least one dielectric layer (shown as a first dielectric layer 118 and a second dielectric layer 126), conductive traces 124 and 132, and landing pads 134 are fabricated, such as described in FIG. 1c-1i.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic package, comprising:

a microelectronic die having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and

at least one conductive trace disposed on said first dielectric material layer and in electrical contact with said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

2. The microelectronic package of claim 1, further including at least one additional dielectric material layer disposed over said at least one conductive trace and said first dielectric material layer.

3. The microelectronic package of claim 2, wherein at least a portion of said at least one conductive trace extends through and resides on said at least one additional dielectric material layer.

4. The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

5. A method of fabricating a microelectronic package, comprising:

providing at least one microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one microelectronic die active surface;

encapsulating said at least one microelectronic die with an encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulating material provides at least one surface of said encapsulation material substantially planar to said microelectronic die active surface; and

removing said protective film.

6. The method of claim 5, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said encapsulation material surface;

forming a via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said via to electrically contact said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

7. The method of claim 5, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

8. The method of claim 7, wherein forming said at least one conductive trace on said at least one dielectric layer further includes forming at least a portion of said at least one conductive trace to extend through and reside on said at least one additional dielectric material layer.

9. The method of claim 5, further including thermally contacting a heat dissipation device with a back surface of said microelectronic die.

10. A method of fabricating a microelectronic package, comprising:

providing an adhesive protective film suspended on a substantially rigid frame;

attaching an active surface of at least one microelectronic die to said adhesive film;

encapsulating said at least one microelectronic die with an encapsulation material adjacent at least one side of said microelectronic die, wherein said encapsulating material provides at least one surface of said encapsulation material substantially planar to said microelectronic die active surface; and

removing said adhesive protective film.

11. The method of claim 10, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said encapsulation material surface;

forming a via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said via to electrically contact said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

12. The method of claim 10, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

13. The method of claim 12, wherein forming said at least one conductive trace on said at least one dielectric layer further includes forming at least a portion of said at least one conductive trace to extend through and reside on said at least one additional dielectric material layer.

14. The method of claim 10, further including thermally contacting a heat dissipation device with a back surface of said microelectronic die.

15. A method of fabricating a microelectronic package, comprising:

providing at least one microelectronic die having an active surface, a back surface, and at least one side;

attaching said at least one microelectronic die back surface to a heat dissipation device;

abutting a protective film against said at least one microelectronic die active surface;

encapsulating said at least one microelectronic die and said heat dissipation device with an encapsulation material, wherein said encapsulating material provides at least one surface of said encapsulation material substantially planar to said microelectronic die active surface; and

removing said protective film.

16. The method of claim 15, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said encapsulation material surface;

forming a via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said via to electrically contact said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

17. The method of claim 15, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

18. The method of claim 17, wherein forming said at least one conductive trace on said at least one dielectric layer further includes forming at least a portion of said at least one conductive trace to extend through and reside on said at least one additional dielectric material layer.

19. The method of claim 15, further including thinning said at least one microelectronic die prior to attaching said at lest one microelectronic die back surface to a heat dissipation device.

20. A method of fabricating a microelectronic package, comprising:

providing an adhesive protective film suspended on a substantially rigid frame;

attaching a back surface of at least one microelectronic die to said adhesive film;

abutting a protective film against an active surface of said at least one microelectronic die;

encapsulating said at least one microelectronic die with an encapsulation material adjacent at least one side of said microelectronic die, wherein said encapsulating material provides at least one surface of said encapsulation material substantially planar to said microelectronic die active surface;

removing said protective film; and

removing said adhesive protective film. .

21. The method of claim 20, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said encapsulation material surface;

forming a via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said via to electrically contact said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

22. A method of fabricating a microelectronic package, comprising:

providing an adhesive protective film suspended on a substantially rigid frame;

attaching a back surface of at least one microelectronic die to at least one heat dissipation device;

attaching a back surface of said at least one heat dissipation device to said adhesive film;

abutting a protective film against an active surface of said at least one microelectronic die;

encapsulating said at least one microelectronic die with an encapsulation material adjacent at least one side of said microelectronic die, wherein said encapsulating material provides at least one surface of said encapsulation material substantially planar to said microelectronic die active surface;

removing said protective film; and

removing said adhesive protective film. .

23. The method of claim 22, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface and said encapsulation material surface;

forming a via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said via to electrically contact said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.