CLAIMS

What is claimed is:

1. An electronic package, comprising:

a first substrate;

a second substrate; and

an array of interconnects electrically coupling the first substrate to the second substrate, wherein the array of interconnects comprises:

first interconnects, wherein the first interconnects have a first volume and a first material composition; and

second interconnects, wherein the second interconnects have a second volume and a second material composition, and wherein the first material composition is different than the second material composition, and wherein the second interconnects each comprise a core, and solder completely surrounding the core, the solder having a material composition different than the first material composition.

2. The electronic package of claim 1, wherein a number of first interconnects is greater than a number of second interconnects.

3. The electronic package of claim 2, wherein the number of first interconnects is at least one-hundred times greater than the number of second interconnects.

4. The electronic package of claim 1, wherein one or more corner locations in the array of interconnects are each populated by second interconnects.

5. The electronic package of claim 1, wherein one or more center locations in the array of interconnects are each populated by second interconnects.

6. The electronic package of claim 1, wherein second interconnects are located at a non-critical-to-function (NCTF) location, a redundant power location, a redundant ground location, or a non-connect location of the electronic package.

7. The electronic package of claim 1, wherein the core is a metallic material.

8. The electronic package of claim 7, wherein the core comprises copper or nickel.

9. The electronic package of claim 1, wherein the core is a polymeric material.

10. The electronic package of claim 1, wherein the first substrate is a package substrate, and wherein the second substrate is a board.

11. The electronic package of claim 1, wherein the first substrate is a package substrate, and wherein the second substrate is an interposer.

12. The electronic package of claim 1, wherein the first substrate is a die, and wherein the second substrate is a package substrate.

13. An electronic package, comprising:

a package substrate having a first surface and a second surface opposite from the first surface;

a die attached to the first surface of the package substrate;

an array of pads over the second surface of the package substrate; and

a plurality of solder balls, wherein each solder ball is over one of the pads in the array of pads, and wherein the plurality of solder balls comprises:

first solder balls; and

second solder balls that are different than the first solder balls, wherein the first solder balls have a first volume and a first material composition, wherein the second solder balls have a second volume and a second material composition, wherein the first volume is different than the second volume and the first material composition is different than the second material composition, and wherein the second solder balls each comprise a core, and solder completely surrounding the core, the solder having a material composition different than the first material composition.

14. The electronic package of claim 13, wherein a thickness of the solder around the core is not uniform.

15. The electronic package of claim 14, wherein the solder around the core comprises a fillet.

16. The electronic package of claim 13, wherein a height of the first solder balls is greater than a height of the second solder balls.

17. The electronic package of claim 13, wherein one or more corner pads of the array of pads are each covered by one of the second solder balls.

18. The electronic package of claim 13, wherein one or more center pads of the array of pads are each covered by one of the second solder balls.

19. An electronic system, comprising:

a first substrate;

a second substrate attached to the first substrate by an array of first level of interconnects; and

a third substrate attached to the second substrate by an array of second level of interconnects, wherein at least one of the array of first level interconnects and the array of second level interconnects comprises:

first interconnects; and

second interconnects, wherein a number of first interconnects is greater than a number of second interconnects, wherein the first interconnects have a first volume and a first material composition, wherein the second interconnects have a second volume and a second material composition, wherein the first volume is different than the second volume and the first material composition is different than the second material composition, and wherein the second interconnects each comprise a core, and solder completely surrounding the core, the solder having a material composition different than the first material composition..

20. The electronic system of claim 19, wherein the first substrate is a die, wherein the second substrate is a package substrate, and wherein the third substrate is a printed circuit board (PCB).

21. The electronic system of claim 19, wherein the second interconnects are located at corner locations and/or center locations of the array of first level interconnects and/or the array of second level interconnects.