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COMPLETE SPECIFICATION

Semiconductor Junction Device for Generating Optical Radiation

We, TEXAS INSTRUMENTS INCORPORATED, a corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and more particularly to semiconductor devices comprising a body of compound semiconductor material capable of emitting optical radiation.

In Patent Specification No. 1,028,782 there is disclosed a device which comprises the semiconductor material gallium-arsenide (GaAs) and contains a rectifying junction across which an electric current flow causes the generation of optical radiation in the infrared region. The theory of operation of the light source is the generation of electron-hole pairs created by forward current flow across the junction of the device, and the recombination of electron-hole pairs produces photons whose energy is in the infrared region with a narrow bandwidth of maximum intensity of about .9 micron wavelength. Light sources of this type are much more useful in most electronic applications than are conventional light sources for many reasons. As examples, the solid state nature of the device lends itself readily to simplicity, miniaturization and high reliability. Moreover, the light output intensity can be modulated at a very high frequency by modulating the current flow to the device.

The present invention provides a semiconductor device comprising a body of compound semiconductor material having a first zone of one conductivity type and a second

zone of an opposite conductivity type contiguous to and forming a rectifying junction with the first zone, the second zone comprising a first region spaced from the periphery of the rectifying junction by a high resistance path constituted by a second region having a high resistivity relative to the first region, the device being operable to emit optical radiation in response to forward biasing of that portion of the rectifying junction adjacent the first region.

The present invention further provides a semiconductor device capable of emitting optical radiation, comprising a body of compound semiconductor material having a first zone of one conductivity type and a second zone of an opposite conductivity type contiguous to and forming a rectifying junction with the first zone, the second zone comprising a first region spaced from the periphery of the rectifying junction and by a high resistance path constituted by a second region having a high resistivity relative to the first region and means for forward biasing that portion of the rectifying junction adjacent the first region.

The invention will be more readily understood from the following description of embodiments thereof when taken in conjunction with the appended claims and the attached drawing wherein like reference numerals refer to like parts throughout the several figures, and in which:

FIGURE 1 is a perspective view in elevational section of a gallium-arsenide semiconductor junction light source without structure features which ~~eliminates~~ the peripheral current flow, and is shown for purposes of illustrating the detrimental effects of the peripheral current flow;

FIGURE 2 is an electrical schematic

[Price 4s. 6d.]





diagram of the equivalent electric circuit of the device of FIGURE 1;

FIGURE 3 is a graphical representation of the total current flowing through the device of FIGURE 1 as a function of the voltage applied thereacross;

FIGURES 4A—4K are elevational views in section illustrating the process by which one embodiment of the invention is made;

FIGURE 5 is a perspective view in elevational section of the embodiment fabricated according to the preceding FIGURES 4A—4K;

FIGURE 6 is an electrical schematic diagram of the equivalent electric circuit of the device of FIGURE 5;

FIGURE 7 is a graphical representation of the total current flowing through the device of FIGURE 5, shown on a log scale, as a function of the voltage applied thereacross, shown on a linear scale;

FIGURES 8A—8C are plan views of the light emitting surface of the device of FIGURE 1 illustrating the light output degradation as a function of operating lifetime;

FIGURE 9 is an elevational view in section of a variation of the embodiment shown in FIGURE 5;

FIGURES 10A—10F are elevational views in section illustrating the process by which another embodiment of the invention is made;

FIGURE 11 is a perspective view in elevational section of the embodiment fabricated according to the preceding FIGURES 10A—10F;

FIGURE 12 is an electrical schematic diagram of the equivalent electric circuit of the device of FIGURE 11;

FIGURE 13 is a graphical representation of the total current flowing through the device of FIGURE 11 as a function of the voltage applied thereacross;

FIGURE 14 is a graphical representation of the quantum efficiency in terms of the light output as a function of the current through the device;

FIGURE 15 is an elevational view in section of a variation of the embodiment shown in FIGURE 11;

FIGURES 16A—16D are elevational views in section illustrating the process by which an embodiment of the present invention is made;

FIGURE 17 is a perspective view in elevational section of the embodiment of the invention fabricated according to the preceding FIGURES 16A—16D;

FIGURE 18 is an electrical schematic diagram of the equivalent electric circuit of the device of FIGURE 17;

FIGURE 19 is a graphical representation of the light output of the device of FIGURE 17 as a function of the current therethrough;

FIGURE 20 is an elevational view in section of the device of FIGURE 17 illustrating its utility in one particular application to an electric circuit;

FIGURE 21 is an elevational view in section of the device of FIGURE 17 illustrating its utility in another application to an electric circuit.

In order to more clearly understand the invention, it is believed that the following discussion relating to some of the current characteristics of semiconductor junction devices will be helpful. All semiconductor junction devices are characterized by the fact that a junction or transition region located within the device intersects one or more surfaces of the device. It has been found that, in some cases, the junction at or near the surface which it intersects acts electrically quite different from the main portion of the junction located within the bulk of the semiconductor material. It is theorized that some form of "surface states" are created at the surface and within a shallow region underlying where the junction intersects the surface, which yields a different voltage-current junction characteristic than that observed for the major portion of the junction located within the bulk of the semiconductor. Moreover, surface currents can flow across the junction at the surface-junction intersection to alter the junction characteristics. Regardless of the actual cause or theory of the surface current and the current flow across the portion of the junction which is effected by the so-called surface states, the fact remains that one or both of the currents exist in some semiconductor materials and reduce the efficiency of the device. When this is the case, the electrical characteristic of the device are different from that which it should theoretically have. For example, in silicon and germanium junction transistors, an alteration of the base-emitter junction characteristics where it intersects the surface of the device has been considered the reason for the reduction in the gain of the transistor at low emitter currents. To reduce or eliminate this effect in silicon and germanium devices, a layer of silicon-dioxide is formed on the surface where the junction exists and has been found to be effective in protecting the junction from contamination, and prevents the "surface states" from being created. It has been concluded from all of the above that if surface currents of this nature exist, the portion of the junction across which this current flows is inactive to produce or contribute to the operation of the device, and consequently represents a current loss.

In addition to the above problem, which has been recognized for some time in silicon and germanium junction devices, there has also been recognized that current flow across the "active" portion of the junction located

within the bulk of the semiconductor contains a component whose magnitude varies differently as a function of voltage than does the major current flow responsible for the operation of the device. It has been concluded that this effect is insignificant in relation to both the surface current effect and the bulk current flowing across the active portion of the junction for silicon and germanium devices. Initially, however, this was not known to be the case, and consequently, the reason for the fall-off of transistor gain at low emitter currents, for example, was not understood. The bulk component effect which represents a current loss was first predicted by William Shockley, and his theory states that the larger the band-gap energy of a semiconductor material, the larger is the effect of the bulk current loss component, all other things being equal. This, taken in conjunction with the fact that both the Shockley bulk current and the surface current are expressed mathematically by the same general equation, which is different from the desired bulk current, leads to the conclusion that it is virtually impossible to predict which loss effect is predominant without suitable experimentation. Specifically, the bulk current I_B , to which the desired operation of the device is attributed, is expressed by the equation

$$(1) \quad I_B = I_0 e^{qV/kT}$$

where I_0 is a constant, q is the electronic charge, V is the voltage across the junction, k is Boltzmann's constant and T is the absolute temperature, wherein this current is usually referred to as the kT current. Both the surface current I_p and the Shockley bulk current component I_B are represented by the equation

$$(2) \quad I_p = I_B' = I_x e^{qV/nkT}$$

where I_x is another constant and n is an integer greater than unity, wherein both these currents are usually referred to as an nkT current. Thus, by observing the current-voltage characteristics of a device, it is possible to determine whether there exists an nkT current component in addition to the kT current. It is not possible, without additional information, to determine the location where, in relation to the junction, the nkT component is most predominant.

A semi-conductor device in accordance with the present invention may be formed of a compound semiconductor material such as gallium-arsenide and it has been found that the current passing through the device when a voltage is applied across the junction is comprised of at least two components, one being expressed by equation (1) above, and the other being expressed by equation (2)

above. It should be noted, however, that the band-gap for gallium-arsenide is considerably larger than for either silicon or germanium, which tends to lead to the conclusion that the nkT bulk current component is considerably larger in relation to the nkT surface current component than for either silicon or germanium. However, it has been found that the nkT bulk current component is insignificant except at extremely small operating currents, and that reduction or elimination of the nkT surface current component effected a considerable efficiency gain and provided a device which generates a greater quantity of light per unit of current input at low current levels in addition to a more linear current versus light relation. In addition to this, it has been unexpectedly observed that the light output degradation as a function of operating lifetime has been substantially reduced, and in one embodiment of the invention, the degradation effect has been eliminated. This last effect is extremely important since considerable degradation in the characteristics of a device precludes its reliable use, although it is still not understood why the degradation is eliminated in this device.

Unlike its effect in silicon and germanium junction devices, a layer of silicon-dioxide overlying the junction of a gallium-arsenide device where the junction intersects the device surface does not prevent the nkT surface current component. This is a result of the peculiarity of gallium-arsenide as compared to silicon and germanium. To reduce the nkT component in one embodiment of the present invention, a high impedance is imposed to the nkT current flow. Since the nkT surface current component exists at the periphery of the junction, or where the junction intersects the surface of the device, the problem resolves itself into the provision of a high impedance to current flow between the active and inactive portions of the junction, and specifically, takes the form of a high impedance region surrounding the active portion of the junction. In another embodiment, the inactive portion of the junction is electrically shorted in addition to providing a high impedance to current flow between the active junction region and the electrically shorted inactive junction region. In the first case, only a small amount of peripheral current flows as compared to the current which would otherwise flow, thus substantially increasing the efficiency and gain of the device at all current levels. In the second case, current flow through the inactive junction region is completely eliminated by means of the electrical short thereacross, which substantially reduces the degradation effect, and for all practical purposes, any degradation effect persisting is insignificant. Moreover, it will be seen that the provision of the high im-





pedance region is made possible by the diffusion technology utilized in forming the junction within a gallium-arsenide device, for example, which is peculiar to the semiconductor gallium-arsenide. By providing the proper bias voltage across this junction, as in one embodiment of the invention, this impedance across this junction can be made effectively infinite. In one particular embodiment of the invention, the compound semiconductor material light source contains an active junction of circular configuration with a high impedance region of annular configuration surrounding the active junction. A guard ring which takes the configuration of an annular metallic contact surrounding both the active junction and the high impedance region is provided to the surface of the device for applying a bias voltage across the high impedance region to provide an effectively infinite impedance across this portion of the junction and the complete elimination of peripheral current flow. It will be seen that the provision of the high impedance region is made possible by the diffusion technology utilized in forming the junction within a gallium-arsenide device, for example, which is peculiar to the semiconductor gallium-arsenide.

Referring now to FIGURE 1, there is shown a perspective view in elevational section of a gallium-arsenide junction device which generates optical radiation in the visual and infra-red spectrums. A single crystal wafer 2 of gallium-arsenide, usually of n-type conductivity, has diffused into one face thereof a region 4 of p-type conductivity which is highly doped and of higher electrical conductivity than the original wafer 2. The region 4 is denoted by P+ because of its high conductivity. The boundary between the two regions 2 and 4 is the junction 6 or transition region which extends to and intersects the surface 8. In this particular case, the junction is of circular configuration, and the line of intersection between the junction and the surface 8 defines a circle. For purposes of illustration only, the dashed enclosure 7 encircles the active portion of the junction situated within the bulk of the body and which is parallel to the surface of the device. An annular portion of the junction enclosed by the dashed enclosure 9, which includes the portion of the junction intersecting the surface of the device and a portion extending into the bulk of the body, will be referred to as the peripheral portion of the junction. The kT bulk current I_B flows across the active portion of the junction as noted earlier, whereas the nkT peripheral current I_P flows across the region 9. The nkT bulk current component I_B' also flows across region 7. An ohmic contact 10 is provided to the region 4, and similarly, an annular ohmic contact 12 is provided to the region

2. Electrodes 16 and 18, respectively, are provided to the two ohmic contacts, and a voltage applied between the two contacts causes a current flow through the junction, whereby the kT current I_B is effective in generating optical radiation shown schematically as N_o in Fig. 5. A layer of silicon dioxide 14 is usually provided on the surface of the device between the contacts during the fabrication thereof to provide some degree of protection for the junction where it intersects the surface of the device, although this protection is inadequate to reduce the peripheral current flow to any considerable degree.

The equivalent circuit of the device of FIGURE 1 is shown in the electrical schematic diagram of FIGURE 2, and comprises two diodes 7 and 9 in parallel with each other, since a part of the total current input flows through the peripheral junction portion 9 and is governed by equation (2) above, and the rest of the total current input flows through the active junction portion 7 and is governed by equation (1) above. The two current components I_B and I_P recombine to flow out the electrode 18 to give the equivalent circuit as shown.

The current-voltage characteristics of the device of FIGURE 1 is shown in the graphical representation of FIGURE 3, wherein the total diode current in milliamperes is shown on a logarithmic scale along the ordinate of the graph and the diode voltage in volts is shown on a linear scale along the abscissa. The voltage-current characteristics of diode 9 is a straight line denoted by I_P , whereas the characteristic of diode 7 is also a straight line denoted by I_B but with a different slope. Since the current I_B is the only component which is effective in generating light within the device, it is obvious that the desired characteristic, or what will be referred to as the ideal characteristic, is the I_B curve. However, it has been found that the device of FIGURE 1 exhibits both components, and to obtain the overall characteristic curve of the device, the two currents are added to give the characteristic curve I , which is equal to the addition of I_B and I_P , as shown. It will be noted that at low voltages, the total current of the device follows the I_P curve, whereas at higher voltages, the current follows the I_B curve. At sufficiently high currents, say above 100 milliamperes, the composite curve breaks over to the right as shown because of the bulk series resistance of the device, which is of no consequence here. It can be seen, thus, that at least one effect of the peripheral current I_P is to preclude generation of substantial optical radiation at low currents. Also shown in the graph of FIGURE 3 is the characteristic curve of the light output N_o as a function of the voltage



Characteristic

across the diode. Since the current I_B generates the light output N_0 and the two are proportional, the curve N_0 is parallel to the curve I_B . Thus, if the ideal current I_B is shown graphically as a function of the light output, a linear relation will result as will be shown later. However, due to the existence of the current component I_P , the light output N_0 is not a linear function of the total current to the device.

Referring to FIGURES 4A—4K, which illustrates the method by which one embodiment of the invention is fabricated, elevational views in section of a wafer of gallium-arsenide semiconductor material is shown during the various stages of fabrication of the device. Initially, a thin coating of silicon dioxide 22 is deposited on a surface 24 of a single-crystalline gallium-arsenide wafer 20, which is usually of n-type conductivity. The surface 24 is usually polished prior to the depositing of the silicon-dioxide layer, and the silicon-dioxide layer is deposited by any suitable means, such as by reactively sputtering, for example, or depositing the silicon-dioxide from the vapor state by the pyrolytic decomposition of a suitable organic compound. All of such processes are well known and will not be described here. After the oxide layer has been deposited, a photographic masking and etching technique is used to remove selected portions of the oxide to permit the diffusion of an impurity into the wafer. For purposes of illustration, the wafer is considered to be circular in geometry with the section views of the figures being taken across the diameter of the wafer. A circular opening 26 is cut in the oxide at the center of the wafer as shown in FIGURE 4B, and an annular ring 28 is cut in the oxide near the periphery of the wafer surrounding the opening 26. The photographic technique used is well known in the art and comprises masking of that portion of the oxide that is to remain on the surface and etching away the remainder of the oxide with a suitable etch that attacks the oxide but not the gallium-arsenide wafer. Once the oxide has been selectively removed as shown in Figure 4B, the wafer is then sealed in a quartz ampule with an appropriate impurity, such as zinc or zinc-arsenide ($ZnAs_2$), as examples, and heated to a temperature of about 900 degrees centigrade for about four minutes. This causes the impurity to diffuse into the wafer beneath the openings in the oxide to a depth of about 0.3 mil. The impurity determines p-type conductivity when diffused into an n-type semiconductor and thus a p-type conductivity region 30 is formed beneath the opening 26 and is separated from the original n-type conductivity wafer by a rectifying junction 7. Similarly, an annular region 32 is formed beneath the annular opening 28,

and is also of p-type conductivity. Actually, the regions 30 and 32 are converted to relatively high conductivity p-type regions, and are more aptly denoted by a P+ region, which indicates that these regions are of a substantially higher conductivity than the original wafer.

Unlike other impurities which are normally used in conjunction with silicon and germanium semiconductors, zinc and zinc-arsenide diffuse through a silicon-dioxide layer, whereas the normal impurities used with silicon and germanium are blocked by a silicon-dioxide layer. Thus, the diffusant penetrates through the oxide coating to form thin annular p-type conductivity channel regions 34 and 36 underlying the oxide. The effect of the oxide layer, however, is to greatly reduce the surface concentration of the impurity at the wafer surface beneath the oxide layer as contrasted to the relatively high surface concentration of the impurity at the surface of the wafer coinciding with the openings. As a result, the diffused regions beneath the oxide layer have a relatively low electrical conductivity. The channel regions are very thin according to the above-described diffusion process and may be approximately 1 micron, or .04 mil in depth.

The oxide is removed from the surface of the wafer after the various regions have been diffused, as shown in FIGURE 4D, and a new layer of silicon-dioxide, which covers the entire surface, is deposited as shown in FIGURE 4E. Subsequently, an annular opening 42 is removed in the oxide at the periphery of the wafer to expose the thin annular diffused region 36 and a small segment of the deep annular region 32, as shown in FIGURE 4F. The wafer is then immersed in an etch which does not attack the silicon-dioxide coating but which etches away the exposed portions of the wafer beneath the opening 42. The wafer is left in the etch for a time just sufficient to etch below the junction between the region 36 and the original wafer to expose an n-type conductivity surface 44 as shown in FIGURE 4G. Again, the oxide layer 40 is removed as shown in FIGURE 4H so that a new layer 46 can be deposited as shown in FIGURE 4I, and subsequently, a circular opening 48 is cut in the oxide layer to expose the central region 30. Also, an annular opening 50 is cut in the oxide to expose the periphery of the wafer and a portion of the annular P+ region 32, all as shown in FIGURE 4J. The device, in this configuration, contains a rectifying junction which intersects the surface 44 of the wafer at the location 51. Finally, metal contacts are provided to the surfaces of the device exposed through the openings in the oxide. As examples, an alloy comprised of 4% zinc and 96% gold by weight is evaporated on and alloyed to the surface of region





30 to form an ohmic contact 52 therewith. An alloy comprised of 0.6% antimony and 99.4% gold by weight is evaporated on the surface exposed through opening 50, subsequently plated with nickel and alloyed to form a single annular ohmic contact 54 to both the original n-type conductivity wafer surface 44 and P+ region 32, thus electrically shorting the two. Electrodes 56 and 58 are then welded to the contacts 52 and 54, respectively. The junction-surface intersection 51 is actually an extension of the central active junction 7 and represents the inactive junction region through which the undesired peripheral current will flow unless prevented. However, contact 54 shorts this inactive junction region, and any current tending to pass through the junction at this point is shunted through the contact. The active bulk junction 7 is not shorted, however, and is isolated from the contact 54 through the high resistance annular channel region 34. All of this is more clearly shown in the perspective view of the completed device shown in FIGURE 5, which is also a sectional view in elevation across the diameter of the wafer. As will be shown later, only a very small percentage of the total current supplied to the device flows through the channel 34.

The equivalent circuit of the device of FIGURE 5 is shown in the electrical schematic diagram of FIGURE 6, and comprises the active junction 7 between the central region 30 and the original wafer 20 connected in parallel with a resistance R_c , which is the equivalent resistance of the channel 34 between the contact 54 and the active junction region 30. No peripheral junction exists because of the fact that it is shorted by contact 54. The current through the diode 7 is the ideal or bulk current I_B governed by equation (1) above, whereas the current through the resistance R_c , which will now be referred to as the peripheral current, I_P , is

equal to $\frac{V}{R_c}$, where V is the voltage across the diode. It should be remembered, however, that the peripheral current is different from that flowing through a junction at the periphery of the device.

The voltage-current characteristics of the device of FIGURE 5 are also shown in the graphical representation of FIGURE 7. The current flow through the parallel resistance, R_c , or that passing through the narrow channel region 34 in parallel with the junction 7, is designated on the graph as I_P and varies linearly as a function of the diode voltage. At very low voltages most of the current supplied to the diode of FIGURE 5 passes through the parallel resistance R_c . However, for a voltage across the diode of about .8 to 1.0 volt, almost all of the current supplied to the device flows through the

diode junction 7. The composite current curve of the equivalent circuit of FIGURE 6 is denoted as $I = I_B + I_P$. It can be seen from these curves that the ideal kT characteristic curve is attained at about the same current level for the improved device as for the unimproved device of FIGURE 1. However, the departure of the curve from the kT characteristic at low currents is because of the resistance R_c and not because of a peripheral nkT current flow.

The foregoing graphs illustrate the electrical characteristics for the unimproved and improved devices having substantially identical dimensions and parameters except the high resistance channel region and shorted contact of the latter. As a specific example of dimensions and parameters for the improved device, the diameter of the active P+ region 30 is usually made to about 5 mils, and the inside diameter of the deep annular region 32 is made to be about 50 mils. This yields an annular channel region 34 whose lateral dimension is about 45 mils. The above diffusion process produces a channel region whose sheet resistance is about 1000 ohms/square, so that the resistance of the channel region is about 300 ohms.

Among the advantages of the embodiment shown in FIGURE 5 is the fact that no current passes through the inactive portion of the junction where it intersects a surface of the device, and as a consequence thereof, it has been found, unexpectedly so, that the lifetime characteristics are markedly improved. The degradation effect substantially reduced here is shown pictorially in FIGURES 8A-8C, wherein FIGURE 8A illustrates, in plan view, the surface of a light emitting device through which the light is emitted, such as the surface of the device of FIGURE 1 opposite the electrical contact 10. FIGURE 8A represents that light is being uniformly emitted over the entire device surface during its initial operation. After several hours of operation, however, dark lines or striations begin to appear at the edge of the light emitting surface with these lines being disposed at various 60° angles to each other as shown in FIGURE 8B. These angles, it is believed, correspond roughly to the crystalline structure of the gallium-arsenide wafer, and by quantitative measurements, it has been found that the total light output has decreased for the same current input. After further operation, the dark lines progress in length and number and eventually extend over the entire diameter of the wafer and occupy a substantially large portion of the surface area, such as illustrated in FIGURE 8C. It can be quite readily concluded that the part of the wafer surface occupied by the dark lines does not emit light, and it is believed that corresponding portions of the rectifying junction

65

70

75

80

85

90

95

100

105

110

115

120

125

substantially



within the wafer have become inactive to light generation, thus representing a current loss. The reason for the occurrence of this effect is not completely understood, and prior to the invention, no plausible reason or cause could be established. It is apparent that a device exhibiting a deteriorating effect of this nature is limited in its reliable application to circuitry.

Observing the quantity of light output for constant currents as a function of operating lifetime for a device having means of eliminating current flow through the inactive peripheral junction portion, such as the improved embodiment just described, indicates that the dark lines do not appear and that the light output remains constant. This is clearly an unexpected and desirable result. It is highly desirable since its operating parameters (light output) remain the same function of current over an indefinite operating lifetime. Evidently, the nkT current flow at the junction periphery is the cause of the deterioration effect, and eliminating this nkT current precludes any onset of degradation. The fact that the device does not generate any more light at lower current levels than the unimproved device is relatively unimportant, since the device of FIGURE 5 is used primarily for high current (and thus high power) applications. It can be seen from the graph that at high currents, the current follows the kT characteristic curve. To improve the efficiency of the device at lower current levels, only the magnitude of R_g need be increased.

A variation of the embodiment of FIGURE 5 is shown in the elevational view in section of FIGURE 9. This device has the same electrical characteristics as the improved embodiment just described, but is somewhat simpler to fabricate. In the preceding embodiment, the provision of the deep annular P+ region 32 is for the purpose of facilitating an ohmic connection to the narrow channel region 34. That is, it is easier to make an ohmic connection to the high conductivity P+ region than the high resistivity region 34. However, such connections can be made to provide the device shown in FIGURE 9 with the metal contact 54 connected directly to the channel region 34 and the n-type wafer 20. Thus, some of the steps of the fabrication process are eliminated, such as obviating the necessity of a photographic mask with an annular opening and the provision of the deep P+ region 32.

A different embodiment of the invention will now be described which has better efficiency characteristics than the previous embodiment, has more linear operation between the light output and current input at low current levels, and which ~~greatly~~ reduces the light output degradation effect alluded to.

Referring now to FIGURES 10A-10F,

which shows a gallium-arsenide wafer during the various stages of fabrication of the embodiment, a layer 72 of silicon-dioxide is deposited onto the surface of a gallium-arsenide single crystal wafer 70, and masking and etching techniques are used to provide a circular opening 76 in the oxide layer, as shown in FIGURE 10A. The wafer is then diffused with a suitable impurity, all as previously described, to provide a P+ region 78 beneath the opening 76 which forms a rectifying junction 82 with the n-type conductivity gallium-arsenide wafer 70, as shown in FIGURE 10B. The impurity also penetrates through the silicon-dioxide layer 72 to form a very thin diffused channel region 80 having an annular configuration surrounding the circular P+ region 78. Again, the region 80 is of p-type conductivity but has a very high resistivity. The oxide layer 72 is then removed and a new layer is deposited over the entire surface of the wafer. Subsequently, a portion of the silicon-dioxide coating is selectively removed to provide an annular opening 86 exposing a portion of the channel region 80, all as shown in FIGURE 10C. The remaining oxide layer covers the entire P+ region 78 and a portion of the channel region 80. The wafer is then etched down below the junction formed between the channel region 80 and the wafer 70 as shown in FIGURE 10D, with the silicon-dioxide coating 84 protecting the wafer therebeneath from being attacked by the etch. Thus, a portion of the channel region is removed and a portion of the latter remains which is contiguous with the P+ region 78. Subsequently, the oxide layer 84 is again removed and another layer deposited on the entire surface of the wafer is selectively etched to provide a central opening 92 whose diameter is slightly less than the diameter of the P+ region 78 and which exposes most of this region. Moreover, an annular opening 94 is provided at the periphery of the wafer which surrounds both the P+ region and the channel region 80, but which does not extend to the channel 80, all as shown in FIGURE 10E. Finally, suitable metallic contacts 96 and 100 are formed into the P+ region 78 and n-type wafer at the periphery of the wafer, respectively, as shown in FIGURE 10F, with electrodes 98 and 102 being connected to the contacts 96 and 100, respectively.

The device of this embodiment, as more clearly shown in the perspective view of FIGURE 11, contains an active junction 79 formed between the central P+ region 78 and the wafer 70. Moreover, the junction intersects the surface 81 of the device at the periphery of the annular channel region 80. However, any current flow across the peripheral junction region is impeded by the high resistance of the channel region 80, just



wafer

as in the previous embodiment, although in this case, the peripheral junction region is not electrically shorted.

The electrical equivalent circuit of this embodiment is shown in the schematic diagram of FIGURE 12, and comprises a diode 79, which is the equivalent of the active junction region, and connected in parallel therewith is the series combination of the equivalent resistance R_g of the channel region 80 and the peripheral diode region 81. The operation of the device can best be described in conjunction with the graphical representation of FIGURE 13, which illustrates the total device current, shown along the logarithmic scale of the ordinate, as a function of voltage along the linear scale of the abscissa. At low voltages, the total current through the device is controlled by diode 81. That is, at small enough voltages the impedance of diode 81 is large as compared to resistance R_g , but is small as compared to the impedance of diode 79. As the voltage across the device increases, the impedance of diode 81 becomes less and the increase in voltage appears across resistance R_g until, at higher voltages, the increase in voltage is seen across diode 79. This all occurs at low voltages and very low currents, such as, for example, between currents of 0.1 ma to about 1.0 ma as shown in FIGURE 13. Above about 1.0 ma, the device acts as if it comprised only the ideal kT current. It will be noted that the current level at which the device current starts to approach the ideal kT current curve is much lower than for either the unimproved device of FIGURE 1 or the previous embodiment. This results from the series combination of diode 81 and resistance 80. Thus, the efficiency improvement at low currents is much more substantial than in the other embodiment. Although some peripheral current flows through diode 81, it is insignificant to that which flows through the unimproved device of FIGURE 1, and thus, degradation effects are greatly reduced.

To further illustrate the efficiency improvement, the quantum efficiency, η_q , as a function of the total diode current in milliamperes is shown in the graphical representation of FIGURE 14, where the quantum efficiency is shown on a normalized scale and the device current is plotted on a logarithmic scale. Here, the quantum efficiency is defined as the ratio of the quantity of light output to the total number of units of electric current supplied to the device. Assuming an ideal case where the only current passing through the device is the kT bulk current through the active junction portion, there will be a constant relation between the quantity of light generated and the amount of input current, designated as $\eta = \text{constant}$ on the graph. In such a case, the light output will vary linearly with the current through the

diode. The efficiency as a function of the total current for the device of FIGURE 1 is designated by the term unimproved device in the graph, where it can be seen that the total current through the device must reach a substantial value, say about 100 milliamperes, before the efficiency approaches that for the ideal case. The efficiency curve as a function of total current for the improved embodiment just described is designated in the graph, where it is apparent that the efficiency is substantially improved at all current levels and reaches about half that of the ideal case at a current less than one milliampere.

A variation of the embodiment just described is shown in FIGURE 15, whereby the channel region extends all the way to the side of the wafer. Instead of contact 100 being made to the top of the wafer as shown in FIGURE 11, an annular contact 104 is provided to the bottom of the n-type conductivity wafer at the periphery thereof, and the light generated within the device is emitted through the opening 108 surrounded by contact 104. Otherwise, the device is electrically equivalent to the device just described.

Turning now to another embodiment of the invention, reference is had to the FIGURES 16A—16D which illustrate the method of fabricating the device of the invention. These figures are various elevational views in section of a wafer of gallium-arsenide semiconductor material during the stages of fabrication of the device which is similar to the fabrication described with reference to FIGURE 4. Initially, a gallium-arsenide single crystal wafer 120 has deposited on a surface 124 thereof a thin coating of silicon-dioxide 122 as shown in FIGURE 16A. This is done by polishing the surface 124 of the wafer and reactively sputtering a film of silicon-dioxide (SiO_2) on the surface to a thickness of approximately 6000 Angstrom ($\text{\AA}$) units. Any other suitable process for depositing the layer can also be used. For purposes of illustration only, the wafer is considered to be circular in geometry with the section views of FIGURES 16A—16D being taken across the diameter of the wafer. A circular opening 126 is cut in the oxide at the center of the wafer as shown in FIGURE 16B, and an annular ring 128 is cut in the oxide at the periphery of the wafer surrounding the hole 126 by photographic masking and oxide etching techniques. An impurity is then diffused into the wafer through the openings in the oxide to a depth of about 0.3 mils. It can then be seen that a circular P+ conductivity region 130 is formed beneath the circular opening 126, and an annular P+ region 132 is formed beneath the annular opening 128 at the periphery of the wafer. In addition to the

diffusion through the holes, the impurity also diffuses through the oxide layers to form a thin annular diffused channel 134 underlying the oxide. The original gallium-arsenide wafer is of n-type conductivity, whereas zinc or zinc-arsenide when diffused into the wafer converts the diffused region to p-type conductivity. Actually, the diffused regions beneath the holes in the oxide are converted to a relatively high conductivity p-type region because of the high surface concentration of the impurity and are more aptly denoted P+ regions. The effect of the oxide layer is to greatly reduce the surface concentration of the impurity beneath the oxide layer as compared to the surface concentration of the impurity at the surface of the wafer beneath the openings. As a result, the p-type channel region 134 has a low electrical conductivity and acts as a relatively high resistance to lateral current flow between the regions 130 and 132 which it connects. The channel region 134 is very thin and may be approximately 1 micron or less in thickness. The junction between the central region 130 and the original wafer constitutes the active junction of the device, whereas the inactive portion of the junction intersects a surface 109 of the wafer at the periphery substantially removed from the active portion and is separated therefrom by the high resistance channel region 134. The surface intersection 109 is the location at which the undesirable peripheral current will flow unless it is eliminated.

After the diffused regions are formed, metallic contacts are provided to the regions 130, 132 and to the n-type wafer 120 in the same manner described above. As examples, an alloy comprised of 4% zinc and 96% gold by weight is evaporated on and then alloyed to the regions 130 and 132 to form ohmic contacts 136 and 138 thereto. An alloy comprised of 0.6% antimony and 99.4% gold by weight is evaporated onto the bottom surface of the n-type wafer 120, subsequently plated with nickel, selected etched to remove all but an annular ring 140, and then alloyed to form an ohmic contact. The contact 136 serves as the anode of the device, and the annular contact 140 serves as the cathode, whereas the contact 138 serves as a guard-ring to be described below. Suitable electrodes 150, 152 and 156 are welded to the contacts 136, 138 and 140, respectively, for making electrical connections to the device. The annular configuration of the contact 140 on the opposite surface of the wafer permits light to emerge from the device when a forward current is passed through the junction 107 by means of electrodes 150 and 156. Without providing any bias whatsoever to the guard-ring 138, only a small amount of peripheral current will flow across the junction where it intersects the surface 109 of the device. How-

ever, the complete elimination of this current is desirable.

The completed device is shown in the perspective view of FIGURE 17, taken in section across the diameter of the wafer. To completely eliminate any peripheral current flow at the junction-surface intersection 109, a suitable biasing voltage V_g supplied by a voltage source 154 is applied between the electrodes 150 and 152 with the positive terminal connected to the electrode 150. The equivalent circuit of the device of FIGURE 17 is shown in the electrical schematic diagram of FIGURE 18 and comprises a resistance R_g in series combination with a diode 109, with this combination being connected in parallel with a diode 107. The resistance R_g is the equivalent series resistance of the channel region 134 to current flow between the region 130 and region 132. Diode 109 is equivalent to the diode at the junction-surface intersection through which the peripheral current is to be eliminated, whereas diode 107 is the equivalent of the active junction of the device. The biasing voltage 154 is connected across the series resistance R_g . By properly adjusting the voltage V_g to create a current I_g through the series resistance R_g , the voltage drop across diode 109 can be reduced to zero or even reverse-biased, which completely eliminates the peripheral current I_p . The use of a relatively small voltage V_g and bias current I_g is made possible by the high value of resistance R_g , and thus the electrical power consumed in the guard-ring structure is not significant. In fact, this amount of power is small as compared to the amount of electrical power lost to peripheral current flow in the device of FIGURE 1. As a result, an overall efficiency gain is realized. Because of the elimination of the peripheral current flow, the current flowing through the device is governed entirely by the active junction of the device, and, for all practical purposes, the total input and output current is equal to the bulk kT current I_B . In such case, the total current versus voltage characteristic then becomes the ideal characteristic and is the same as the ideal I_B and N_0 curves of FIGURE 3.

The diameter of the active P+ emitter region 130 of the device is usually made to be about 5 mils, and the inside diameter of the annular P+ region 132 is made to be about 50 mils by making the dimensions of the oxide openings accordingly. This yields an annular channel region 134 whose lateral dimension is about 45 mils. The above diffusion process, as noted earlier, produces a channel depth of only about 0.03 mil (about 1 micron), and the conductivity of this region in terms of its sheet resistance is about 1000 ohms/square. The resistance of this region to lateral current flow is then about 300

ohms. It has been found that a bias voltage of about 1.2 volts is sufficient to completely eliminate any peripheral current flow, which causes a current of about 4 milliamperes to flow through the annular channel 134. Thus, the amount of electrical power required is about 5 milliwatts. It should be noted, however, that the current flow through the series resistance R_s neither adds to nor subtracts from the current flow through the main electrode of the device, thus in no way affecting the ideal characteristic curves of the device or the linear relationship between the current and light output.

15 The light output, N_o , in microwatts is shown as a function of the forward current through the device in milliamperes in the graphical representation of FIGURE 19 for several different bias voltages, V_g . Both the ordinate and the abscissa of the graph is plotted on a logarithmic scale, and the various slopes for the different bias voltages can be noted. For a log-log scale plot, only a straight line having a slope of unity (45°) represents a linear function. Thus, it can be seen that only the curve denoted by V_g equal to -1.2 volts, which gives a zero peripheral current flow through the diode 109, yields a linear function between the light output and the forward current diode. For all other bias voltages, and for a conventional junction light source without the guard ring biasing (not shown in the graph), the quantum efficiency of the device is significantly reduced at all current levels. This is shown more clearly in the graphical representation of FIGURE 14, which shows the quantum efficiency, η , plotted on a normalized scale as a function of the total diode current in milliamperes. For the case with the de-biased guard-ring to completely eliminate peripheral current flow, the efficiency of the device remains constant for all currents, whereas a significant current flow must be achieved for a diode without a guard-ring before the efficiency approaches that for the de-biased condition. In fact, the current must attain a level of about 100 milliamperes before the efficiency of the device approaches that of the de-biased guard-ring case. The reason why the peripheral current flow controls at low currents in a device such as shown in FIGURE 1 is that the active junction is not sufficiently forward-biased at these low currents.

In addition to the advantages of increasing the efficiency of the device and achieving complete linearity between the light output and the total current input, the lifetime characteristics of the embodiment shown in FIGURE 17 are also markedly improved.

The embodiment of FIGURE 17 is shown to require a separate battery 154 to supply the necessary debiasing potential V_g . In addition, a current source is required to supply

the operating current of the device. However, in certain applications, such as when the device is incorporated within a miniature circuit, separate battery sources are usually unavailable, especially those whose terminals are isolated from the other circuitry. To adapt the improved device to applications of this type, the circuit of FIGURE 20 was devised to obviate the necessity of a separate biasing source.

The device is shown in an elevational view in section and is identical to that shown in FIGURE 17. The anode or terminal 150 attached to the P+ region is connected to a reference point, such as ground potential 180, and the guard-ring terminal 152 is connected to a constant potential 184 through a current limiting resistor 182. The potential source 184 can be the main power supply output of the circuit to which the device is applied, and as shown, the guard-ring is connected to the negative terminal thereof so that the guard-ring is biased negative with respect to ground potential to which the terminal 150 is connected. The magnitude of resistor 182 is chosen to provide the desired biasing effect, where usually the guard-ring is completely debiased to eliminate peripheral current flow, such as the $V_g = -1.2V$ curve of FIGURE 19. To drive the device, the terminal 156, attached to the n-type conductivity wafer 120, is connected to a suitable driving source such as an amplifier 186 (used in its broadest sense), or any other signal source which provides the driving current. The potential on the terminal 156 will be maintained negative relative to terminal 150 to provide the proper forward bias across the junction. A signal can thus be applied between the input terminal 188 of the amplifier and ground, and so long as the signal on terminal 156 remains negative in potential relative to terminal 150, the device will produce a light output N_o proportional to the current flow I . Since the potential between terminals 150 and 152 remains constant under normal operation regardless of the potential on terminal 156, the light output of the device will remain generally linear for all driving signals. Since all of the terminals of the device can be reference to a single power supply as shown, the operation of the device is equivalent to using a separate constant potential biasing battery without the necessity thereof. This circuit may be varied by connecting the guard-ring terminal 152 to ground potential, for example, and the terminal 150 to a more positive potential.

To maintain constant gain as a function of input current, the device must be completely debiased to eliminate peripheral current flow as shown in the $V_g = -1.2V$ curve of FIGURE 19. Any other guard-ring potential which does not completely eliminate the



peripheral current flow results in a non-linear function between the light output and current input, as shown in the other curves of FIGURE 19. This latter effect can be used to advantage in the circuit of FIGURE 20 to perform certain analogue functions that correspond to the current versus light output characteristics. To increase the versatility of the device when used for such purposes, the circuit of FIGURE 21 is utilized, which is identical to that of FIGURE 20 except the guard-ring terminal 152 is used as a control terminal. In this application the device can be thought of as a true three terminal device having a control electrode for varying the gain as a function of the control signal. The control signal source is shown generally as an amplifier with an input terminal. The control signal potential is negative relative to the terminal 150, with other conditions being the same. Thus, a family of curves, such as shown in FIGURE 19, can be obtained, and either one or both of the potentials on terminals 152 and 156 can be varied. Such an operation is analogous to operating a triode tube or transistor in the non-linear extremes of its operating characteristics. It can be seen that many analogue functions are made possible by the improved device when used as such.

WHAT WE CLAIM IS:—

1. A semi-conductor device comprising a body of compound semiconductor material having a first zone of one conductivity type and a second zone of an opposite conductivity type contiguous to and forming a rectifying junction with the first zone, the second zone comprising a first region spaced from the periphery of the rectifying junction by a high resistance path constituted by a second region having a high resistivity relative to the first region, the device being operable to emit optical radiation in response to forward biasing of that portion of the rectifying junction adjacent the first region.

2. A semiconductor device capable of emitting optical radiation, comprising a body of compound semiconductor material having a first zone of one conductivity type and a second zone of an opposite conductivity type contiguous to and forming a rectifying junction with the first zone, the second zone comprising a first region spaced from the periphery of the rectifying junction by a high resistance path constituted by a second region having a high resistivity relative to the first region, and means for forward biasing that portion of the rectifying junction adjacent the first region.

3. A semiconductor device according to claim 2, wherein the biasing means are arranged to create a voltage bias of a polarity and of a sufficient magnitude across the second region to prevent substantial current

flow through that portion of the rectifying junction which is spaced away from the first region.

4. A semiconductor device according to claim 2 or 3 wherein the first region is a relatively deep region extending from a first portion of the surface of the body of semiconductor material to a first portion of the rectifying junction, which first portion of the junction is spaced from the outer periphery of the junction, and the second region is a relatively shallow high resistance channel region contiguous with the first region and extending from a second portion of the surface to a second portion of the junction.

5. A semiconductor device according to claim 4, wherein the second channel region substantially completely surrounds the first region.

6. A semiconductor device according to claim 4 or 5, wherein the second zone further comprises a third region contiguous with and laterally surrounding the second region, the third region having a lower resistivity than the second region.

7. A semiconductor device according to claim 6, wherein the third region further includes a third portion of the surface of the semiconductor body and the periphery of the rectifying junction.

8. A semiconductor device according to any one of claims 2 to 7, wherein the biasing means comprise a first electrical contact to the first region of the second zone and a second electrical contact to the first zone.

9. A semiconductor device according to claim 6 wherein the biasing means comprise a first electrical contact at the first region of the second zone and a second electrical contact at the peripheral portion of the junction.

10. A semiconductor device according to claim 9, wherein the first region has a circular configuration, the second and third regions have annular configurations and the second electrical contact comprises an annular metallic electrode.

11. A semiconductor device according to any preceding claim, wherein the first zone is N-type conductivity and the second zone is P-type conductivity.

12. A semiconductor device according to any one of claims 2 to 11, wherein the body of compound semiconductor material comprises gallium arsenide.

13. A semiconductor device as claimed in claim 1 or 2, wherein a short circuit is provided for electrically connecting the second region of the second zone to the first zone.

14. A semiconductor device substantially as hereinbefore described with reference to Figs. 4A to 7 of the accompanying drawings.

15. A semiconductor device substantially



peripheral current flow results in a non-linear function between the light output and current input, as shown in the other curves of FIGURE 19. This latter effect can be used to advantage in the circuit of FIGURE 20 to perform certain analogue functions that correspond to the current versus light output characteristics. To increase the versatility of the device when used for such purposes, the circuit of FIGURE 21 is utilized, which is identical to that of FIGURE 20 except the guard-ring terminal 152 is used as a control terminal. In this application the device can be thought of as a true three terminal device having a control electrode for varying the gain as a function of the control signal. The control signal source is shown generally as an amplifier with an input terminal. The control signal potential is negative relative to the terminal 150, with other conditions being the same. Thus, a family of curves, such as shown in FIGURE 19, can be obtained, and either one or both of the potentials on terminals 152 and 156 can be varied. Such an operation is analogous to operating a triode tube or transistor in the non-linear extremes of its operating characteristics. It can be seen that many analogue functions are made possible by the improved device when used as such.

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2. A semiconductor device capable of emitting optical radiation, comprising a body of compound semiconductor material having a first zone of one conductivity type and a second zone of an opposite conductivity type contiguous to and forming a rectifying junction with the first zone, the second zone comprising a first region spaced from the periphery of the rectifying junction by a high resistance path constituted by a second region having a high resistivity relative to the first region, and means for forward biasing that portion of the rectifying junction adjacent the first region.
3. A semiconductor device according to claim 2, wherein the biasing means are arranged to create a voltage bias of a polarity and of a sufficient magnitude across the second region to prevent substantial current

flow through that portion of the rectifying junction which is spaced away from the first region.

4. A semiconductor device according to claim 2 or 3 wherein the first region is a relatively deep region extending from a first portion of the surface of the body of semiconductor material to a first portion of the rectifying junction, which first portion of the junction is spaced from the outer periphery of the junction, and the second region is a relatively shallow high resistance channel region contiguous with the first region and extending from a second portion of the surface to a second portion of the junction.

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10. A semiconductor device according to claim 9, wherein the first region has a circular configuration, the second and third regions have annular configurations and the second electrical contact comprises an annular metallic electrode.

11. A semiconductor device according to any preceding claim, wherein the first zone is N-type conductivity and the second zone is P-type conductivity.

12. A semiconductor device according to any one of claims 2 to 11, wherein the body of compound semiconductor material comprises gallium arsenide.

13. A semiconductor device as claimed in claim 1 or 2, wherein a short circuit is provided for electrically connecting the second region of the second zone to the first zone.

14. A semiconductor device substantially as hereinbefore described with reference to Figs. 4A to 7 of the accompanying drawings.

15. A semiconductor device substantially

as hereinbefore described with reference to Fig. 9 of the accompanying drawings.

- 5 16. A semiconductor device substantially as hereinbefore described with reference to Figs. 10A to 14 of the accompanying drawings.

17. A semiconductor device substantially as hereinbefore described with reference to Fig. 15 of the accompanying drawings.

18. A semiconductor device substantially as hereinbefore described with reference to Figs. 16A to 19 of the accompanying drawings. 10

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