DESCRIPTION

OXIDE SEMICONDUCTOR LAYER AND SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The technical field of the disclosed invention relates to a semiconductor layer including an oxide semiconductor. Alternatively, the technical field of the disclosed invention relates to a semiconductor device using the semiconductor layer.

BACKGROUND ART

[0002]

A field-effect transistor is one of the most widely-used semiconductor elements. A variety of materials are used for field-effect transistors according to their uses. In particular, semiconductor materials including silicon are frequently used.

[0003]

The field-effect transistor using silicon has characteristics satisfying the needs with respect to a variety of uses. For example, single crystal silicon is used for an integrated circuit or the like which needs to be operated at a high speed, whereby the need with respect to the integrated circuit is satisfied. Further, amorphous silicon is used for an object which needs a large area, such as a display device, whereby the need with respect to the object can be satisfied.

[0004]

As described above, silicon is highly versatile and can be used for various purposes. However, in recent years, semiconductor materials tend to be expected to have higher performance as well as versatility. For example, in terms of improving performance of a large-area display device, in order to realize high-speed operation of a switching element, a semiconductor material which facilitates increase of the area of a display device and has higher performance than amorphous silicon is needed.

[0005]

Under such conditions, a technique relating to a field-effect transistor (also called an FET) using an oxide semiconductor has attracted attention. For example, in

Patent Document 1, a transparent thin film field-effect transistor using a homologous compound $InMO_3(ZnO)_m$ (M is In, Fe, Ga, or Al, and m is an integer number of greater than or equal to 1 and less than 50) is disclosed.

[0006]

In addition, in Patent Document 2, a field-effect transistor is disclosed in which an amorphous oxide semiconductor whose electron carrier concentration is less than $10^{18}/cm^3$ and which contains In, Ga, and Zn is used. Note that in Patent Document 2, the ratio of In:Ga:Zn equals to 1:1:m ($m < 6$) in the amorphous oxide semiconductor.

[0007]

Further, in Patent Document 3, a field-effect transistor is disclosed in which an amorphous oxide semiconductor including a microcrystal is used for an active layer.

[Reference]

[Patent Document]

[0008]

[Patent Document 1] Japanese Published Patent Application No. 2004-103957

[Patent Document 2] PCT International Publication No. 05/088726

[Patent Document 3] Japanese Published Patent Application No. 2006-165529

DISCLOSURE OF INVENTION

[0009]

In Patent Document 3, a disclosure is given in which a composition in a crystal state is $InGaO_3(ZnO)_m$ (m is an integer number of less than 6). Further, in Example 1 of Patent Document 3, a case of $InGaO_3(ZnO)_4$ is disclosed. However, in the real condition, adequate characteristics have not been obtained even when such oxide semiconductors are used.

[0010]

In view of the foregoing problem, it is an object to provide an oxide semiconductor layer having a novel structure which is preferably used for a semiconductor device. Alternatively, it is another object to provide a semiconductor device using an oxide semiconductor layer having the novel structure.

[0011]

In the disclosed invention, an oxide semiconductor layer having a

predetermined crystal structure in a vicinity of the surface is provided. Alternatively, a semiconductor device including the oxide semiconductor layer is provided. As an example of the predetermined crystal structure, a crystal structure having electrical anisotropy is given. Alternatively, a crystal structure having a function of suppressing the entry of impurities is given.

[0012]

It is preferable that in the oxide semiconductor layer, a region other than the above crystal structure be mainly amorphous. Note that a "vicinity of a surface (surface vicinity)" means, for example, a region in which a distance (depth) from the surface is 20 nm or less. In addition, "mainly" means a state where one occupies 50 % or more, for example. As examples of means to solve the problem, the following can be given.

[0013]

One embodiment of the disclosed invention is an oxide semiconductor layer including an amorphous region which mainly contains an amorphous oxide semiconductor containing In, Ga, and Zn and a crystal region containing crystal grains of $In_2Ga_2ZnO_7$ in a vicinity of a surface of the oxide semiconductor layer. The crystal grains are oriented so that the c-axis is almost vertical with respect to the surface. Note that almost vertical means a state within ± 10° from a vertical direction.

[0014]

In the above, the crystal grains of $In_2Ga_2ZnO_7$ preferably has a stacked-layer structure of a first layer containing In, a second layer without In, a third layer without In, a fourth layer containing In, a fifth layer without In. Further, one of a 5s orbital of In is preferably overlapped with an adjacent 5s orbital of In in the first layer containing In or the fourth layer containing In.

[0015]

In the above amorphous region, a Zn content (atomic%) is preferably less than an In content or a Ga content (atomic%). In addition, the length (size) of the crystal grains in a c-axis direction is preferably less than five times as long as the length (size) thereof in an a-axis direction or a b-axis direction.

[0016]

Another embodiment of the disclosed invention is a semiconductor device including a gate electrode layer, a gate insulating layer over the gate electrode layer, a semiconductor layer over the gate insulating layer, and a source electrode layer and a drain electrode layer which are electrically connected to part of the semiconductor layer. The above oxide semiconductor layer is applied to the semiconductor layer.

[0017]

Another embodiment of the disclosed invention is a semiconductor device including a semiconductor layer, a gate insulating layer over the semiconductor layer, a gate electrode layer over the gate insulating layer, and a source electrode layer and a drain electrode layer which are electrically connected to part of the semiconductor layer. The above oxide semiconductor layer is applied to the semiconductor layer.

[0018]

The above semiconductor device preferably includes an insulating layer covering the semiconductor layer. Further, the source electrode layer or the drain electrode layer, and the semiconductor layer are electrically connected to each other on an upper surface or a lower surface of the semiconductor layer.

[0019]

Note that in this specification and the like, terms such as "over" and "below" are not limited to being directly above or directly below. For example, the expression of "a gate insulating layer over a gate electrode layer" does not exclude the case where another component is interposed between the gate electrode layer and the gate insulating layer. In addition, "over" and "below" are used only for convenience of the description. Unless otherwise specified, the case where the positions thereof are interchanged is included.

[0020]

Electric characteristics of an oxide semiconductor layer which employs a crystal structure having electrical anisotropy in a vicinity of a surface is changed in comparison with those of an oxide semiconductor layer which does not employ the crystal structure. For example, conductivity in a direction parallel to the surface of the oxide semiconductor layer is improved, and an insulating property in a direction vertical to the surface of the oxide semiconductor layer is improved.

[0021]

In addition, in an oxide semiconductor layer which employs a crystal structure having a function of suppressing the entry of impurities into a vicinity of the surface, the entry of impurities is suppressed in comparison with an oxide semiconductor layer which does not employ the crystal structure. For example, the entry of water, hydrogen, and the like which adversely affect an oxide semiconductor is suppressed.

[0022]

Therefore, according to one embodiment of the disclosed invention, an oxide semiconductor layer having excellent electric characteristics is provided. In addition, a highly reliable oxide semiconductor layer is provided.

[0023]

According to another embodiment of the disclosed invention, a semiconductor device having excellent characteristics is provided. In addition, a highly reliable semiconductor device is provided.

BRIEF DESCRIPTION OF DRAWINGS

[0024]

In the accompanying drawings:

FIGS. 1A and 1B are cross-sectional views illustrating a structure of an oxide semiconductor layer;

FIG. 2 is a diagram illustrating a crystal structure of $In_2Ga_2ZnO_7$;

FIGS. 3A to 3C are cross-sectional views illustrating a method for manufacturing an oxide semiconductor layer;

FIGS. 4A and 4B are bright-field-TEM images of a vicinity of a surface;

FIGS. 5A-1 to 5A-6 and 5B are electron diffraction patterns of a vicinity of a surface and cross-sectional TEM images illustrating measurement points;

FIGS. 6A-1 to 6A-3 and 6B-1 to 6B-3 are diagrams for comparing actual measurement data and simulation results of electron diffraction patterns;

FIGS. 7A and 7B are diagrams for comparing a crystal structure of $InGaZnO_4$ and a crystal structure of $In_2Ga_2ZnO_7$;

FIGS. 8A-1, 8A-2, 8B-1, and 8B-2 show simulation results of HAADF-STEM images;

FIG. 9 is a HAADF-STEM image of a cross section of crystal grains of $In_2Ga_2ZnO_7$;

FIG. 10 is a HAADF-STEM image of a cross section of crystal grains of $In_2Ga_2ZnO_7$;

FIGS. 11A to 11D are diagrams illustrating a crystal structure and a surface structure used for surface energy calculation;

FIG. 12 shows details of calculation conditions;

FIG. 13 shows calculation results of surface energy;

FIGS. 14A to 14C are diagrams illustrating a formation mechanism and a growth mechanism of the crystal grains of $In_2Ga_2ZnO_7$;

FIGS. 15A to 15D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 16A to 16D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 17A to 17D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 18A to 18D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 19A to 19D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 20A to 20D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 21A to 21D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 22A to 22D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 23A and 23B illustrate an example of a display device; and

FIGS. 24A to 24D are diagrams each showing an application of a display device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025]

Hereinafter, embodiments will be described in detail using the drawings. Note that the present invention is not limited to the description of the following embodiments, and it is apparent to those skilled in the art that modes and details can be modified in various ways without departing from the spirit of the present invention disclosed in this specification and the like. Structures of different embodiments can be implemented in an appropriate combination. Note that in the structures of the invention described below, the same portions or portions having a similar function are denoted by the same reference numerals, and the description thereof is omitted.

[0026]

(Embodiment 1)

In this embodiment, an oxide semiconductor layer according to one embodiment of the disclosed invention, a manufacturing method thereof, and the like will be described in detail with reference to FIGS. 1A and 1B, FIG. 2, FIGS. 3A to 3C, FIGS. 4A and 4B, FIGS. 5A-1 to 5A-6 and 5B, FIGS. 6A-1 to 6A-3 and 6B-1 to 6B-3, FIGS. 7A and 7B, FIGS. 8A-1, 8A-2, 8B-1, and 8B-2, FIG. 9, FIG. 10, FIGS. 11A to 11D, FIG. 12, FIG. 13, and FIGS. 14A to 14C.

[0027]

<Structure of Oxide Semiconductor Layer>

First, a structure of an oxide semiconductor layer is described with reference to FIGS. 1A and 1B and FIG. 2.

[0028]

FIGS. 1A and 1B show an example where an oxide semiconductor layer 100 is provided on a surface on which a base material 110 is to be formed. Note that any material may be used for the base material 110 as long as it can support the oxide semiconductor layer 100. The oxide semiconductor layer 100 is not limited to being provided on the surface on which the base material 110 is to be formed and may be a self-supported layer.

[0029]

The oxide semiconductor layer 100 includes an amorphous region 120 mainly formed with an amorphous oxide semiconductor and a crystal region 140 including crystal grains 130 in a vicinity of a surface of the oxide semiconductor layer 100 (see FIG. 1A). The crystal grains 130 are oriented so that the c-axis is almost vertical with

respect to the surface of the oxide semiconductor layer 100. Here, "almost vertical" means a state within ± 10° from a vertical direction.

[0030]

As examples of an oxide semiconductor material for forming the oxide semiconductor layer 100, an In-Ga-Zn-O-based oxide semiconductor material, an In-Sn-Zn-O-based oxide semiconductor material, an In-Al-Zn-O-based oxide semiconductor material, a Sn-Ga-Zn-O-based oxide semiconductor material, an Al-Ga-Zn-O-based oxide semiconductor material, a Sn-Al-Zn-O-based oxide semiconductor material, an In-Zn-O-based oxide semiconductor material, a Sn-Zn-O-based oxide semiconductor material, an Al-Zn-O-based oxide semiconductor material, an In-O-based oxide semiconductor material, a Sn-O-based oxide semiconductor material, and a Zn-O-based oxide semiconductor material are given.

[0031]

In particular, an In-Ga-Zn-O-based oxide semiconductor material has sufficiently high resistance when there is no electric field and thus off current can be sufficiently reduced. In addition, with high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is suitable for a semiconductor device.

[0032]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, one represented by $InGaO_3(ZnO)_m$ ($m>0$) is given. Note that a composition according to this representation is based on a crystal structure and is not limited to the above composition as the whole oxide semiconductor material. Alternatively, in the above, one represented by $InMO_3(ZnO)_m$ ($m>0$) can be also given using M instead of Ga. Here, M denotes one or more of metal elements selected from gallium (Ga), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. Ga is selected as M in the In-Ga-Zn-O-based oxide semiconductor material and the case where the above metal element other than Ga is selected, such as a combination of Ga and Ni or a combination of Ga and Fe, as well as the case where only Ga is used is included. In some cases, the In-Ga-Zn-O-based oxide semiconductor material may contain impurities such as a transition metal element and an oxide thereof in addition to a metal element contained as M.

[0033]

The amorphous region 120 mainly contains an amorphous oxide semiconductor. Note that "mainly" means a state where one occupies 50 % or more, for example. In this case, it is a state where the amorphous oxide semiconductor occupies 50 % or more at volume% (or weight%). That is, other than an amorphous oxide semiconductor, the amorphous region 120 includes crystals of an oxide semiconductor in some cases, and the percentage of content thereof is preferably less than 50 % at volume% (or weight%). Note that it can be said that an essence of the disclosed invention is the structure of the crystal region 140; therefore, the structure of the amorphous region 120 is not necessarily limited to the above structure as long as required characteristics can be obtained.

[0034]

In the case where the In-Ga-Zn-O-based oxide semiconductor material is used, the composition of the above amorphous region 120 is preferably set so that a Zn content (atomic%) is less than an In or Ga content (atomic%). With the use of such a composition, the crystal grains 130 of a predetermined composition are easily formed in the crystal region 140.

[0035]

The crystal region 140 in the vicinity of the surface includes the crystal grains 130 in which c-axis is oriented in an almost vertical direction with respect to the surface of the oxide semiconductor layer 100 (see FIG. 1B). For example, in the case of using an In-Ga-Zn-O-based oxide semiconductor material, in the crystal region 140, the c-axis of the crystal grains of $In_2Ga_2ZnO_7$ is oriented in an almost vertical direction with respect to the surface of the oxide semiconductor layer 100. Note that a "vicinity of a surface (surface vicinity)" means, for example, a region in which a distance (depth) from the surface is 20 nm or less. Note that the case where the thickness of the oxide semiconductor layer 100 is large is not limited to this. For example, in the case where the oxide semiconductor layer 100 has a thickness of 200 nm or more, a "vicinity of a surface (surface vicinity)" means a region in which a distance (depth) from the surface is 10 % or lower of the thickness of the oxide semiconductor layer.

[0036]

The crystals of $In_2Ga_2ZnO_7$ include any of In, Ga, and Zn, and can be considered to have a stacked-layer structure of layers parallel to a-axis and b-axis (see FIG. 2). That is, the crystals of $In_2Ga_2ZnO_7$ have a structure in which a first layer containing In, a second layer without In (containing Ga or Zn), a third layer without In (containing Ga or Zn), a fourth layer containing In, and a fifth layer without In (containing Ga or Zn) are stacked in a c-axis direction.

[0037]

Since electrical conductivity of the crystals of $In_2Ga_2ZnO_7$ are controlled mainly by In, electric characteristics of the first layer containing In and the fourth layer containing In which is related to a direction parallel to the a-axis and the b-axis are preferable. This is because one of a 5s orbital of In is overlapped with an adjacent 5s orbital of In in the first layer containing In or the fourth layer containing In, so that a carrier path is formed. On the other hand, it can be said that an insulating property in a direction vertical to the above layer (that is, the c-axis direction) is increased.

[0038]

When such crystal grains having electrical anisotropy are oriented, an effect on electric characteristics of the oxide semiconductor layer 100 also arises. Specifically, for example, electric characteristics in a direction parallel to the surface of the oxide semiconductor layer 100 are increased. This is because the c-axis of the crystal grains of $In_2Ga_2ZnO_7$ is oriented in an almost vertical direction with respect to the surface of the oxide semiconductor layer 100, and current flows in a direction parallel to the a-axis and the b-axis in $In_2Ga_2ZnO_7$ crystals.

[0039]

Note that the crystal region 140 may include crystal grains other than the crystal grains 130. The crystal structure of the crystal grains is not limited to the above structure, and the crystal region 140 may include crystal grains of another structure. For example, in the case of using an In-Ga-Zn-O-based oxide semiconductor material, crystal grains of $InGaZnO_4$ may be included in addition to crystal grains of $In_2Ga_2ZnO_7$. Needless to say, the case where crystal grains of $In_2Ga_2ZnO_7$ exist in the whole crystal region 140 is more effective and more preferable.

[0040]

The length (size) of the crystal grains in a c-axis direction is preferably less

than five times as long as the length (size) in an a-axis direction or a b-axis direction, more preferably less than three times. This is because when the thickness of the crystal region 140 is too large (that is, when the length of the crystal grains 130 in a c-axis direction is too long), there is a possibility that characteristics of the oxide semiconductor layer 100 may depend only on the crystal region 140 and desired characteristics cannot be obtained.

[0041]

As described above, when the oxide semiconductor layer 100 has the crystal region 140 in the vicinity of the surface, favorable electric characteristics can be achieved. In particular, when the crystal region 140 is formed so as to include the crystal grains of $In_2Ga_2ZnO_7$ whose c-axis is oriented in an almost vertical direction with respect to the surface of the oxide semiconductor layer 100, excellent electric characteristics can be realized by anisotropy in electric characteristics of the crystal grains of $In_2Ga_2ZnO_7$.

[0042]

Further, the crystal region 140 is more stable than the amorphous region 120; therefore, when the crystal region 140 is included in the vicinity of the surface of the oxide semiconductor layer 100, the entry of impurities (e.g., moisture and the like) into the amorphous region 120 can be suppressed. Thus, the reliability of the oxide semiconductor layer 100 can be increased.

[0043]

<Method for Manufacturing Oxide Semiconductor Layer>

Next, a method for manufacturing the oxide semiconductor layer 100 will be described with reference to FIGS. 3A to 3C.

[0044]

An oxide semiconductor layer 200 which is to be the oxide semiconductor layer 100 later is formed using the oxide semiconductor material described in <Structure of Oxide Semiconductor Layer>. The oxide semiconductor layer 200 is formed by a sputtering method or the like under an atmosphere of a rare gas such as argon, under an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen (see FIG. 3A). When a target including SiO_2 at 2 weight% to 10 weight% inclusive is used in a

sputtering method, SiO_x ($x>0$) is included in the oxide semiconductor layer 200, so that crystallization of the oxide semiconductor layer 200 can be suppressed. This method is particularly effective in the case where the oxide semiconductor layer 200 which is amorphous is desired to be obtained.

[0045]

For example, an In-Ga-Zn-O-based amorphous oxide semiconductor layer can be obtained as the oxide semiconductor layer 200 using a metal oxide target containing In, Ga, and Zn (such as a target having a composition ratio of In:Ga:Zn = 1:1:0.5 [atom%], In:Ga:Zn = 1:1:1 [atom%], and In:Ga:Zn = 1:1:2 [atom%]) under the following conditions: the distance between the substrate and the target is 100 mm; the pressure is 0.6 Pa; the direct current power is 0.5 kW; and the atmosphere is an oxygen atmosphere (the proportion of the oxygen flow is 100 %). Note that the case where a pulse direct current power source is used as a power source is preferable because powder substances (also referred to as particles or dust) generated in film formation can be reduced and thickness distribution can be evened.

[0046]

The thickness of the oxide semiconductor layer 200 can be set as appropriate in accordance with an objective purpose or objective characteristics. For example, it may be approximately 20 nm to 10 μm.

[0047]

The crystal region 140 is formed through heat treatment after the oxide semiconductor layer 200 is formed (see FIG. 3B). Note that since H_2, H, OH, and the like in the oxide semiconductor layer 200 are eliminated through the heat treatment, the heat treatment can be called dehydration treatment or dehydrogenation treatment.

[0048]

Rapid thermal anneal (RTA) treatment in which a high-temperature inert gas (a nitrogen gas, a rare gas, or the like) is used can be employed as the above heat treatment. Here, the temperature of the heat treatment is preferably 500 °C or higher. Note that there is no requirement for the upper limit of the heat treatment temperature from an essential part of the invention; however, it is required to be in the range of allowable temperature limit when the base material 110 is used as a support. The length of the

heat treatment is preferably greater than or equal to 1 minute and less than or equal to 10 minutes. For example, RTA treatment is preferably performed at 650 °C for approximately 3 minutes to 6 minutes. By employing the RTA treatment, heat treatment can be performed for a short time; therefore, adverse effect of heat on the base material 110 can be reduced. That is, the upper limit of the heat treatment temperature can be increased in this case as compared with the case where heat treatment is performed for a long time. Further, the crystal grains of a predetermined structure can be selectively formed in the vicinity of the surface.

[0049]

Note that the above heat treatment may be performed at any timing as long as it is performed after the oxide semiconductor layer 200 is formed; however, in order to promote dehydration or dehydrogenation, the heat treatment is preferably performed before other components are formed on a surface of the oxide semiconductor layer 200. In addition, the heat treatment may be performed plural times instead of once.

[0050]

Note that it is preferable that in the above heat treatment, hydrogen (including water) and the like be not contained in the treatment atmosphere. For example, the purity of an inert gas which is introduced into a heat treatment apparatus is set to 6N (99.9999 %, that is, an impurity concentration is 1 ppm or lower) or more, preferably, 7N (99.99999 %, that is, an impurity concentration is 0.1 ppm or lower) or more.

[0051]

Through the above heat treatment, the oxide semiconductor layer 100 which includes the amorphous region 120 which is mainly amorphous and the crystal region 140 including the crystal grains 130 which is oriented so that the c-axis is almost vertical with respect to the surface of the oxide semiconductor layer is formed (see FIG. 3C).

[0052]

Note that the above crystal region 140 has a function of suppressing the entry of impurities into a film; however, when a large number of impurities exist, it is difficult to suppress the entry completely. Therefore, it is important that the oxide semiconductor layer 100 be not made in contact with water, hydrogen, and the like after

the above heat treatment as much as possible. This can be achieved in such a manner that the substrate is not exposed to the atmosphere in the heat treatment and a following temperature decreasing process. For example, the heat treatment and the following temperature decreasing process may be performed in one atmosphere. It is needless to say that the atmosphere in the temperature decreasing process may be different from the heat treatment atmosphere. In this case, the atmosphere in the temperature decreasing process can be, for example, an oxygen gas atmosphere, an N_2O gas atmosphere, an ultra-dry air (having a dew point of –40 °C or lower, preferably, –60 °C or lower), or the like.

[0053]

<About Growth Mechanism of Crystal Grains>

An example of a growth mechanism of crystal grains in an In-Ga-Zn-O-based amorphous oxide semiconductor layer will be described below with reference to FIGS. 4A and 4B, FIGS. 5A-1 to 5A-6 and 5B, FIGS. 6A-1 to 6A-3 and 6B-1 to 6B-3, FIGS. 7A and 7B, FIGS. 8A-1, 8A-2, 8B-1, and 8B-2, FIG. 9, FIG. 10, FIGS. 11A to 11D, FIG. 12, FIG. 13, and FIGS. 14A to 14C.

[0054]

First, a state where the crystal grains of $In_2Ga_2ZnO_7$ are c-axis-oriented in the vicinity of the surface of the In-Ga-Zn-O-based amorphous oxide semiconductor layer is shown together with results of experimental observation.

[0055]

As the In-Ga-Zn-O-based amorphous oxide semiconductor layer, a film which is formed with a thickness of 50 nm over the glass substrate by a DC sputtering method is used. In addition, as a sputtering target, a target having a composition ratio of In:Ga:Zn = 1:1:0.5 [atom%] was used. Other deposition conditions were as follows: the direct current power was 0.5 kW; the deposition pressure was 0.6 Pa; the deposition atmosphere was an oxygen atmosphere (the proportion of the oxygen flow is 100 %); and the substrate temperature was room temperature.

[0056]

The In-Ga-Zn-O-based amorphous oxide semiconductor layer was subjected to RTA treatment so that the crystal grains of $In_2Ga_2ZnO_7$ were c-axis-oriented in the

vicinity of the surface. The heat treatment conditions were as follows: the atmosphere was a nitrogen atmosphere under atmospheric pressure; the temperature was 650 °C; and the time was set to 6 minutes.

[0057]

In order to observe a cross section of the sample formed in such a manner, reduction in thickness by an Ar ion milling method (acceleration voltage: 5 kV) or a reduction in thickness by an FIB milling method (irradiation ion: Ga, acceleration voltage: processing at 5 kV after processing at 40 kV) was performed after mechanical polishing. Note that PIPS manufactured by Gatan, Inc. was used in an Ar ion milling method and NB-5000 and FB-2100 manufactured by Hitachi, Ltd. was used in an FIB milling method.

[0058]

FIGS. 4A and 4B are bright-field-TEM images of the vicinity of the surface of the sample. Note that the TEM images are images which are observed under a condition in which the acceleration voltage was 300 kV using H-9000NAR manufactured by Hitachi, Ltd.. In FIGS. 4A and 4B, it can be observed that a crystal region including crystal grains with a width of 1 nm to 3 nm inclusive and a depth of 2 nm to 4 nm inclusive is formed in the vicinity of the surface of an In-Ga-Zn-O-based oxide semiconductor layer with a thickness of 50 nm.

[0059]

FIG. 5A-1 is a cross-sectional TEM image of the vicinity of the surface of the sample. FIG. 5A-2 is an electron diffraction pattern corresponding to reference numeral 1 in the cross-sectional TEM image. FIG. 5A-3 is an electron diffraction pattern corresponding to reference numeral 2 in the cross-sectional TEM image. FIG. 5A-4 is an electron diffraction pattern corresponding to reference numeral 3 in the cross-sectional TEM image. FIG. 5A-5 is an electron diffraction pattern corresponding to reference numeral 4 in the cross-sectional TEM image. FIG. 5A-6 is an electron diffraction pattern corresponding to reference numeral 5 in the cross-sectional TEM image. In each of the electron diffraction patterns, an obvious spot in which d value is 0.29 nm to 0.30 nm inclusive is shown. A direction of the spots corresponds to the c-axis direction of the crystal.

[0060]

FIG. 5B is a cross-sectional TEM image which shows a relation of the c-axis direction and the surface. Arrows in the drawing indicates the c-axis direction of the crystal grains at each point. From FIG. 5B, it is found that the c-axis (<001> direction) is almost vertical with respect to the surface. It is also found that the c-axis direction reflects flatness of the surface.

[0061]

Next, a detailed analysis of the electron diffraction patterns was conducted to determine crystal structures of the crystal grains. FIGS. 6A-1 to 6A-3 show typical actual measurement data of the electron diffraction patterns and FIGS. 6B-1 to 6B-3 show simulation results (assuming $In_2Ga_2ZnO_7$ crystals) corresponding to the actual measurement data. By comparison of the actual measurement data and the simulation results, the crystal structure of the crystal grains can be confirmed to be $In_2Ga_2ZnO_7$.

[0062]

In FIGS. 7A and 7B, comparison of a crystal structure ($InGaZnO_4$) in which m is 1 in a homologous structure of $InGaO_3(ZnO)_m$ (m is a natural number) (see FIG. 7A) and a crystal structure of $In_2Ga_2ZnO_7$ (see FIG. 7B) is shown.

[0063]

In the structure of $InGaZnO_4$, two layers of GaO or ZnO exist between layers of In and O (InO layers) which are vertical with respect to the c-axis (<001> direction). On the other hand, in the structure of $In_2Ga_2ZnO_7$, one layer and two layers of GaO or ZnO exist alternately and repeatedly between InO layers. A lattice constant in the c-axis direction of $InGaZnO_4$ is 2.61 nm, and that of $In_2Ga_2ZnO_7$ is 2.95 nm.

[0064]

Next, observation of HAADF (high-angle annular dark field)-STEM images in the crystal structure of $InGaZnO_4$ and the crystal structure of $In_2Ga_2ZnO_7$ is described. FIG. 8A-1 shows simulation results of the crystal structure of $InGaZnO_4$ and FIG. 8A-2 is a HAADF-STEM image of the crystal structure of $InGaZnO_4$. FIG. 8B-1 shows simulation results of the crystal structure of $In_2Ga_2ZnO_7$ and FIG. 8B-2 is a HAADF-STEM image of the crystal structure of $In_2Ga_2ZnO_7$. Note that FIG. 8A-1 and FIG. 8B-1 each show the crystal structure seen from a (100) plane.

[0065]

In a HAADF-STEM image, a contrast proportional to the square of an atomic number is obtained; therefore, the brighter dot indicates the heavier atom. That is, in the above four-component structure, brighter dots represent In atoms and darker dots represent Ga or Zn atoms. In addition, O atoms do not appear as images because they are smaller in mass than the above atoms. Thus, a HAADF-STEM image is an innovative observation method in terms that a structure at the atomic level can be imaged easily and directly.

[0066]

HAADF-STEM images of a cross section of the crystal grains of $In_2Ga_2ZnO_7$ in the vicinity of the surface of the sample are shown in FIG. 9 and FIG. 10. For the observation, a Schottky field emission STEM with a spherical aberration correcting function (HD-2700 manufactured by Hitachi, Ltd., spherical aberration Cs: 5 μm or less) was used. The acceleration voltage was set to 200 kV and the detection angle was set to greater than or equal to 40 mrad and less than or equal to 210 mrad. In FIG. 9 and FIG. 10, intensity difference between In atoms, and Ga atoms or Zn atoms is not obvious unlike in FIGS. 8A-1, 8A-2, 8B-1, and 8B-2. This is considered to be due to the fact that sufficient signal intensity cannot be obtained because the crystal grains are minute.

[0067]

When FIG. 9 is observed in detail, a structure in which two layers containing Ga or Zn exist between layers containing In (the distance between the layers containing In: 0.89 nm) and a structure in which one layer containing Ga or Zn exist between the layers containing In (the distance between the layers containing In: 0.62 nm) can be confirmed. In FIG. 10, a more characteristic structure can be confirmed. An outermost surface layer does not contain In in most of the region. This indicates that the outermost surface is a layer containing Ga or Zn. This is an interesting fact to understand a formation mechanism of the crystal grains.

[0068]

Next, based on the above observation results, a formation mechanism of crystal nuclei and a growth mechanism of the crystals in the vicinity of a surface of the oxide semiconductor layer were confirmed by computer calculation.

[0069]

In order to examine the plane orientation of a seed crystal related to crystal growth, surface energy of $In_2Ga_2ZnO_7$ (a symmetry property of a crystal: P63/MMC), In_2O_3 (a symmetry property of a crystal: R-3C), Ga_2O_3 (a symmetry property of a crystal: R-3C), and ZnO (a symmetry property of a crystal: P63MC) was obtained by first principle calculation. Here, surface energy means energy per unit area which is needed to cut out a crystal surface from a bulk crystal. That is, it can be said that as surface energy is larger, a surface structure is more unstable in terms of energy and a seed crystal is difficult to generate.

[0070]

CASTEP which is first principle calculation software based on the density functional theory is used for the above calculation. In the above calculation, surface energy is obtained from the following formula (1).

[0071]

[Formula 1]

$$(\text{Surface energy}) = \frac{(\text{Energy of surface structure}) - (\text{Energy of crystal structure})}{(\text{Surface area})} \cdots (1)$$

[0072]

Ga and Zn are adjacent to each other in the periodic table, and atomic radiuses thereof are almost the same; therefore, arrangements thereof are random. That is, in some cases, Zn is arranged in a site in which Ga is arranged, and Ga is arranged in a site in which Zn is arranged. In order to deal with such a random arrangement, a virtual crystal approximation was used in the calculation. That is, a composition ratio of Ga to Zn is set to 2:1 in a site in which Ga or Zn is arranged, and a virtual atom in which Ga is 66.7 % and Zn is 33.3 % is arranged. More specifically, pseudopotentials of atoms were mixed at the above proportion and were assigned to virtual atoms.

[0073]

FIG. 11A shows a crystal structure used for the surface energy calculation of (001) plane of $In_2Ga_2ZnO_7$ and FIGS. 11B to 11D show the surface structures used for the surface energy calculation. FIG. 11B shows a structure in which O is on the outermost surface in the (001) plane (denoted by "(001):(Ga, Zn)O"), FIG. 11C shows a structure in which In is on the outermost surface in the (001) plane (denoted by

"(001):In"), and FIG. 11D shows a structure in which Ga or Zn is on the outermost surface in the (001) plane (denoted by "(001):Ga, Zn"). Lattices of FIGS. 11B to 11D are taken so that they are minimum units of a periodic structure in an in-plane direction. Therefore, the sizes of the lattices in the in-plane direction of the (001) plane are different depending on the surface structure. Note that structures after structure optimization by first principle calculation are shown in FIGS. 11B to 11D. Ga or Zn is on the outermost surface in (001):Ga, Zn before structure optimization; however, O is on the outermost surface by structure optimization.

[0074]

The calculation was performed in the following manner: after the most stable structure of the crystal including lattices is obtained, a crystal surface is cut out, and structure optimization is performed only on atom arrangement with the lattices fixed. Note that a thickness of a vacuum region where atoms do not exist was set to 1 nm. The details of the calculation conditions are shown in FIG. 12. In consideration of no periodicity in a direction vertical to the surface, the number of k point was 1. Similar calculations were also performed on the (100) plane of $In_2Ga_2ZnO_7$, In_2O_3, Ga_2O_3, and ZnO.

[0075]

The calculation results of the surface energy are shown in FIG. 13. From FIG. 13, it can be found that in the surface structure of $In_2Ga_2ZnO_7$, the surface energy of (001):(Ga, Zn)O is the smallest. In, Ga, and Zn are metallic and become unstable in terms of energy due to the existence of surface charge. On the other hand, when a bond is terminated by O, the surface energy can be reduced.

[0076]

From the calculation results of the surface energy, it can be easily understood that (001):In is difficult to form. This can be supported also from the observation results of FIG. 10 and the like.

[0077]

By comparison of the surface energy of (001):(Ga, Zn)O and the surface energy of the (001) plane of ZnO, a formation mechanism and a growth mechanism of the crystal grains of $In_2Ga_2ZnO_7$ can be understood. The formation mechanism and the

growth mechanism of the crystal grains of $In_2Ga_2ZnO_7$ will be briefly described with reference to FIGS. 14A to 14C.

[0078]

The vapor pressure of ZnO is large and is easily vaporized. Thus, when heat treatment is performed, the composition ratio of Zn becomes small and that of Ga becomes large in the vicinity of the surface of the In-Ga-Zn-O-based amorphous oxide semiconductor layer (see FIG. 14A). When the surface energy of (001):(Ga, Zn)O and the surface energy of the (001) plane of ZnO are compared, the surface energy of (001):(Ga, Zn)O is small. A layer containing ZnO and GaO is formed on a surface, and the amount of ZnO is small on a surface thereof; therefore, a layer containing GaO is stably formed (see FIG. 14B). Accordingly, the crystal grains of $In_2Ga_2ZnO_7$ are grown from the above layer containing GaO (see FIG. 14C). That can be easily understood when it is assumed that the outermost surface is a layer containing Ga and the second layer is a layer containing In in FIG. 10.

[0079]

Note that the surface energy of (001):(Ga, Zn)O of $In_2Ga_2ZnO_7$ is smaller than those of the main planes of In_2O_3, Ga_2O_3, and ZnO. Thus, it can be said that In_2O_3, Ga_2O_3, and ZnO are not separated from each other on the surface of the oxide semiconductor layer as far as it is determined in terms of the surface energy.

[0080]

In crystal growth, on a plane having small surface energy, crystal grains tend to be formed more easily and crystals tend to be grown more easily, than on a plane having large surface energy. Therefore, (001):(Ga, Zn)O of $In_2Ga_2ZnO_7$ is likely to be crystallized in comparison with In_2O_3, Ga_2O_3, ZnO, and the like. In addition, the surface energy of (001):(Ga, Zn)O is smaller than those of the (100) plane of $In_2Ga_2ZnO_7$, (001):In, and (001):Ga, Zn. Thus, the outermost surface is likely to be (001):(Ga, Zn)O and be c-axis-oriented.

[0081]

As described above, it can be seen that by heating the surface of the oxide semiconductor layer, the crystal grains of $In_2Ga_2ZnO_7$ which is c-axis-oriented are formed in the vicinity of the surface and grown. The oxide semiconductor layer has

excellent electric characteristics, which is suitable for a semiconductor device. Alternatively, the oxide semiconductor layer has high reliability, which is suitable for a semiconductor device.

[0082]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0083]

(Embodiment 2)

In this embodiment, an example of a transistor as a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 15A to 15D and FIGS. 16A to 16D.

[0084]

First, a conductive layer 302 is formed over a substrate 300 (see FIG. 15A).

[0085]

Any substrate can be used for the substrate 300 as long as it is a substrate having an insulating surface, for example, a glass substrate. It is preferable that the glass substrate be a non-alkali glass substrate. As a material of the non-alkali glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Besides, as the substrate 300, an insulating substrate formed using an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate, a semiconductor substrate which is formed using a semiconductor material such as silicon and whose surface is covered with an insulating material, or a conductive substrate which is formed using a conductive material such as metal or stainless steel and whose surface is covered with an insulating material can be used. A plastic substrate can also be used as long as it can withstand heat treatment in a manufacturing process.

[0086]

The conductive layer 302 is preferably formed using a conductive material such as aluminum (Al), copper (Cu), molybdenum (Mo), tungsten (W), or titanium (Ti). As a formation method, a sputtering method, a vacuum evaporation method, a CVD method, and the like are given. In the case of using aluminum (or copper) for the

conductive layer 302, since aluminum itself (or copper itself) has disadvantages such as low heat resistance and a tendency to be corroded, it is preferably formed in combination with a conductive material having heat resistance.

[0087]

As the conductive material having heat resistance, it is possible to use metal containing an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc), an alloy containing any of these elements as its component, an alloy containing a combination of any of these elements, a nitride containing any of these elements as its component, or the like. The conductive layer 302 may be formed by stacking the conductive material having heat resistance and aluminum (or copper).

[0088]

Although not shown in the drawings, the substrate 300 may be provided with a base layer. The base layer has a function of preventing diffusion of an alkali metal (Li, Cs, Na, or the like), an alkaline earth metal (Ca, Mg, or the like), or other impurities from the substrate 300. In other words, provision of the base layer can realize improvement in the reliability of the semiconductor device. The base layer may be formed to have a single-layer structure or a stacked-layer structure using a variety of insulating materials such as silicon nitride or silicon oxide. Specifically, for example, a structure in which silicon nitride and silicon oxide are stacked in that order over the substrate 300 is favorable. This is because silicon nitride has a high blocking effect against an impurity. At the same time, in the case where silicon nitride is in contact with a semiconductor, there is a possibility that a problem occurs in the semiconductor element; thus, silicon oxide is preferably applied as a material to be in contact with the semiconductor.

[0089]

Next, a resist mask 304 is selectively formed over the conductive layer 302 and the conductive layer 302 is selectively etched using the resist mask 304, whereby a conductive layer 306 which functions as a gate electrode is formed (see FIG. 15B).

[0090]

The resist mask 304 is formed through steps such as application of a resist

material, light exposure using a photomask, and development. For the application of the resist material, a method such as a spin-coating method can be employed. Instead, the resist mask 304 may be selectively formed by a droplet discharging method, a screen printing method, or the like. In this case, the steps of light exposure using a photomask, development, and the like are not needed; therefore, improvement in productivity can be achieved. Note that the resist mask 304 is removed after the conductive layer 306 is formed by etching the conductive layer 302.

[0091]

The resist mask 304 may be formed using a multi-tone mask. Here, the multi-tone mask is a mask capable of light exposure with multi-level light intensity. With the use of a multi-tone mask, one-time exposure and development process allow a resist mask with plural thicknesses (typically, two kinds of thicknesses) to be formed. By use of the multi-tone mask, increase in the number of steps can be suppressed.

[0092]

As the above etching treatment, dry etching may be used, or wet etching may be used. In order to improve coverage of a gate insulating layer or the like which is formed later and prevent disconnection, the etching is preferably performed so that end portions of the conductive layer 306 are tapered. For example, the end portions are preferably tapered at a taper angle 20° or more and less than 90°. Here, the "taper angle" refers to an angle formed by a side surface of a layer which is tapered to a bottom surface thereof when the layer having a tapered shape is observed from a cross-sectional direction.

[0093]

Next, an insulating layer 308 which functions as a gate insulating layer is formed so as to cover the conductive layer 306 (see FIG. 15C). The insulating layer 308 can be formed using a material such as silicon oxide, silicon oxynitride, silicon nitride, silicon nitride oxide, aluminum oxide, or tantalum oxide. The insulating layer 308 may also be formed by stacking films formed of these materials. These films are preferably formed to a thickness of 5 nm or more and 250 nm or less by a sputtering method or the like. For example, as the insulating layer 308, a silicon oxide film can be formed to a thickness of 100 nm by a sputtering method.

[0094]

Alternatively, the insulating layer 308 with a stacked-layer structure may be formed by combination of a sputtering method and a CVD method (a plasma CVD method or the like). For example, a lower layer of the insulating layer 308 (a region in contact with the conductive layer 306) is formed by a plasma CVD method and an upper layer of the insulating layer 308 can be formed by a sputtering method. Since a film with favorable step coverage is easily formed by a plasma CVD method, it is suitable for a method for forming a film directly above the conductive layer 306. In the case of using a sputtering method, since it is easy to reduce hydrogen concentration in the film as compared with the case of using a plasma CVD method, by providing a film by a sputtering method in a region in contact with a semiconductor layer, the hydrogen in the insulating layer 308 can be prevented from being diffused into the semiconductor layer. Specifically, in an oxide semiconductor layer, since hydrogen has a great influence on characteristics, it is effective to employ such a structure.

[0095]

Note that in this specification and the like, an oxynitride refers to a substance that contains more oxygen (atoms) than nitrogen (atoms). For example, a silicon oxynitride is a substance including oxygen, nitrogen, silicon, and hydrogen in ranges of 50 at.% to 70 at.%, 0.5 at.% to 15 at.%, 25 at.% to 35 at.%, and 0.1 at.% to 10 at.%, respectively. Further, nitride oxide refers to a substance that contains more nitrogen (atoms) than oxygen (atoms). For example, a silicon nitride oxide is a substance including oxygen, nitrogen, silicon, and hydrogen in ranges of 5 at.% to 30 at.%, 20 at.% to 55 at.%, 25 at.% to 35 at.%, and 10 at.% to 25 at.%, respectively. Note that the above ranges are obtained by measurement using Rutherford backscattering spectrometry (RBS) or hydrogen forward scattering spectrometry (HFS). Moreover, the total of the content rate of the constituent elements does not exceed 100 at.%.

[0096]

Next, a semiconductor layer 310 is formed so as to cover the insulating layer 308 (see FIG. 15D). In this embodiment, the oxide semiconductor layer described in the above embodiment is applied to the semiconductor layer 310. The above embodiment can be referred to for details of the oxide semiconductor layer.

[0097]

Note that in this embodiment, the case where the semiconductor layer 310 is formed using a single layer is described; however, the semiconductor layer 310 may be formed using a stacked-layer structure. For example, the semiconductor layer 310 may be formed by stacking two or more oxide semiconductor layers each of which has a different composition over the insulating layer 308. Alternatively, the semiconductor layer 310 may be formed by stacking two or more oxide semiconductor layers each of which has different crystallinity.

[0098]

Next, a resist mask 312 is selectively formed over the semiconductor layer 310 and the semiconductor layer 310 is selectively etched using the resist mask 312, whereby a semiconductor layer 314 is formed (see FIG. 16A). Here, the resist mask 312 can be formed in a manner similar to that of the resist mask 304. Note that the resist mask 312 is removed after the semiconductor layer 314 is formed by etching the semiconductor layer 310.

[0099]

Either wet etching or dry etching can be employed as an etching method used for the etching of the semiconductor layer 310. For example, an unnecessary portion of the semiconductor layer 310 is removed by wet etching using a mixed solution of acetic acid, nitric acid, and phosphoric acid, so that the semiconductor layer 314 can be formed. Note that an etchant (an etching solution) used in the above wet etching may be any solution which can etch the semiconductor layer 310, and not limited to the above-described solution.

[0100]

When dry etching is performed, for example, a gas including chlorine or a gas including chlorine to which oxygen is added is preferably used. This is because by using a gas including chlorine, etching selectivity of the semiconductor layer 310 with respect to the conductive layer or the base layer can be easily obtained.

[0101]

As an etching apparatus used for the dry etching, an etching apparatus using a reactive ion etching method (an RIE method), or a dry etching apparatus using a high-density plasma source such as electron cyclotron resonance (ECR) or inductively

coupled plasma (ICP) can be used. An enhanced capacitively coupled plasma (ECCP) mode etching apparatus may be used by which uniform electric discharge can be obtained over a wide area as compared with an ICP etching apparatus. This ECCP mode etching apparatus can be employed even when a substrate of the tenth generation or later is used.

[0102]

Next, a conductive layer 316 is formed so as to cover the insulating layer 308 and the semiconductor layer 314 (see FIG. 16B). The conductive layer 316 can be formed using a material and by a method which are similar to those of the conductive layer 302. For example, the conductive layer 316 can be formed to have a single-layer structure of a molybdenum layer or a titanium layer. Alternatively, the conductive layer 316 may be formed to have a stacked-layer structure and can have a stacked-layer structure of an aluminum layer and a titanium layer, for example. A three-layer structure in which a titanium layer, an aluminum layer, and a titanium layer are stacked in this order may be employed. A three-layer structure in which a molybdenum layer, an aluminum layer, and a molybdenum layer are stacked in this order may be employed. Further, an aluminum layer containing neodymium (an Al-Nd layer) may be used as the aluminum layer used for these stacked-layer structures. Further alternatively, the conductive layer 316 may have a single-layer structure of an aluminum layer containing silicon.

[0103]

Next, a resist mask 318 and a resist mask 320 are selectively formed over the conductive layer 316 and the conductive layer 316 is selectively etched using the resist masks so as to form a conductive layer 322 which functions as one of a source electrode and a drain electrode and a conductive layer 324 which functions as the other of the source electrode and the drain electrode (see FIG. 16C). Here, the resist masks 318 and 320 can be formed in a manner similar to that of the resist mask 304. Note that the resist masks 318 and 320 are removed after the conductive layers 322 and 324 are formed by etching the conductive layer 316.

[0104]

Note that either wet etching or dry etching can be employed as a method for etching the conductive layer 316.

[0105]

Next, an insulating layer 326 is formed so as to cover the conductive layer 322, the conductive layer 324, the semiconductor layer 314, and the like (see FIG. 16D). Here, the insulating layer 326 serves as a so-called interlayer insulating layer. The insulating layer 326 can be formed using a material such as silicon oxide, aluminum oxide, or tantalum oxide. The insulating layer 326 may also be formed by stacking films formed of these materials. Through the above steps, a transistor 350 using an oxide semiconductor layer is completed (see FIG. 16D).

[0106]

As described in this embodiment, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, the entry of impurities (e.g., moisture and the like) into the oxide semiconductor layer can be suppressed. Thus, the reliability of the semiconductor device can be increased.

[0107]

Further, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, a semiconductor device with favorable electric characteristics can be provided.

[0108]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0109]

(Embodiment 3)

In this embodiment, another example of a transistor as a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 17A to 17D and FIGS. 18A to 18D. Note that many parts of a method for manufacturing a semiconductor device in this embodiment are common to those in the above embodiments; therefore, description of the common parts is omitted below and only different parts will be described in detail.

[0110]

First, a conductive layer 402 is formed over a substrate 400 (see FIG. 17A). The above embodiments (the description with reference to FIG. 4A and the like) can be

referred to for the details of the substrate 400, the conductive layer 402, and the like. A base layer may be formed over the substrate 400. The above embodiment can also be referred to for the details of the base layer.

[0111]

Next, a resist mask 404 is selectively formed over the conductive layer 402 and the conductive layer 402 is selectively etched using the resist mask 404, whereby a conductive layer 406 which functions as a gate electrode is formed (see FIG. 17B). The above embodiment (the description with reference to FIG. 15B and the like) can be referred to for the details of the resist mask 404, the conductive layer 406, the etching, and the like.

[0112]

Then, an insulating layer 408 which functions as a gate insulating layer is formed so as to cover the conductive layer 406 (see FIG. 17C). The above embodiment (the description with reference to FIG. 15C and the like) can be referred to for the details of the insulating layer 408 and the like.

[0113]

A conductive layer 410 is formed so as to cover the insulating layer 408 (see FIG. 17D). The conductive layer 410 can be formed using a material and by a method which are similar to those of the conductive layer 402. In other words, the above embodiment (the description with reference to FIG. 15A, FIG. 16B, and the like) can be referred to for the details.

[0114]

Next, a resist mask 412 and a resist mask 414 are selectively formed over the conductive layer 410 and the conductive layer 410 is selectively etched using the resist masks so as to form a conductive layer 416 which functions as one of a source electrode and a drain electrode and a conductive layer 418 which functions as the other of the source electrode and the drain electrode (see FIG. 18A). The resist masks 412 and 414 can be formed in a manner similar to that of the resist mask 404. Either wet etching or dry etching can be employed as a method for etching the conductive layer 410. In other words, the above embodiment (the description with reference to FIG. 15B, FIG. 16C, and the like) can be referred to for the details of the resist masks and the etching.

[0115]

Next, a semiconductor layer 420 is formed so as to cover the insulating layer 408, the conductive layer 416, the conductive layer 418 and the like (see FIG. 18B). In this embodiment, the oxide semiconductor layer described in the above embodiment is applied to the semiconductor layer 420. The above embodiment can be referred to for the details of the oxide semiconductor layer.

[0116]

Next, a resist mask 422 is selectively formed over the semiconductor layer 420 and the semiconductor layer 420 is selectively etched using the resist mask 422 so as to form a semiconductor layer 424 (see FIG. 18C). The above embodiment (the description with reference to FIG. 15B, FIG. 16A, and the like) can be referred to for the details of the resist mask and the etching.

[0117]

Then, an insulating layer 426 is formed so as to cover the conductive layer 416, the conductive layer 418, the semiconductor layer 424, and the like (see FIG. 18D). Here, the insulating layer 426 serves as a so-called interlayer insulating layer. The insulating layer 426 can be formed using a material such as silicon oxide, aluminum oxide, or tantalum oxide. The insulating layer 426 may also be formed by stacking films formed of these materials. Through the above steps, a transistor 450 using an oxide semiconductor layer is completed (see FIG. 18D).

[0118]

As described in this embodiment, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, the entry of impurities (e.g., moisture and the like) into the oxide semiconductor layer can be suppressed. Thus, the reliability of the semiconductor device can be increased.

[0119]

Further, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, a semiconductor device with favorable electric characteristics can be provided.

[0120]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0121]

(Embodiment 4)

In this embodiment, another example of a transistor as a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 19A to 19D and FIGS. 20A to 20D. Note that many parts of a method for manufacturing a semiconductor device in this embodiment are common to those in the above embodiments; therefore, description of the common parts is omitted below and only different parts will be described in detail.

[0122]

First, a semiconductor layer 502 is formed over a substrate 500 (see FIG. 19A). After a resist mask 504 is selectively formed over the semiconductor layer 502, the semiconductor layer 502 is selectively etched using the resist mask 504, whereby a semiconductor layer 506 is formed (see FIG. 19B). In this embodiment, the oxide semiconductor layer described in the above embodiment is applied to the semiconductor layer 502. The above embodiment can be referred to for the details of the oxide semiconductor layer. The above embodiments can also be referred to for the other details.

[0123]

Next, a conductive layer 508 is formed so as to cover the semiconductor layer 506 (see FIG. 19C). After a resist mask 510 and a resist mask 512 are selectively formed over the conductive layer 508, the conductive layer 508 is selectively etched using the resist masks, so that a conductive layer 514 which functions as one of a source electrode and a drain electrode and a conductive layer 516 which functions as the other of the source electrode and the drain electrode are formed (see FIG. 19D). The above embodiments can be referred to for the details.

[0124]

Next, an insulating layer 518 serving as a gate insulating layer is formed so as to cover the semiconductor layer 506, the conductive layer 514, and the conductive layer 516 (see FIG. 20A). Then, a conductive layer 520 is formed over the insulating layer 518 (see FIG. 20B). After a resist mask 522 is selectively formed over the conductive layer 520, the conductive layer 520 is selectively etched using the resist mask 522, whereby a conductive layer 524 serving as a gate electrode is formed (see

FIG. 20C). The above embodiments can also be referred to for the details. Through the above steps, a transistor 550 using an oxide semiconductor layer is completed (see FIG. 20D).

[0125]

As described in this embodiment, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, the entry of impurities (e.g., moisture and the like) into the oxide semiconductor layer can be suppressed. Thus, the reliability of the semiconductor device can be increased.

[0126]

Further, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, a semiconductor device with favorable electric characteristics can be provided.

[0127]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0128]

(Embodiment 5)

In this embodiment, another example of a transistor as a semiconductor device and a manufacturing method thereof will be described with reference to FIGS. 21A to 21D and FIGS. 22A to 22D. Note that many parts of a method for manufacturing a semiconductor device in this embodiment are common to those in the above embodiments; therefore, description of the common parts is omitted below and only different parts will be described in detail.

[0129]

First, a conductive layer 602 is formed over a substrate 600 (see FIG. 21A). After a resist mask 604 and a resist mask 606 are selectively formed over the conductive layer 602, the conductive layer 602 is selectively etched using the resist masks, so that a conductive layer 608 which functions as one of a source electrode and a drain electrode and a conductive layer 610 which functions as the other of the source electrode and the drain electrode are formed (see FIG. 21B). The above embodiments can be referred to for the details.

[0130]

Next, a semiconductor layer 612 in contact with the conductive layer 608 and the conductive layer 610 is formed (see FIG. 21C). After a resist mask 614 is selectively formed over the semiconductor layer 612, the semiconductor layer 612 is selectively etched using the resist mask 614, so that a semiconductor layer 616 is formed (see FIG. 21D). In this embodiment, the oxide semiconductor layer described in the above embodiment is applied to the semiconductor layer 612. The above embodiment can be referred to for the details of the oxide semiconductor layer. The above embodiments can also be referred to for the other details.

[0131]

Next, an insulating layer 618 serving as a gate insulating layer is formed so as to cover the semiconductor layer 616, the conductive layer 608, and the conductive layer 610 (see FIG. 22A). Accordingly, a conductive layer 620 is formed over the insulating layer 618 (see FIG. 22B). After a resist mask 622 is selectively formed over the conductive layer 620, the conductive layer 620 is selectively etched using the resist mask 622, whereby a conductive layer 624 serving as a gate electrode is formed (see FIG. 22C). The above embodiments can be referred to for the details. Through the above steps, a transistor 650 using an oxide semiconductor layer is completed (see FIG. 22D).

[0132]

As described in this embodiment, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, the entry of impurities (e.g., moisture and the like) into the oxide semiconductor layer can be suppressed. Thus, the reliability of the semiconductor device can be increased.

[0133]

Further, by manufacturing a semiconductor device with the use of the oxide semiconductor layer described in the above embodiment, a semiconductor device with favorable electric characteristics can be provided.

[0134]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0135]

(Embodiment 6)

In this embodiment, a structure of a display device including an electrophoretic element will be described with reference to FIGS. 23A and 23B, as an example of using the semiconductor device described in any of the above embodiments. Note that in this embodiment, an example of a display device including an electrophoretic element will be described; however, a display device for which a semiconductor device according to one embodiment of the disclosed invention can be used is not limited thereto. The semiconductor device according to one embodiment of the disclosed invention can be applied to a display device including a variety of display elements such as a liquid crystal display element or an electroluminescent element.

[0136]

FIG. 23A illustrates a plan view of a pixel of a display device, and FIG. 23B illustrates a cross-sectional view along line A-B in FIG. 23A. The display device illustrated in FIGS. 23A and 23B includes a substrate 700, a transistor 702 and a capacitor 704 formed over the substrate 700, an electrophoretic element 706 formed over the transistor 702 and the capacitor 704, and a light-transmitting substrate 708 formed over the electrophoretic element 706. Note that the electrophoretic element 706 is not illustrated in FIG. 23A for simplicity.

[0137]

The transistor 702 includes a conductive layer 710, an insulating layer 712 which covers the conductive layer 710, a semiconductor layer 714 formed over the insulating layer 712, a conductive layer 716 and a conductive layer 718 which are in contact with the semiconductor layer 714. Here, the conductive layer 710 functions as a gate electrode of the transistor; the insulating layer 712 functions as a gate insulating layer of the transistor; the conductive layer 716 functions as a first terminal (one of a source terminal and a drain terminal) of the transistor; and the conductive layer 718 functions as a second terminal (the other of the source terminal and the drain terminal) of the transistor. The above embodiments can also be referred to for the details.

[0138]

Additionally, the conductive layer 710 is electrically connected to a gate line 720, and the conductive layer 716 is electrically connected to a source line 722 in the

above. The conductive layer 710 may be integrated with the gate line 720, and the conductive layer 716 may be integrated with the source line 722.

[0139]

The capacitor 704 includes the conductive layer 718, the insulating layer 712, and a conductive layer 724. The capacitor 704 has a function of holding a signal which is input to a pixel. The above components of the capacitor 704 can be formed together with components of the transistor.

[0140]

In the above, the conductive layer 724 is electrically connected to a capacitor wiring 726. The conductive layer 718 functions as one terminal of the capacitor. The insulating layer 712 functions as a dielectric. The conductive layer 724 functions as the other terminal of the capacitor. The conductive layer 724 may be integrated with the capacitor wiring 726.

[0141]

The electrophoretic element 706 includes a pixel electrode 728, a common electrode 730 (it may be called a counter electrode), and a layer 732 containing charged particles which is provided between the pixel electrode 728 and the common electrode 730. As the charged particles contained in the layer 732 containing charged particles, titanium oxide or the like can be used as positively-charged particles, and carbon black or the like can be used as negatively-charged particles. In addition, a single material selected from a conductor, an insulator, a semiconductor, a magnetic material, a liquid crystal material, a ferroelectric material, an electroluminescent material, an electrochromic material, and a magnetophoretic material, or a composite material formed using any of these materials can also be used.

[0142]

In the above, the pixel electrode 728 is electrically connected to the conductive layer 718 through an opening provided in an insulating layer 734 and an insulating layer 736 which cover the transistor 702 and the capacitor 704. The common electrode 730 is electrically connected to a common electrode of another pixel.

[0143]

The above structure makes it possible to control an electric field applied to the layer 732 containing charged particles, and to control the arrangement of the charged

particles in the layer 732 containing charged particles. Thus, display can be realized. The above structure is merely an example, and the display device using the semiconductor device according to one embodiment of the disclosed invention is not limited to the above structure.

[0144]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

[0145]

(Embodiment 7)

In this embodiment, applications of the display device illustrated in the above embodiment are described with reference to specific examples in FIGS. 24A to 24D.

[0146]

FIG. 24A shows a portable information terminal, which includes a housing 801, a display portion 802, operation buttons 803, and the like. The display device described in the above embodiment can be applied to the display portion 802.

[0147]

FIG. 24B is an example of an e-book reader on which the display device described in the above embodiment is mounted. A first housing 811 includes a first display portion 812 and operation buttons 813, and a second housing 814 includes a second display portion 815. The display device described in the above embodiment can be applied to the first display portion 812 or the second display portion 815. In addition, the first housing 811 and the second housing 814 can be opened and closed with a support portion 816. With such a structure, the e-book reader can be handled like a paper book.

[0148]

FIG. 24C illustrates a display device 820 for advertisement in a vehicle. In the case where an advertising medium is printed paper, the advertisement is replaced by hand; however, by using the display device, the advertising display can be changed in a short time with less manpower. In addition, an image can be stably displayed without display deterioration.

[0149]

FIG. 24D illustrates a display device 830 for outdoor advertisement. The display device is manufactured using a flexible substrate and can enhance the advertising effect by being waved.

[0150]

The methods, structures, and the like described in this embodiment can be combined as appropriate with any of the methods, structures, and the like described in the other embodiments.

This application is based on Japanese Patent Application serial no. 2009-234507 filed with the Japan Patent Office on October 8, 2009, the entire contents of which are hereby incorporated by reference.

EXPLANATION OF REFERENCE

100: oxide semiconductor layer; 110: base material; 120: amorphous region; 130: crystal grain; 140: crystal region; 200: oxide semiconductor layer; 300: substrate; 302: conductive layer; 304: resist mask; 306: conductive layer; 308: insulating layer; 310: semiconductor layer; 312: resist mask; 314: semiconductor layer; 316: conductive layer; 318: resist mask; 320: resist mask; 322: conductive layer; 324: conductive layer; 326: insulating layer; 350: transistor; 400: substrate; 402: conductive layer; 404: resist mask; 406: conductive layer; 408: insulating layer; 410: conductive layer; 412: resist mask; 414: resist mask; 416: conductive layer; 418: conductive layer; 420: semiconductor layer; 422: resist mask; 424: semiconductor layer; 426: insulating layer; 450: transistor; 500: substrate; 502: semiconductor layer; 504: resist mask; 506: semiconductor layer; 508: conductive layer; 510: resist mask; 512: resist mask; 514: conductive layer; 516: conductive layer; 518: insulating layer; 520: conductive layer; 522: resist mask; 524: conductive layer; 550: transistor; 600: substrate; 602: conductive layer; 604: resist mask; 606: resist mask; 608: conductive layer; 610: conductive layer; 612: semiconductor layer; 614: resist mask; 616: semiconductor layer; 618: insulating layer; 620: conductive layer; 622: resist mask; 624: conductive layer; 650: transistor; 700: substrate; 702: transistor; 704: capacitor; 706: electrophoretic element; 708: substrate; 710: conductive layer; 712: insulating layer; 714: semiconductor layer; 716: conductive layer; 718: conductive layer; 720: gate line; 722: source line; 724: conductive layer; 726: capacitor wiring; 728: pixel electrode; 730: common electrode; 732: layer containing charged particles; 734: insulating layer; 736: insulating layer; 801: housing; 802: display portion; 803: operation button; 811: housing; 812: display portion; 813: operation button; 814: housing; 815: display portion; 816: support portion; 820: display device; and 830: display device.

CLAIMS

1. A semiconductor device comprising:

a substrate;

a gate electrode layer over the substrate;

a gate insulating layer over the gate electrode layer;

an oxide semiconductor layer over the gate insulating layer; and

a source electrode layer and a drain electrode layer electrically connected to the oxide semiconductor layer,

wherein the oxide semiconductor layer includes an amorphous region and a crystal region,

wherein the amorphous region contains an amorphous oxide semiconductor containing In, Ga, and Zn,

wherein the crystal region contains crystal grains of $In_2Ga_2ZnO_7$ in a vicinity of a surface of the oxide semiconductor layer, and

wherein the crystal grains are oriented so that a c-axis is almost vertical with respect to the surface.

2. The semiconductor device according to claim 1, wherein the crystal grains of $In_2Ga_2ZnO_7$ has a stacked-layer structure of a first layer containing In, a second layer without In, a third layer without In, a fourth layer containing In, and a fifth layer without In.

3. The semiconductor device according to claim 2, wherein one of a 5s orbital of In is overlapped with an adjacent 5s orbital of In in the first layer containing In or the fourth layer containing In.

4. The semiconductor device according to claim 1, wherein a Zn content is less than an In content or a Ga content in the amorphous region.

5. The semiconductor device according to claim 1, wherein a length of the crystal grains in the c-axis direction is less than five times as long as a length of the crystal grains in an a-axis direction or a b-axis direction.

6. The semiconductor device according to claim 1, further comprising an insulating layer covering the oxide semiconductor layer.

7. The semiconductor device according to claim 1, wherein the source electrode layer or the drain electrode layer, and the oxide semiconductor layer are electrically connected to each other on an upper surface or a lower surface of the oxide semiconductor layer.

8. The semiconductor device according to claim 6, wherein the source electrode layer or the drain electrode layer, and the oxide semiconductor layer are electrically connected to each other on an upper surface or a lower surface of the oxide semiconductor layer.

9. A semiconductor device comprising:

a substrate;

an oxide semiconductor layer over the substrate;

a gate insulating layer over the oxide semiconductor layer;

a gate electrode layer over the gate insulating layer; and

a source electrode layer and a drain electrode layer electrically connected to the oxide semiconductor layer,

wherein the oxide semiconductor layer includes an amorphous region and a crystal region,

wherein the amorphous region contains an amorphous oxide semiconductor containing In, Ga, and Zn,

wherein the crystal region contains crystal grains of $In_2Ga_2ZnO_7$ in a vicinity of a surface of the oxide semiconductor layer, and

wherein the crystal grains are oriented so that a c-axis is almost vertical with respect to the surface.

10. The semiconductor device according to claim 9, wherein the crystal grains of $In_2Ga_2ZnO_7$ has a stacked-layer structure of a first layer containing In, a second layer without In, a third layer without In, a fourth layer containing In, and a fifth layer without In.

11. The semiconductor device according to claim 10, wherein one of a 5s orbital of In is overlapped with an adjacent 5s orbital of In in the first layer containing In or the fourth layer containing In.

12. The semiconductor device according to claim 9, wherein a Zn content is less than an In content or a Ga content in the amorphous region.

13. The semiconductor device according to claim 9, wherein a length of the crystal grains in the c-axis direction is less than five times as long as a length of the crystal grains in an a-axis direction or a b-axis direction.

14. The semiconductor device according to claim 9, further comprising an insulating layer covering the oxide semiconductor layer.

15. The semiconductor device according to claim 9, wherein the source electrode layer or the drain electrode layer, and the oxide semiconductor layer are electrically connected to each other on an upper surface or a lower surface of the oxide semiconductor layer.

16. The semiconductor device according to claim 14, wherein the source electrode layer or the drain electrode layer, and the oxide semiconductor layer are electrically connected to each other on an upper surface or a lower surface of the oxide semiconductor layer.

17. A semiconductor device comprising:

a substrate;

a gate electrode layer over the substrate;

a gate insulating layer adjacent to the gate electrode layer;

a first oxide semiconductor layer adjacent to the gate electrode layer with the gate insulating layer interposed therebetween; and

a source electrode layer and a drain electrode layer in contact with the first oxide semiconductor layer,

wherein the first oxide semiconductor layer includes an amorphous region and a crystal region,

wherein the amorphous region comprises an oxide semiconductor containing In, Ga, and Zn,

wherein the crystal region is formed in a vicinity of a surface of the first oxide semiconductor layer,

wherein the crystal region comprises crystal grains of an oxide semiconductor containing In, Ga, and Zn, and

wherein the crystal grains are oriented so that c-axes of the crystal grains are almost vertical with respect to the surface of the first oxide semiconductor layer.

18. The semiconductor device according to claim 17, wherein the crystal grains include a crystal structure of $In_2Ga_2ZnO_7$.

19. The semiconductor device according to claim 17, wherein the crystal grains include a crystal structure of $InGaZnO_4$.

20. The semiconductor device according to claim 17, wherein the crystal grains include a mix of crystal structures of $In_2Ga_2ZnO_7$ and $InGaZnO_4$.

21. The semiconductor device according to claim 17, wherein a Zn content is less than an In content or a Ga content in the amorphous region.

22. The semiconductor device according to claim 17, further comprising a second oxide semiconductor layer adjacent to the first oxide semiconductor layer,

wherein a composition ratio of In, Ga, and Zn in the first oxide semiconductor layer is different from a composition ratio of In, Ga, and Zn in the second oxide semiconductor layer.