WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, the method comprising:

forming an active pattern on a substrate such that the active pattern includes sacrificial patterns and semiconductor patterns alternately and repeatedly stacked on the substrate;

forming first spacer patterns at both sides of each of the sacrificial patterns by performing an oxidation process,

selectively removing the first spacer patterns to form recess regions that respectively expose both sidewalls of each of the sacrificial patterns, and

forming spacer patterns in the recess regions, respectively,

wherein the first spacer patterns correspond to oxidized portions of each of the sacrificial patterns,

wherein the sacrificial patterns include a first semiconductor material containing impurities,

wherein the semiconductor patterns include a second semiconductor material different from the first semiconductor material,

wherein the impurities include an element different from semiconductor elements of the first semiconductor material and the second semiconductor material, and

wherein each of the recess regions exposes one sidewall of each of the sacrificial patterns and a top or bottom surface of each of adjacent ones of the semiconductor patterns.

2. The method as claimed in claim 1, wherein the first spacer patterns include an oxide containing the impurities.

3. The method as claimed in claim 1, further comprising forming second spacer patterns at both sides of each of the semiconductor patterns by performing the oxidation process,

wherein the second spacer patterns correspond to oxidized portions of each of the semiconductor patterns, and

wherein the first spacer patterns include the impurities.

4. The method as claimed in claim 3, wherein:

each of the first spacer patterns has a thickness in a direction parallel to a top surface of the substrate, and

each of the second spacer patterns has a thickness in the direction parallel to the top surface of the substrate, and

the thicknesses of the first spacer patterns are greater than the thicknesses of the second spacer patterns.

5. The method as claimed in claim 4, further comprising:

selectively removing the second spacer patterns;

removing the sacrificial patterns to form empty regions such that each empty region is defined between first spacer patterns laterally spaced apart from each other; and

forming a gate electrode in the empty regions.

6. The method as claimed in claim 1, wherein forming the spacer patterns includes:

forming a spacer layer filling the recess regions on the substrate; and

anisotropically etching the spacer layer to locally form the spacer patterns in the recess regions, respectively.

7. The method as claimed in claim 6, further comprising:

removing the sacrificial patterns to form empty regions such that each empty region is defined between the spacer patterns laterally spaced apart from each other; and

forming a gate electrode in the empty regions.

8. The method as claimed in claim 1, wherein:

the active pattern includes first sidewalls opposite to each other in a first direction and second sidewalls opposite to each other in a second direction intersecting the first direction,

the method further comprises:

forming a sacrificial gate pattern on the substrate and covering the second sidewalls and a top surface of the active pattern; and

forming source/drain patterns on the first sidewalls of the active pattern at both sides of the sacrificial gate pattern, respectively, and

the oxidation process is performed after the forming of the sacrificial gate pattern and before the forming of the source/drain patterns.

9. The method as claimed in claim 1, wherein the impurities include aluminum (Al), gallium (Ga), antimony (Sb), arsenic (As), indium (In), zirconium (Zr), hafnium (Hf), or tantalum (Ta).

10. A method for manufacturing a semiconductor device, the method comprising:

forming a preliminary active pattern extending in a first direction on a substrate such that the preliminary active pattern includes preliminary sacrificial patterns and preliminary semiconductor patterns alternately and repeatedly stacked on the substrate;

forming a sacrificial gate pattern on the substrate such that the sacrificial gate pattern extends in a second direction intersecting the first direction to intersect the preliminary active pattern;

removing portions of the preliminary active pattern at both sides of the sacrificial gate pattern to form an active pattern under the sacrificial gate pattern such that the active pattern includes sacrificial patterns and semiconductor patterns alternately and repeatedly stacked; and

oxidizing both sidewalls of the active pattern to form first spacer patterns at both sides of each of the sacrificial patterns and second spacer patterns at both sides of each of the semiconductor patterns at the same time,

wherein the preliminary sacrificial patterns and the sacrificial patterns include a first semiconductor material containing impurities,

wherein the preliminary semiconductor patterns and the semiconductor patterns include a second semiconductor material different from the first semiconductor material, and

wherein the impurities include aluminum (Al), gallium (Ga), antimony (Sb), indium (In), zirconium (Zr), hafnium (Hf), or tantalum (Ta).

11. The method as claimed in claim 10, wherein:

the active pattern includes first sidewalls opposite to each other in the first direction and second sidewalls opposite to each other in the second direction,

the sacrificial gate pattern covers the second sidewalls and a top surface of the active pattern, and

the first spacer patterns and the second spacer patterns are formed by oxidizing the first sidewalls.

12. The method as claimed in claim 10, wherein:

the first spacer patterns correspond to oxidized portions of each of the sacrificial patterns,

the second spacer patterns correspond to oxidized portions of each of the semiconductor patterns, and

the first spacer patterns include the impurities.

13. The method as claimed in claim 12, wherein:

each of the first spacer patterns has a thickness in the first direction,

each of the second spacer patterns has a thickness in the first direction, and

the thicknesses of the first spacer patterns are greater than the thicknesses of the second spacer patterns.

14. The method as claimed in claim 10, wherein:

the first semiconductor material includes silicon (Si), silicon-germanium (SiGe), or germanium (Ge),

the second semiconductor material includes silicon (Si), silicon-germanium (SiGe), or germanium (Ge).

15. The method as claimed in claim 10, further comprising:

selectively removing the second spacer patterns; and

forming source/drain patterns at both sides of the sacrificial gate pattern after the selective removal of the second spacer patterns.

16. The method as claimed in claim 15, further comprising:

removing each sacrificial pattern between the first spacer patterns and the sacrificial gate pattern to form an empty region; and

forming a gate electrode in the empty region.

17. The method as claimed in claim 10, further comprising:

removing the first and second spacer patterns;

forming spacer patterns at both sides of each of the sacrificial patterns; and

forming source/drain patterns at both sides of the sacrificial gate pattern after the forming of the spacer patterns.

18. The method as claimed in claim 17, wherein the spacer patterns include silicon nitride.

19. The method as claimed in claim 17, further comprising:

removing each sacrificial pattern between the spacer patterns and the sacrificial gate pattern to form an empty region; and

forming a gate electrode in the empty region.