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ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

TECHNICAL FIELD

The present invention relates to processes for selectively etching doped silicon dioxide that overlies silicon nitride or undoped silicon dioxide. Particularly, the process of the present invention includes an etchant mixture which includes the use of an ethane gas having the general formula $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y equals six. The present invention also relates to etchant mixtures which include a component having the general formula $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y equals six.

BACKGROUND ART

The fabrication of multi-layered structures upon semiconductor devices typically involves the patterning of doped silicon dioxide layers, including, without limitation, layers of phosphosilicate glass (PSG), borosilicate glass (BSG) and borophosphosilicate glass (BPSG). Such materials are typically employed as passivation layers on semiconductor devices. Etching techniques are typically employed to pattern many types of semiconductor device structures, including the formation of contact openings through passivation layers. Etch stop layers are typically formed on underlying structures, such as over a conductively doped contact region formed in a semiconductor substrate, in order to terminate the etch process once the desired patterning of the passivation layer, or etch substrate, has occurred. Silicon nitride (Si_3N_4) is typically utilized as an etch stop during the patterning of silicon dioxide.

Conventionally, prior to etching, protective layers, such as photoresists, are deposited and developed to act as templates, or protective masks, in order to define structures from a passivation layer, such as a doped silicon dioxide layer, by etching techniques. Wet etch or dry etch techniques may be employed through such protective

masks to define semiconductor device structures from doped silicon dioxide passivation layers.

An exemplary wet etch process is disclosed in United States Patent 5,300,463 ("the '463 patent"), issued to David A. Cathey et al. The wet etch process of the '463 patent, which employs hydrofluoric acid (HF) as an etchant, is selective for doped silicon dioxide over undoped silicon dioxide. Despite the selectivity, or specificity, of that technique, it is somewhat undesirable from the standpoint that it suffers from many of the shortcomings that are typically associated with wet etch processes. Specifically, the technique of the '463 patent is an isotropic etch. Consequently, the structures defined thereby may have different dimensions than those of the target area of the etch substrate that is exposed through the protective mask. Moreover, as those of skill in the art are aware, since wet etch techniques are typically isotropic, if the thickness of the film being etched is approximately equivalent to the minimum desired pattern dimension, the undercutting that is typically caused by isotropic etching becomes intolerable. Similarly, with the ever-decreasing size of structures that are carried on the active surfaces of semiconductor devices, etching must be very accurate and maintained within very precise tolerances in order to preserve the alignment of such minute structures and to optimize the electrical characteristics of such structures. Such precision often cannot be obtained when many conventional wet etch processes are used to define structures on semiconductor devices. Thus, the lack of precision and isotropic nature of typical wet etching processes are inconsistent with the overall goal of etch processes in forming structures on state-of-the-art semiconductor devices: reproducing the features defined by the protective mask with a high degree of fidelity.

In contrast, many dry etch techniques, including, without limitation, glow-discharge sputtering, ion milling, reactive ion etching (RIE), reactive ion beam etching (RIBE), and high-density plasma etching, are capable of etching in a substantially anisotropic fashion, meaning that the target area of an etch substrate is etched primarily in a substantially vertical direction relative to the exposed, or active, surface of the etched substrate. Thus, such dry etch techniques are capable of defining structures with substantially upright sidewalls from the etch substrate. Consequently, such dry etch techniques are capable of accurately reproducing the features of a protective mask. Due

to ever-decreasing dimensions of structures on semiconductor devices, dry etching is often desirable for defining structures upon semiconductor device active surfaces.

Many techniques that employ plasmas to dry etch silicon dioxide layers, however, lack the specificity of comparable wet etch techniques. Fluorocarbons, such as CF_4 and CHF_3, are typically employed in plasma dry etches of silicon dioxide layers. The radio-frequency (RF) plasmas that are typically utilized with these fluorocarbons generate activated species, such as fluoride ions and fluorine free radicals, which attack silicon dioxide to etch same. These activated fluorine radicals and fluoride ions may also attack other materials, such as silicon and silicon nitride. Consequently, in addition to etching the desired layer, many dry etch techniques that employ plasmas also undesirably etch the etch stop layers and other structures of the semiconductor device that are exposed or which become exposed during the etching process.

Etch stop materials employed in dry etch techniques typically underlie an associated etch substrate and are etched at a lower rate than the associated etch substrate. Since the dry etchant etches the etch stop layer at a slower rate than the outer etch substrate, the etch stop layer acts to protect structures therebeneath from the dry etch process, even as the etch stop itself is being consumed.

Since the gate structures of many semiconductor devices include a silicon nitride (Si_3N_4) cap, selectivity between silicon dioxide (SiO_2) and silicon nitride is desirable in order to etch contacts through passivation layers. Many of the so-called silicon dioxide-selective plasma dry etch techniques, however, have a SiO_2 to Si_3N_4 selectivity ratio, or etch rate of SiO_2 to etch rate of Si_3N_4, of less than about 3:1.

United States Patent 5,286,344 ("the '344 Patent"), issued to Guy Blalock et al. on February 15, 1994, discloses a dry etch process which has much better selectivity for silicon dioxide over silicon nitride than many other conventional silicon dioxide dry etch techniques. Specifically, CH_2F_2, which is employed as an additive to a primary etchant such as CF_4 or CHF_3, imparts the dry etchant mixture with improved selectivity for silicon dioxide over silicon nitride. The high energy ions that are required to etch both silicon dioxide and silicon nitride act by dissociating a chemical bond at the respective oxide or nitride surface. The dissociation energy that is required to etch silicon nitride is, however, less than that required to etch silicon dioxide. The use of CH_2F_2 in the dry etchant causes polymer deposition on the silicon nitride surface that offsets the

dissociation properties of silicon nitride relative to the dissociation properties of silicon dioxide to a greater extent than conventional dry etchants that lack additives such as CH_2F_2. As a result, the etchant of the '344 Patent etches silicon dioxide over an etch stop of silicon nitride with a selectivity of greater than 30:1. As with other conventional silicon dioxide dry etch techniques, however, the only material that is disclosed as a useful etch stop in the '344 Patent is silicon nitride. Thus, the utility of the dry etch process that is disclosed in the '344 Patent is limited to defining semiconductor device structures which include a silicon nitride dielectric layer, such as contacts over silicon nitride-capped gates. Moreover, the relative flow rates of each of the dry etchant components disclosed in the '344 Patent are limited to narrow ranges in order to achieve the desired level of selectivity. Similarly, many other conventional dry etch processes require the use of very specific dry etchant components. Thus, the process windows of many conventional dry etch systems are narrow.

Although silicon nitride is widely employed as an etch stop material, the use of silicon nitride etch stops is somewhat undesirable from the standpoint that the deposition of silicon nitride upon a semiconductor device active surface by low pressure chemical vapor deposition (LPCVD) processes may also form a thick nitride layer on the back surface of the semiconductor device. Such thick nitride layers must be subsequently removed, which increases fabrication time and costs, as well as the potential for damaging the semiconductor device during the fabrication thereof.

Moreover, the fluorine radicals and fluoride ions generated during conventional dry etch processes that employ plasmas non-selectively attack, or etch, both doped and undoped silicon dioxide. Stated another way, such silicon dioxide dry etch techniques are incapable of distinguishing between doped and undoped silicon dioxide. Consequently, when conventional dry etch techniques are employed, the use of alternatives to silicon nitride in state-of-the-art semiconductor devices is restricted.

Accordingly, the inventors have recognized a need for etchants that are specific for silicon dioxide over both undoped silicon dioxide and silicon nitride, as well as a need for a selective doped silicon dioxide dry etch process for which both silicon nitride and undoped silicon dioxide act as etch stops, or for which the use of an etch stop is unnecessary. Etchant mixtures are also needed wherein relative concentrations of each

of the components of such etchant mixtures may be varied in order to facilitate the use of such mixtures in a broad range of doped silicon dioxide etching applications.

DISCLOSURE OF INVENTION

The present invention includes a dry etch process and etchants that address the foregoing needs and overcome the disadvantages manifested by conventional dry etch processes.

The etchants of the present invention include $C_2H_xF_y$, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y equals six. Specifically, the $C_2H_xF_y$ component of the present invention may be selected from the group consisting of $C_2H_2F_4$, $C_2H_3F_3$, $C_2H_4F_2$, and C_2H_5F. The $C_2H_xF_y$ component may be used as either a primary etchant or as a component of an etchant mixture. When employed as a primary etchant, $C_2H_xF_y$ etches doped silicon dioxide at a slow rate relative to the etch rates of many conventional silicon dioxide dry etch techniques, but selectively etches doped silicon dioxide over undoped silicon dioxide.

When used as an additive to other silicon dioxide etchants, $C_2H_xF_y$ imparts the etchant mixture with selectivity for doped silicon dioxide over undoped silicon dioxide, while permitting the doped silicon dioxide etch to proceed at a comparable rate relative to many conventional doped silicon dioxide dry etch techniques. The amount of $C_2H_xF_y$ used in the etchant mixture may be varied, depending upon the particular species of $C_2H_xF_y$ used, the desired level of doped to undoped silicon dioxide selectivity (i.e., selectivity ratio), the desired level of silicon dioxide to silicon nitride selectivity, the desired etch rate, and other factors.

The dry etch process of the present invention employs an etchant of the present invention (i.e., an etchant which includes $C_2H_xF_y$), and is selective for doped silicon dioxide over both undoped silicon dioxide and silicon nitride. Thus, the dry etch process of the present invention may be effectively employed for anisotropically etching a doped silicon dioxide layer down to an underlying etch stop of either undoped silicon dioxide or silicon nitride.

Structures fabricated by use of the inventive etchant in the dry etch process of the present invention are also within the scope of the present invention.

Other features and advantages of the present invention will become apparent to those of ordinary skill in the relevant art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1 through 4 are cross-sectional schematic representations that illustrate an embodiment of the process of the present invention and an exemplary structure that may be formed thereby; and

FIGs. 5 through 8 are cross-sectional schematic representations that illustrate use of the process of the present invention on another semiconductor device structure and an example of the resulting structure.

BEST MODE OR MODES FOR CARRYING OUT THE INVENTION

The present invention includes an etchant that is selective for doped silicon dioxide over both undoped silicon dioxide and silicon nitride. As those of skill in the art are aware, "doped" silicon dioxide typically includes a dopant such as boron or phosphorus, whereas undoped silicon dioxide is substantially free of dopants and other impurities. Exemplary types of doped silicon dioxide include, without limitation, borosilicate glass (BSG), phosphosilicate glass (PSG), and borophosphosilicate glass (BPSG). The present invention also includes a dry etch process which utilizes the inventive etchant.

The doped silicon dioxide etchant of the present invention, which is also referred to herein as an etchant for simplicity, includes an ethane component of the general formula $C_2H_xF_y$, which is also referred to as the $C_2H_xF_y$ component or $C_2H_xF_y$ for simplicity, where x is an integer from two to five, inclusive, y is an integer from one to four, inclusive, and x plus y equals six. Specifically, the $C_2H_xF_y$ component of the present invention is desirably selected from the group consisting of $C_2H_2F_4$, $C_2H_3F_3$, $C_2H_4F_2$, and C_2H_5F. The doped silicon dioxide etchant may also include combinations of various types of $C_2H_xF_y$.

As the $C_2H_xF_y$ component of a doped silicon dioxide etchant is RF activated, the hydrogen ions and activated hydrogen species react with the fluorine-containing ions and activated fluorine-containing species (e.g., F* and CF*), removing the activated

fluorine-containing species from the surface of the wafer prior to the occurrence of any substantial amount of etching of an etch stop layer of either undoped silicon dioxide or silicon nitride. The hydrogen content of the $C_2H_xF_y$ additives imparts etchants including the same with specificity for doped silicon dioxide over undoped silicon dioxide.

In a first embodiment of the doped silicon dioxide etchant of the present invention, $C_2H_xF_y$ is a primary etchant. When used as the primary etchant, $C_2H_xF_y$ is selective for doped silicon dioxide over undoped silicon dioxide. Stated another way, $C_2H_xF_y$ etches doped silicon dioxide at a higher rate than it etches undoped silicon dioxide. As the primary etchant, $C_2H_xF_y$ etches doped silicon dioxide at a relatively slow rate compared to the etch rates of many conventional silicon dioxide dry etchants. Thus, additives which will increase the etch rate may be used in combination with $C_2H_xF_y$. Such additives include, but are not limited to, CF_4, CHF_3, and other halogenated carbon materials which have been used as primary etchants in conventional doped silicon dioxide dry etch techniques.

Similarly, additives that increase an etchant's selectivity for silicon dioxide over silicon nitride (i.e., reduce the rate at which silicon nitride is etched) may also be used as additives to etchants which include $C_2H_xF_y$ as the primary etchant. The '334 Patent disclosure of which is hereby incorporated in its entirety by this reference, discloses some exemplary additives that may enhance the selectivity of $C_2H_xF_y$ in this manner. The additives of the '344 Patent are fluorocarbons in which the number of hydrogen atoms is equal to or greater than the number of fluorine atoms, such as CH_2F_2 and CH_3F.

Other additives may also be used with silicon dioxide etchants that include $C_2H_xF_y$ as the primary etchant in order to alter other characteristics of such etchants, including, without limitation, the selectivity of such etchants for doped silicon dioxide over undoped silicon dioxide and the selectivity for certain types of doped silicon dioxide over other types of doped silicon dioxide.

In another embodiment of the doped silicon dioxide etchant of the present invention, $C_2H_xF_y$ is employed as an additive to one or more primary etchants. $C_2H_xF_y$ may be used as an additive to etchants which include a fluorocarbon primary etchant, such as CF_4, CHF_3, or other fluorocarbons that etch silicon dioxide at a higher rate than they etch silicon nitride (i.e., are selective for silicon dioxide over silicon nitride).

According to the '344 Patent, CF_4 and CHF_3 are exemplary primary etchants with which $C_2H_xF_y$ may be utilized as an additive.

When used as an additive to a silicon dioxide etchant, such as CF_4 or CHF_3, $C_2H_xF_y$ imparts the silicon dioxide etchant with selectivity for doped silicon dioxide over undoped silicon dioxide while permitting the doped silicon dioxide etch to proceed at a substantially normal rate. The amount of $C_2H_xF_y$ that is used in an etchant mixture, relative to the amounts of other etchants and any carrier gas, may be varied in order to tailor the characteristics of the etchant mixture and to achieve the desired etching results. The various characteristics of the etchant mixture that may be varied by altering the concentration of $C_2H_xF_y$ in the mixture include, but are not limited to, selectivity for doped silicon dioxide over undoped silicon dioxide, selectivity for silicon dioxide over silicon nitride, and the doped silicon dioxide etch rate.

An exemplary dry etchant that is selective for doped silicon dioxide over both undoped silicon dioxide and silicon nitride includes about 40% of the additive $C_2H_2F_4$ (i.e., the $C_2H_xF_y$ component), about 30% of the primary etchant CHF_3, and about 30% of CH_2F_2, an additive which improves the selectivity of the primary etchants for silicon dioxide over silicon nitride, each of the percentages based on the relative flow rates of each gas into the etcher.

Alternatively, the amounts of the $C_2H_xF_y$ component may be varied considerably. Etchants that include any amount of an additive of the general formula $C_2H_xF_y$, where x is an integer from two to five, inclusive, where y is an integer from one to four, inclusive, and where x plus y equals six, are within the scope of the present invention. Exemplary etchants may include five percent, ten percent, twenty percent, sixty-five percent, or ninety percent of the $C_2H_xF_y$ additive or any combination of $C_2H_xF_y$ additives.

Similarly, it is also foreseen that $C_2H_xF_y$ may be employed as an additive to silicon dioxide dry etchant mixtures that include other components. For example, $C_2H_xF_y$ could be used along with an etchant that includes either CF_4 or CHF_3, or both of them as primary etchants and a carrier gas, such as argon or nitrogen. Alternatively, the $C_2H_xF_y$-containing dry etchant may include one or more other additives that alter the various characteristics of the dry etchant, such as the etch rate, the degree of selectivity, and the type of selectivity. For example, as disclosed in the '344 Patent, the use of

CH_2F_2 as an additive enhances the selectivity of the dry etchant for silicon dioxide over silicon nitride. Combinations of the additives of the general formula $C_2H_xF_y$ may also be employed as components in a doped silicon dioxide dry etchant.

A preferred embodiment of the dry etch process of the present invention employs an etchant of the present invention (i.e., an etchant which includes $C_2H_xF_y$), and is *selective for doped silicon dioxide over both undoped silicon dioxide and silicon nitride.* The dry etch process includes using the etchant to etch a doped silicon dioxide layer down to a structure or layer of either undoped silicon dioxide or silicon nitride, which structure or layer may form or be part of an etch stop.

Referring to FIGs. 1 to 4, the etch process of the present invention, which utilizes the inventive etchant, is illustrated. FIG. 1 depicts an exemplary multi-layer structure 10, which is also referred to as a semiconductor device structure, that may be fabricated, at least in part, in accordance with the process of the present invention. Multi-layer structure 10 includes a semiconductor substrate 12 (e.g., a silicon wafer, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), silicon-on-glass (SOG), etc.), a field oxide layer 14 disposed on an active surface 13 of the semiconductor substrate and an active device region 16. A diffusion region 17, which is also referred to herein as a contact, that includes conductively doped semiconductor material (e.g., silicon) is formed in active device region 16 and is continuous with active surface 13. Conductive lines 18, which are formed from a conductive material such as metal or polysilicon, are disposed on active surface 13 in active device region 16, electrically separated from active surface 13 by way of gate oxides 19, and are positioned laterally adjacent diffusion region 17. Sidewall spacers 20, which are positioned on each side of the conductive lines 18, and intermediate structural layer or insulative caps 22 disposed over conductive lines 18, electrically insulate conductive lines 18. Sidewall spacers 20 and caps 22 may be fabricated from silicon nitride or undoped silicon dioxide. Multi-layer structure 10 also includes a passivation layer 24 disposed over each of the foregoing elements. Passivation layer 24 is fabricated from doped silicon dioxide (e.g., BPSG, PSG or BSG).

FIG. 2 depicts masking of multi-layer structure 10 prior to defining a structure through passivation layer 24. A mask 26, which is also referred to as a protective layer, is layered and patterned over passivation layer 24. Mask 26 may be formed from a

material such as a photoresist or other photoimageable material. Exemplary positive photoresists that are useful as mask 26 may include a novolac resin, a diazonaphthaquinone, and a solvent, such as n-butyl acetate or xylene. Exemplary negative photoresists that are useful as mask 26 may include a cyclized synthetic rubber resin, bis-arylazide, and an aromatic solvent. Such a mask 26 may be applied to, or coated onto, multi-layer structure 10 and patterned by techniques that are known to those in the art, such as spin coating and photomask processing and patterning techniques. Alternatively, mask 26 may comprise an aerosol spray pattern of electrostatically chargeable hardenable liquid material, such as a polymer, which is not etched or is etched at a much slower rate than the underlying passivation layer 24. An exemplary method for spray-patterning such electrostatically chargeable hardenable liquid materials is described in United States Patent 5,695,658 (the "'658 Patent"), which issued to James J. Alwan on December 9, 1997, the disclosure of which is hereby incorporated in its entirety by this reference. Both photoresist materials (positive and negative) and non-photoimageable materials may be employed as mask 26 in accordance with the '658 Patent. The utilization of masks 26 that comprise other non-photoimageable materials and the processes for applying and patterning them are also within the scope of the method of the present invention. The patterning of mask 26 defines openings 28, which are also referred to as apertures or contact apertures, therethrough, through which predetermined structures will be defined in the underlying passivation layer 24 during a subsequent etch step. Mask 26 comprises a material that is resistant to the etchant of the present invention (i.e., the etchant does not etch mask 26 or etches the mask at a relatively slow rate compared to the rate at which the etch substrate is etched). Thus, the areas of passivation layer 24 that underlie mask 26 are protected from the etchant during the subsequent etch step.

Turning now to FIG. 3, an etch is depicted, wherein an activated etchant 30, which is introduced into an etch chamber (not shown) either with or without a carrier gas, attacks the areas of passivation layer 24 that are exposed through openings 28 of mask 26. Dry etch processes that are known to those of skill in the art, including, without limitation, high-density plasma etching, reactive ion etching (RIE), magnetic ion etching (MIE), magnetically enhanced reactive ion etching (MERIE), plasma etching (PE), point plasma etching, plasma enhanced reactive ion etching (PERIE), and electron

cyclotron resonance (ECR), may be employed with the etchant of the present invention and are within the scope of the process of the present invention. When activated, etchant 30, which comprises a $C_2H_xF_y$-containing etchant of the present invention, etches a contact opening 32, or an aperture, through passivation layer 24 in a substantially vertical fashion until intermediate structural layer 22 is exposed. Intermediate structural layer 22, which is fabricated from either undoped silicon dioxide or silicon nitride, acts as an etch stop layer. Thus, etchant 30 etches intermediate structural layer 22 at a slower rate than the rate at which passivation layer 24 is etched. After the exposed areas of passivation layer 24 have been etched, mask 26 may be removed by processes that are known in the art, such as washing or etching (wet or dry) techniques.

FIG. 4 illustrates a contact opening 32 or aperture that has been formed through passivation layer 24 by the etch process of the present invention. Contact opening 32 includes sidewalls 34 that are substantially vertical relative to active surface 13 of semiconductor substrate 12 or oriented substantially perpendicular relative to a plane of semiconductor substrate 12. Contact openings 32 of the multi-layer structure 10 expose at least a portion of the intermediate structural layer 22 that lies above each of conductive lines 18. Intermediate structural layer 22 defines a cap 36 over each conductive line 18. Thus, cap 36 may be fabricated from either undoped silicon dioxide or silicon nitride.

Intermediate structural layer 22 may then be removed from above diffusion region 17 to expose same by known processes, such as by masking multi-layer structure 10 and patterning intermediate structural layer 22 with wet or dry etchants, which preferably etch the material of intermediate structural layer 22 with selectivity over the material of diffusion region 17. Further processing of multi-layer structure 10 may then be conducted as known in the art (e.g., to form a conductive structure in contact with diffusion region 17).

Another example of the use of the etchant and process of the present invention is illustrated in FIGs. 5 to 8. FIG. 5 illustrates another exemplary multi-layer structure 10′ with which the process of the present invention may be employed. Multi-layer structure 10′, which is also referred to herein as a semiconductor device structure, includes a semiconductor substrate 12′, a field oxide layer 14′ formed on an active surface 13′ of semiconductor substrate 12′, and an active device region 16′ adjacent

field oxide layer 14′. A conductively doped diffusion region 17′, which is also referred to herein as a contact, is formed in active device region 16′ of semiconductor substrate 12′ adjacent active surface 13′. Conductive lines 18′, which may be formed from polysilicon or other electrically conductive materials, as known in the art, overly active device region 16′ on active surface 13′, are separated therefrom by way of gate oxide 19′, and are positioned laterally adjacent diffusion region 17′. Conductive lines 18′ are insulated by sidewall spacers 20′ positioned adjacent each side thereof, as well as a cap 22′ covering the top of each conductive line 18′. Sidewall spacers 20′ and caps 22′ may be fabricated from silicon nitride or undoped silicon dioxide. Multi-layer structure 10′ also includes a passivation layer 24′, formed from doped silicon dioxide (e.g., BPSG, PSG, or BSG), over diffusion region 17′, conductive lines 18′, sidewall spacers 20′, and caps 22′.

In FIG. 6, multi-layer structure 10′ is depicted as including a mask 26′, or protective layer, formed over passivation layer 24′. Mask 26′ may be formed by the same processes disclosed above with reference to the fabrication of mask 26 depicted in FIG. 2. Mask 26′ includes openings 28′, which are also referred to as apertures or contact apertures, formed therethrough, through which predetermined structures will be defined in the underlying passivation layer 24′ during a subsequent etch step. Mask 26′ comprises a material that is resistant to the etchant of the present invention (i.e., the etchant does not etch mask 26′ or etches mask 26′ at a relatively slow rate compared to the rate at which passivation layer 24′ is etched). The areas of passivation layer 24′ that underlie mask 26′ are protected from the etchant during the subsequent etch step.

The removal of material of passivation layer 24′ through mask 26′ is depicted in FIG. 7. An etchant 30, which is introduced into an etch chamber (not shown) either with or without a carrier gas, attacks the areas of passivation layer 24′ that are exposed through openings 28′ of mask 26′. Known dry etch processes, such as those listed previously herein with reference to the use of etchant 30 as depicted in FIG. 3, may be used with the inventive etchant in the process of the present invention. Etchant 30, which comprises a $C_2H_xF_y$-containing etchant of the present invention, etches an aperture 32′ through passivation layer 24′ in a substantially vertical fashion until diffusion region 17′ is exposed, as shown in FIG. 8. As passivation layer 24′ is etched through aperture 28′ down to diffusion region 17′, sidewall spacers 20′, which are

formed of silicon dioxide or silicon nitride, are exposed within contact aperture 32′ without being substantially etched, or are etched at a slower rate than the rate at which passivation layer 24′ is etched. After the exposed areas of passivation layer 24′ have been etched, mask 26′ may be removed by processes that are known in the art, such as washing or etching techniques. Etchant 30 also preferably etches doped silicon dioxide with selectivity over conductively doped silicon or another material of diffusion region 17′.

Further processing of multi-layer structure 10′ may then be conducted as known in the art (e.g., to form a conductive structure in contact with diffusion region 17′).

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. The scope of this invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions and modifications to the invention as disclosed herein which fall within the meaning and scope of the claims are to be embraced within their scope.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate including an active surface;

at least one undoped silicon oxide structure over said semiconductor substrate; and

at least one doped silicon oxide structure positioned at least partially over said at least one undoped silicon oxide structure and including at least one sidewall oriented substantially perpendicular to a plane of said substrate, said at least one sidewall terminating at said at least one undoped silicon dioxide structure, said active surface being at least partially exposed laterally adjacent said at least one sidewall.

2. The semiconductor device of claim 1, wherein said at least one sidewall comprises a sidewall of an aperture.

3. The semiconductor device of claim 1, wherein said at least one sidewall at least partially defines an aperture through said at least one doped silicon oxide structure.

4. The semiconductor device of claim 1, wherein said at least one doped silicon oxide structure comprises borophosphosilicate glass, phosphosilicate glass, or borosilicate glass.

5. The semiconductor device of claim 1, wherein said at least one undoped silicon oxide structure comprises an insulative cap over a conductive line.

6. The semiconductor device of claim 5, wherein said at least one undoped silicon oxide structure comprises a sidewall spacer adjacent said conductive line.

7. The semiconductor device of claim 6, wherein at least a portion of said sidewall spacer is exposed through an aperture of said at least one doped silicon oxide structure defined by said at least one sidewall.

8. A method for patterning doped silicon dioxide, comprising:

disposing a mask material over the doped silicon dioxide;

patterning said mask material to expose selected regions of the doped silicon dioxide; and

dry etching said exposed selected regions with an etchant comprising $C_2H_xF_y$, where x is an integer from two to five, inclusive, where y is an integer from one to four, inclusive, and where x plus y equals six, and said etchant is selective for the doped silicon dioxide over undoped silicon dioxide and silicon nitride.

9. The method of claim 8, wherein said disposing said mask material comprises disposing a photoimageable material.

10. The method of claim 9, wherein said patterning comprises photolithography.

11. The method of claim 8, wherein said disposing said mask material comprises disposing a non-photoimageable material.

12. The method of claim 8, further comprising providing an etch stop under the doped silicon dioxide and etching said exposed selected regions down to said etch stop.

13. The method of claim 12, wherein said providing said etch stop comprises providing an etch stop comprising undoped silicon dioxide.

14. The method of claim 12, wherein said providing said etch stop comprises providing an etch stop comprising silicon nitride.

15. The method of claim 8, wherein said dry etching is effected using a technique selected from the group comprising reactive ion etching, plasma etching, high-density plasma etching, point plasma etching, magnetic ion etching, magnetically

enhanced reactive ion etching, plasma enhanced reactive ion etching, and electron cyclotron resonance.

16. The method of claim 8, wherein said dry etching comprises reactive ion etching.

17. The method of claim 8, wherein said dry etching comprises high plasma etching.

18. A process for selectively etching a doped silicon dioxide structure, comprising:

exposing the doped silicon dioxide structure and at least a portion of an adjacent undoped silicon dioxide structure to an etchant comprising $C_2H_xF_y$, where x is an integer from three to five, inclusive, y is an integer from one to three, inclusive, and x plus y equals six; and

etching the doped silicon dioxide layer with said etchant without substantially etching said adjacent undoped silicon dioxide structure.

19. A dry etchant for etching doped silicon dioxide with selectivity over undoped silicon dioxide and silicon nitride, comprising:

a component having the general formula $C_2H_xF_y$;

where x is an integer from three to five, inclusive;

where y is an integer from one to three, inclusive; and

where x + y equals six.