

Description

The present invention relates to a vertical synchronizing pulse generating circuit for use in a television receiver, and more particularly, to a vertical synchronizing pulse generating circuit which is suited to be formed in an IC (integrated circuit).

Generally, in a television receiver, a signal having a frequency $n f_H$, which is equal to an integer number times the frequency of the horizontal frequency f_H , is formed in synchronization with the horizontal synchronizing signal. The signal with the frequency $n f_H$ is divided in accordance with the vertical synchronizing signal to obtain a signal having a vertical frequency f_v , which is used in a vertical deflection circuit for effecting the vertical deflection. An example of such a circuit formed in an IC is an IC element LA7620 for use in a deflection circuit for an image and color, and is explained, for examples, in "85 Sanyo Semi-Conductor Handbook Monosilic Bipolar Integrated Circuit" (issued on March 20, 1985, at page 1,000).

Fig. 1 shows a vertical deflection circuit which is a part of the IC. In Fig. 1, a numeral 1 shows an IC part, wherein a video signal from an image detecting circuit is applied to a composite synchronizing separation circuit 3 through an input pin 2, whereby a composite synchronizing signal consisting of a horizontal and a vertical synchronizing signals, etc. are separated. Since the composite synchronizing signal is applied to a vertical synchronizing separation circuit 7 comprising an integration circuit 4, a clamping circuit 5, and a transistor 6, the collector of the transistor 6 can obtain a pulse signal synchronizing a vertical synchronizing signal, and the pulse signal is impressed, as a reset signal, on a frequency divider 8.

In the meantime, a signal-generating circuit 9, which is impressed by a composite synchronizing signal obtained from the composite synchronizing separation circuit 3, generates a signal with a frequency $2f_H$ which is 2 times as many as a horizontal frequency synchronizing a horizontal synchronizing signal. The generated signal is then impressed on the frequency divider 8 as a clock signal. Thus, the signal with a frequency $2f_H$ is divided in the frequency divider 8 into $1/525$ according to pulses from the vertical synchronizing separation circuit 7. An output signal with a vertical frequency f_v which is obtained from the frequency divider 8 is applied to the base of an output transistor 10. As a result, an output pin 11 will produce driving pulses for driving a vertical deflection circuit 12.

Therefore, according to the circuit as shown in Fig. 1, a driving pulse for a vertical deflection can be obtained from a video signal.

However, in the circuit shown in Fig. 1, to obtain a vertical synchronizing signal, a capacitor is charged directly according to a composite synchronizing signal which has comparatively large level for a signal to be used in an IC. Therefore, the capacitor can not be incorporated in the IC, but is connected outside the IC chip. Accordingly, the integration circuit 4 and the clamping circuit 5 are connected outside the IC chip, resulting in the increase of parts and producing processes thereof. Also, a further problem arises that the number of pins increases, resulting in difficulty in arranging the circuit in an IC chip.

A vertical synchronizing pulse generator as mentioned above and as defined in a preamble of claim 1 is disclosed in IEEE TRANSACTIONS ON CONSUMER ELECTRONIC, vol. CE-29, no. 3, August 1983, pp. 287-296, IEEE, New York, US; I. NISHIMURA et al.: "A new self-alignment system for television receivers in LSI ERA".

To avoid the above mentioned problems of this prior art generator US-A-4 313 137 proposes an integratable vertical sync separator in which a load circuit is connected outside the IC and provides a feedback signal for controlling the charging and discharging currents of the capacitor. Therefore, the capacitor is capable of being incorporated in an integrated circuit, and the number of pins of this integrated circuit therefore decreases.

However, when the vertical synchronizing separation circuit has a low detecting sensitivity, there is such a problem that the vertical synchronizing signal cannot be detected when receiving a signal of weak electric field or when the wave form of the synchronizing signal is deformed. Especially, in mountainous countries where reception of the television signal is poor, such a problem occurs constantly.

It is therefore an object of the invention to provide a vertical synchronizing pulse generator which can detect vertical synchronizing signals even in case the received signal has low level amplitude or the wave form of the synchronizing signal is deformed.

This object is achieved by a vertical synchronizing pulse generator as defined in claim 1; the dependent claims are related to further developments of the invention.

According to the present invention, the load of the output transistor is regulated, thereby controlling an electric current flowing into the output transistor so as to permit an electric current resulting from the above described control to flow into the constant current generator. Therefore, a capacitor can be charged or discharged with a small amount of stable current. Accordingly, the capacitor can be incorporated in an IC chip, resulting in the decrease of outer circuit components and pins for the

external connection.

The preferred embodiments according to the present invention will be described as follows.

Fig. 1 shows a circuit diagram of a conventional vertical synchronizing separation circuit;

Fig. 2 shows a circuit diagram of a conventional integrated vertical synchronizing separation circuit;

Fig. 3 illustrates the waveforms observed at major points in the circuit of Fig. 2;

Fig. 4 shows a circuit diagram according to a first embodiment of a vertical synchronizing separation circuit of the present invention;

Fig. 5 shows a circuit diagram according to a second embodiment of a vertical synchronizing separation circuit of the present invention;

Fig. 6 shows a circuit diagram of a frequency divider for use in a vertical synchronizing separation circuit according to the present invention;

Fig. 7 illustrates the waveforms observed at major points in the circuit of Fig. 5, during when the vertical synchronizing signal is properly received;

Fig. 8 illustrates the waveforms observed at major points in the circuit of Fig. 5, during when the vertical synchronizing signal is not received;

Fig. 9 shows a circuit diagram according to a third embodiment of a vertical synchronizing separation circuit of the present invention; and

Fig. 10 illustrates the waveforms observed at major points in the circuit of Fig. 9.

Fig. 2 shows a circuit diagram of a conventional integrated vertical synchronizing separation circuit. In fig. 2, a numeral 13 designates a transistor for performing a switching operation (on/off) when the base thereof is applied with a composite synchronizing signal from a composite synchronizing separation circuit 3; numerals 14 to 16 designate constant current transistors having emitters thereof connected with a power supply (+ Vcc) through resistors 17 to 19 respectively; a numeral 20 designates a diode which is supplied with a constant current by the constant current transistors 14 and 15; a numeral 21 designates a transistor wherein the collector thereof is supplied with a constant current by the constant current transistor 16, and the base thereof is connected with the collector of the transistor 13; a numeral 22 designates a capacitor which is charged and discharged according to the on and off switching operation of the transistor 21; a numeral 23 designates a comparing circuit wherein the non-inverting input terminal thereof is connected with one edged portion of the capacitor 22, and the inverting input terminal thereof is connected with a reference supply E_0 ; a numeral 24 designates an output transistor wherein a driving pulse for vertical deflection from a transistor 25 is impressed on the

base thereof, and the collector thereof is connected with the power supply (+ Vcc) through a diode 26 and a resistor 27, and the emitter thereof is connected with an outer variable resistor 28, which will serve as a load, through an output pin 11; and a numeral 29 designates a bias circuit for temperature compensation comprising resistors 30 and 31, and diodes 32 and 33. In addition, if the resistance value of the resistor 27 is assumed to be "1", each of the resistance values of the resistors 17 to 19 is set to be M ($M \geq 1$). Also, if the area of the emitter of the diode 26 is assumed to be "1", each area of the emitters of the constant current transistors 14 to 16 is set to be $1/M$. Accordingly, if an electric current flowing between the collector and the emitter in the transistor 24 is assumed to be "1", an electric current flowing between the collector and the emitter in each of the transistors 14, 15, and 16 is $1/M$. Furthermore, each emitter area of the diode 20 and the transistor 21 is designed to be equal to each other, and therefor, the diode 20 and transistor 21 compose a current mirror circuit. The same circuit elements as those of Fig. 1 are provided with similar reference number, and the description therefor is omitted for the sake of brevity.

In Fig. 2, a video signal is applied through input pin 2 to a composite synchronizing separation circuit 3, in which a composite synchronizing signal as shown by S1 in Fig. 3 is separated. The composite synchronizing signal is applied to a signal generating circuit 9, and also to the base of the transistor 13.

When a rectangular pulse, for example, P1 is impressed on the base of the transistor 13, the transistor 13 switches on, and the transistor 21 switches off. Accordingly, during the pulse period of the pulse P1 as shown by a line Nc of S2 in Fig. 3, the capacitor 22 is charged by a constant current I_0 generated from the constant current transistor 16, and the voltage resulting from the charge is impressed on the non-inverting input terminal of the comparing circuit 23.

When the rectangular pulse P1 to the base of the transistor 13 disappears, the transistor 13 switches off, and the transistor 21 switches on. Since the diode 20 and the transistor 21 define a current mirror circuit, an electric current $2I_0$, which is the sum of an electric current I_0 flowing through each of the constant current transistors 14 and 15, flows into the diode 20. Moreover, an electric current $2I_0$, which is the sum of an electric current I_0 of the constant current transistor 16 and a discharging electric current I_0 of the capacitor 22, flows into the transistor 21. Therefore, when the pulse P1 disappears, the capacitor 22 is discharged as shown by a line Nd in Fig. 3. As mentioned above, when the base of the transistor

13 is impressed by a composite synchronizing signal as shown by S1 in Fig. 3, the non-inverting input terminal of the comparing circuit 23 is impressed by the output signal from the capacitor 22 as shown by S2 of Fig. 3. If the voltage from the reference supply in the comparing circuit 23 is set as shown by a single dot chain line S2 in Fig. 3, a rectangular pulse as shown by A in Fig. 3 is applied as a reset signal to the frequency divider 8 from the comparing circuit 23. It is to be noted that, for example, the reset signal (shown by A of Fig. 3) is so regulated as to be outputted at each 261.5H ('H' represents one cycle period of a horizontal synchronizing signal) after the former reset.

The frequency divider 8 receives a signal with a 2fH as a clock signal from the signal-generating circuit 9, and outputs a vertical synchronizing pulse as shown by B in Fig. 3, according to a rectangular pulse from the comparing circuit 23 as shown by A in Fig. 3, and resets itself synchronously.

The details of the frequency divider 8 will be described later in connection with Fig. 6. A vertical synchronizing pulse (positive going) obtained as mentioned above is impressed on the base of the transistor 25. In accordance with the impression, a vertical synchronizing pulse (negative going) is generated from the emitter of the output transistor 24, so that a vertical deflection circuit 12 connected to one end of the variable resistor 28 is driven.

It is to be noted that the constant current flowing into the transistors 14 to 16 is determined according to the adjustment of the variable resistor 28. For example, if the resistances of the resistors 30 and 31 are made equal to each other, and the transistor 25 switches off, the voltage from the emitter in the output transistor 24 results in $1/2 V_{cc}$. Therefore, the electric current from the emitter in the output transistor 24 results in a value I_1 which is determined by the voltage $1/2 V_{cc}$ from the emitter and the value of the externally connected variable resistor 28 of the integrated circuit ICI. Since the electric current of the emitter and that of the collector in the output transistor 24 can be considered to be equal to each other, an electric current I_1 flows into each of the diode 26 and the resistor 27. Moreover, the diode 26 and each of the constant current transistors 14 to 16 are connected in such a manner as to define a current mirror circuit having a current ratio of $1 : 1/M$. Therefore, a constant current of $1/M \cdot I_1 (= I_0)$ flows in each of the transistors 14 to 16. Accordingly, since variable resistor 28 regulates the electric current I_1 and, in turn, the electric current I_0 , the electric current for charging the capacitor 22 can be regulated.

Since the base of the output transistor 24 is connected with a bias circuit 29 for the temperature compensation, and the externally connected vari-

able resistor 28 has a small temperature dependency, in comparison with the resistor provided inside the integrated circuit ICI, the output current of the output transistor 24 will take a predetermined value determined by the value of the variable resistor 28. Therefore, the change of the detecting sensitivity for detecting the vertical synchronizing signal due to the temperature variation can be maintained constant.

As has been described, according to the present embodiment, with a very small amount of electric current, the capacitor can be charged and discharged in accordance with the composite synchronizing signal, so that the capacitor having small capacity can be employed, which is capable of being incorporated in an integrated circuit, therefore, the number of the externally provided circuit components can be decreased. Moreover, since the current for charging and discharging the capacitor is determined by the current flowing through the load connected to the output pin for the drive pulse for use in vertical deflection, no particular control pin is necessary. Thus, it is possible to decrease the number of pins provided in the integrated circuit to enable the designing of the integrated circuit with a high efficiency.

Fig. 4 shows the first embodiment according to the present invention. The vertical synchronizing separation circuit VS, as shown in Fig. 2, is so designed as to have a low detecting sensitivity to enable the separation of only the vertical synchronizing signal and not to be influenced by the noise signals or other signals. In other words, the circuit is made to have a small amount of charging electric current I_0 . However, when the vertical synchronizing separation circuit has a low detecting sensitivity, there is such a problem that the vertical synchronizing signal can not be detected when receiving a signal of weak electric field, that is, when the received signal as shown by S1 in Fig. 3 has a low level amplitude, or when the waveform of the synchronizing signal is deformed. Especially, out in the mountainous country where reception of the television signal is poor, such a problem occurs constantly, resulting in such a problem that the television picture will be deformed and blurred.

In the first embodiment according to the present invention, the integrated circuit further comprises transistors 40, and 42, and resistors 39, and 41. The base of the transistor 40 is connected with the collector of an output transistor 24, and the collector of the transistor 40 is grounded through the resistor 41. The base of the transistor 42 is connected with the midpoint of the connecting line between the collector of the transistor 40 and the resistor 41, and the collector of the transistor 42 is connected with the base of the transistor 21 in the first vertical synchronizing separation circuit VS. A

diode 26 is connected with the transistor 40 and each of the constant current transistors 14 to 16 in such a manner as to define a current mirror circuit having a current ratio of $1 : 1/M(M \geq 1)$. A second vertical synchronizing separation circuit 43, which has a high detecting sensitivity, a transistor 45, and a resistor 44 are externally connected to the integrated circuit and also to the variable resistor 28. The second vertical synchronizing separation circuit 43 may be configured in the same way, for example, as the circuit VS, or the circuit 7 in Fig. 1.

When the level of the waveforms as shown by S1 in Fig. 3 is sufficiently large, and the received electric wave is excellent, a positive going vertical synchronizing pulse (B in Fig. 3) is outputted from a frequency divider 8, and a negative going vertical synchronizing pulse which changes from $1/2 V_{cc}$ to "0" is outputted from a pin 11. It is assumed that variable resistor 28 has a resistance R_0 . When the negative going vertical synchronizing pulse is not generated and, at the same time, the emitter voltage of the transistor 24 is $1/2 V_{cc}$, an electric current $V_{cc}/2R_0$ flows into the transistor 24, and also, an electric current $V_{cc}/2MR_0$ flows into the transistor 40 which is in a current mirror relationship with the diode 26. It is to be noted that the value R_1 of the resistor 41 is so set that: $(V_{cc} \cdot R_1) / 2MR_0 < V_{be}$ (wherein, V_{be} represents a base-emitter voltage of the transistor 42). Accordingly, when the received electric wave is excellent, the transistor 42 is maintained switched off.

Next, the description is directed to a case in which the received electric wave is so poor that the composite synchronizing signal of high level can not be obtained from the composite synchronizing separation circuit 3, and that no vertical synchronizing pulse as shown in Fig. 3 is outputted from the frequency divider 8. Since it is not necessary for the second vertical synchronizing separation circuit 43 to obtain the horizontal synchronizing signal from the video signal, the circuit 43 can obtain a vertical synchronizing pulse in high sensitivity, even when the first vertical synchronizing circuit VS can not separate a vertical synchronizing pulse. A vertical synchronizing signal obtained from the second vertical synchronizing separation circuit 43 is applied to the base of the transistor 45, and thereby switches transistor 45 on. If the value of the resistor 44 is assumed to be R_2 , an electric current of $(V_{cc}/2)(1/R_0 + 1/R_2)$, i.e., the sum of electric current flowing in the variable resistor 28 and the resistor 44, flows into the output transistor 24, and the same current flows also into the diode 26. In addition, the value of the resistor 44 is so set as to be $(V_{cc}/2M)(1/R_0 + 1/R_2)R_1 > V_{be}$. Accordingly, an electric current of $(V_{cc}/2M)(1/R_0 + 1/R_2)$ flows into the transistor 40, and the electric current value is larger than the electric current value as obtained

in the case where the received electric wave is excellent, as mentioned above. Therefore, the transistor 42 switches on so as to ground the base of the transistor 21 in the first synchronizing separation circuit VS. In other words, when a vertical synchronizing signal is detected in the second vertical synchronizing separation circuit 43, the transistor 21 is maintained switched off while the vertical synchronizing signal is present. As a result, a capacitor 22 is charged in the same way as in the case where an output is generated from the composite synchronizing separation circuit 3, and thus a reset signal is impressed on the frequency divider 8 from a comparing circuit 23. Accordingly, the frequency divider 8 is reset in the same way as mentioned above, and a vertical drive pulse is outputted from the output pin 11.

It is to be noted that even if an output is generated from the second vertical synchronizing separation circuit 43, the voltage of the output pin 11 is not varied. Thus, the output from the second vertical synchronizing separation circuit 43 will not adversely affect the operation when a vertical synchronizing pulse is generated normally.

Next, the second embodiment according to the present invention will be described in connection with Figs. 5 to 8.

In the preceding embodiment, when it is necessary to examine the frequency dividing operation of frequency divider 8 in the integrated circuit, the waveforms of the vertical drive pulse generated from the output pin 11 are observed. However, in order to detect whether or not the vertical synchronizing pulse is generated according to a normal counting operation, a pulse interval between subsequent two vertical synchronizing pulses must be examined, resulting in such a problem that the detection requires troublesome procedures.

In comparison with the first embodiment shown in Fig. 2, the second embodiment shown in Fig. 5 further comprises a transistor 50, a diode 51, and a resistor 52. Moreover, frequency divider 8 is provided with outputs B and C. The second frequency divided output C from the frequency divider 8 is impressed on the base of the transistor 50, and the emitter thereof is connected to ground. Still furthermore, the diode 51 and the resistor 52 are connected in series with diodes 32 and 33, and resistors 30 and 31, so that the resistors 30 and 31, the diodes 32, 33, and 51, and the resistor 52 compose a bias circuit for temperature compensation.

Fig. 6 shows the details of the frequency divider 8. A pulse having a frequency $2fH$ applied to the clock terminal X is divided in a divider defined by T flip-flops 137 to 146, which are connected in series. After the entire dividers 137 to 146 have been reset, and when 512 input pulses are counted to reach 256H, an output from Q of the last flip-flop

146 produces a HIGH level signal. The HIGH level signal is impressed on an input of a NAND circuit 147. As a result, while the output from the T flip-flop 146 produces a HIGH level signal, an invert signal of the output of Q terminal of flip-flop 140 is generated as the second frequency divided output at point C. After 260H has passed since the reset, a pulse signal (shown By C in Fig. 7) is outputted from the point C. However, in the case where the flip-flops are not reset after 260H, a pulse signal having a period 8H (shown by C in Fig. 8) is outputted from the point C. Next, the operation of the frequency divider 8 shown in Fig. 6 will be described.

When a reset pulse (shown by A in Fig. 7) is impressed on reset terminal A from comparator 23, SR flip-flop 148 is set, and the output from Q thereof is impressed on D flip-flop 150 through a NOR circuit 149. Since a terminal C of the D flip-flop 150 is connected with a clock terminal X, D flip-flop 150 acts as a delay circuit which can perform a delay of the maximum 0.5H. Accordingly, after an output from the NOR circuit 149 is impressed, Q terminal produces an output in response to a next clock pulse, and therefore the output from the Q terminal is delayed by the maximum 0.5H and is applied to each of dividers 137 to 146 to reset the same. Moreover, the Q output is applied to a set-input of SR flip-flop 152 through inverter 151 to produce an output pulse (B in Fig. 7), from point B, as a first frequency-divide output. Then, the dividers 137 to 146 start counting in response to the next clock pulses (which are delayed by 0.5H). Furthermore, since the SR flip-flop 152 is reset after all the dividers 137 to 146 are reset and then, when 8.5H has been counted, the Q output from the flip-flop 152 produces a LOW level signal again. Accordingly, from the point B, an output pulse having a pulse width 8.5H is generated.

For example, when the received electric waves are so poor that no reset signal will be impressed on the reset terminal of a point A (as shown by a dotted line in Fig. 8), the counting operation of dividers continues even after the period of 261.5H. Then, when 296H are counted, the entire inputs of AND circuit 153 are HIGH level signals, so that the output thereof is also a HIGH level signal, thereby triggering the D flip-flop 150. Thus, after a further 0.5H period from the 296H period, the dividers are all reset and, at the same time, SR flip-flop 152 is set to generate an output pulse (shown by B in Fig. 8) from the point B.

As apparent from the above description, the SR flip-flop 152 is set either by the reset signal impressed on the point A, or by the output signal from the AND circuit 153. Fig. 7 shows a case when the SR flip-flop 152 is set by the reset signal

impressed on the point A; and Fig. 8 shows a case when the SR flip-flop 152 is set by the output signal from the AND circuit 153.

Referring again to Fig. 5, in the case of an NTSC system, a vertical synchronizing signal appears after a period of 262.5H. As shown by A in Fig. 7, when a vertical synchronizing signal is separated properly, a frequency divider 8, as shown by B in Fig. 7, is reset after a period of 262H, and at the same time, a HIGH level reset pulse having a pulse period of 8.5H is produced from the point B. Moreover, as shown by C in Fig. 7, after a period of 260H, a negative going pulse having a pulse width 2H is outputted from a point C. Accordingly, before a period 260H, a transistor 50 is maintained switched on, and a transistor 25 is maintained switched off, and therefore, resistors 30 and 31 (having the same resistance to each other) are eventually connected in series between a power supply +Vcc and the ground. Thus, the electric potential of the emitter (a point D) of a transistor 24 will be $V_{cc}/2$.

During a period between 260H and 262H, both of the transistors 50 and 25 are switched off, and therefore, the resistors 30, 31, and 52 (having the same resistance to each other) are eventually connected in series between the power supply +Vcc and the ground. Thus, the electric potential of the emitter (point D) becomes $2V_{cc}/3$.

At 262H, the frequency divider 8 is reset to be "0"H, and therefore, the transistor 25 switches on for a period of 8.5H, during which the point D is grounded, regardless of the on and off switching operation of the transistor 50.

As understood from the frequency description, the electric potential of the point D is varied as shown by D in Fig. 7, and a negative going pulse, serving as a vertical synchronizing pulse, is produced from pin 11. Moreover, until 260H, since the electric potential at point D is $V_{cc}/2$, the electric current flowing into the transistor 24 is $V_{cc}/2R_0$. But after 260H and before the generation of the vertical synchronizing signal, the electric potential at point D rises to $2V_{cc}/3$, and at the same time, the electric current flowing into the transistor 24 increases to $2V_{cc}/3R_0$.

Since it can be considered that the electric current flowing into the emitter and the current flowing out from the collector of the output transistor 24 are equal to each other, the electric currents flowing through the constant current transistors 14 to 16, which are in a current-mirror relationship with the diode 26, show a small value $V_{cc}/2MR_0$ after 260H. However, the currents flowing through transistors 14 to 16 show a large value $2V_{cc}/3MR_0$ until before the generation of the vertical synchronizing pulse. Therefore, when the current $2V_{cc}/3MR_0$ flows through transistors 14 to 16, the

electric current for charging the capacitor 22 will be greater than that obtained when the electric current $V_{cc}/2MR_0$ flows through transistors 14 to 16. Therefore, the detecting sensitivity of the vertical synchronizing signal can be improved to enable the detection even in the case of a weak electric field.

Next, in the case where the received signal is so poor that the vertical synchronizing signal can not be separated, as shown by a dotted line A in Fig. 8, after the lapsed period of 260H, frequency divider 8 repeatedly outputs pulses having a period 8H, as shown by C in Fig. 8. At 296H, AND circuit 153 outputs a HIGH level signal which is a quasi vertical synchronizing signal generated by the frequency divider 8. Then, after the delay of 0.5H, a reset pulse is outputted from a flip-flop 150 to reset the dividers, and at the same time, a reset pulse having a pulse width 8.5H is outputted from a point B.

Accordingly, until 260H, the transistor 50 is maintained switched on, and the transistor 25 is maintained switched off, so that in the same manner as described above, the electric potential at point D is maintained $V_{cc}/2$.

From 260H to 296H, transistor 25 is maintained off and transistor 50 repeats on and off at a period of 8H. Accordingly, the electric potential at point D will be at $V_{cc}/2$ and $2V_{cc}/3$ repeatedly.

At 296.5 H, the dividers are all reset to be be "0" H, and thereafter, for a period of 8.5H, the transistor 25 is maintained switching on to ground point D in the same way as described above.

In this way, the voltage at point D changes as shown by D in Fig. 8, in which the negative going pulses are the vertical synchronizing pulses produced from pin 11. The positive going pulse period which is between 260H and 296H, can be detected readily by connecting an oscilloscope to pin 11. Therefore, by detecting these positive going pulses generated properly, it can be confirmed that the frequency divider operates properly.

According to the second embodiment, since an output terminal of the output transistor will produce a vertical drive pulse and a signal having a waveform which shows the operation condition of the frequency divider, the frequency divider in an integrated circuit can be checked readily. Also, since no particular check pin is required for such a check, a synchronizing signal generator suited to be formed in an integrated circuit can be provided. Furthermore, as shown in the embodiment, when the vertical synchronizing signal is detected by selecting a detection sensitivity according to the output signal generated from the emitter of the output transistor, the detection can be carried out without any failure even in the case where the level of the vertical synchronizing signal is low such as when the electric field is weak.

Referring to Figs. 9 and 10, the third embodiment according to the present invention will be described.

The circuit provided in the form of the integrated circuit according to the third embodiment is equivalent to a circuit which is obtained by combining integrated circuits described in the first and the second embodiments. Moreover, as the external circuit, a circuit defined by resistors 60, 63, and 64, transistors 61 and 66, a capacitor 62, and a reference voltage supply 65 is connected to pin 11.

In Fig. 10, waveforms D and D' correspond to waveforms shown in Figs 7D and 8D, and waveforms F and D'' are obtained at point F and D in the third embodiment.

When a reset signal can not be impressed on a point A due to the influence of the ghost interferences after 260H, pulses having a period 8H are outputted, as the second frequency-dividing output from a point C of the frequency divider 8. Also, the emitter voltage of output transistor 24 switches between $V_{cc}/2$ and $2V_{cc}/3$ at a period 4H repeatedly.

In the externally provided circuit shown in Fig. 9, if the voltage from a reference voltage supply 65 for the transistor 66 is assumed to be, for example, $(2V_{cc}/3) - V_{be}$, transistor 66 switches on to charge capacitor 62 while output pin 11 is producing $2V_{cc}/3$. Therefore, when a signal having a waveform shown by D' in Fig. 10 is produced from pin 11 in the case where no vertical synchronizing signal is present, capacitor 62 will be charged, so that the charged voltage thereof shows such a waveform as shown by F in Fig. 4. Then, if the threshold level of the transistor 61 is set at a level indicated by a single dot chain line, the transistor 61 will switch on at 279H. If the resistance of the resistor 60 is assumed to be R_3 , an electric current flowing through the transistor 24 will be equal to the sum of electric currents flowing through resistors 28 and 60, which can be expressed as follows: $2V_{cc}/3 \cdot (1/R_0 + 1/R_3)$. Also, the same amount of electric current flows through the diode 26. Therefore, an electric current of $2V_{cc}/3M \cdot (1/R_0 + 1/R_3)$ flows through a transistor 40 to switch transistor 42 on. Accordingly, transistor 21 of vertical synchronizing separation circuit Vs switches off, and capacitor 22 will be charged in the same manner as mentioned above. As a result, a reset signal is impressed on the frequency divider 8 from a comparing circuit 23, so that the frequency divider 8 will generate the first frequency dividing output signal, and that the output pin will generate the vertical drive pulse as shown by D'' in Fig. 4.

In addition, the resistance of resistor 63 is selected to have such a value that the electric current which flows when the transistor 66 switches

on will no influence the electric current flowing through the output transistor 24. Furthermore, by adjusting the variable resistor 64, it is possible to manually adjust the timing for resetting the frequency divider 8. For example, if the variable resistor 64 is set to take a large resistance, the capacitor 62 will discharge in accordance with a curve with less change, so that the frequency divider 8 may be reset before 279H. On the contrary, if the variable resistor 64 is set to take a small resistance, the capacitor 62 will discharge rapidly, so that the frequency divider 8 may be reset after 279H. Accordingly, an operator may adjust, while he is viewing the television screen to obtain a position which can acquire the synchronization rapidly with a high stability.

As have been described above, the present embodiment makes it possible to form the vertical synchronizing separation circuit in an integrated circuit and also to decrease the number of pins. Furthermore, even when the ghost interferences occur to fail the detection of the vertical synchronizing signal from the video signal, frequency divider 8 can be reset by itself or by a quasi vertical synchronizing signal provided from the outside the integrated circuit. Therefore, a vertical drive pulse can be obtained with a high stability even in the case of a vertical deflection circuit of countdown system.

Still furthermore, by adjusting the variable resistor in the external circuit, the timing when to produce the quasi vertical synchronizing signal can be adjusted, so that the operator may quickly adjust, while he is viewing the television screen, to obtain a position which can acquire the stable vertical synchronized condition.

An Explanation of the numerals and the lettering on the Drawings

VS : a vertical synchronizing separation circuit,
 3 : a composite synchronizing separation circuit,
 8 : frequency dividing means, 9 : signal-generating means,
 13 to 16, and 21 : transistors,
 16, and 19 : a constant current source,
 21 : reset-signal-generating means, 22 : a condenser,
 23 : a comparing circuit, 28 : an outer load,
 24, 25, and 29 : output means,
 14 to 19, 26, and 27 : sensitivity-controlling means,
 40, and 42 : load-electric-current-detecting means,
 43 : the second vertical synchronizing signal separation means,
 44, and 45 : variable-load-electric-current

Claims

1. A vertical synchronizing pulse generator comprising: a first vertical synchronizing signal separation means (VS) for separating a vertical synchronizing signal included in a composite video signal;
 a signal generating means (9) for generating a signal having a frequency which is a predetermined number times as many as the frequency of a horizontal synchronizing signal included in the composite video signal;
 a frequency dividing means (8), which receives an output signal from said first vertical synchronizing signal separation means as a reset signal and also receives said signal from said signal generating means as a clock signal, for dividing said clock signal;
 characterized by an output means (25, 24 and 29) for supplying an output signal to a load according to an output from said frequency dividing means; and
 a sensitivity controlling means (26, 27, and 14 to 19) for controlling a separation sensitivity of said first vertical synchronizing signal separation means according to the electric current flowing through the load by controlling charging and discharging currents of a capacitor (22) of the first vertical synchronizing signal separation circuit via said output means;
 a second vertical synchronizing signal separation means (43) which is connected to said load and having a separation sensitivity which is superior to that of said first vertical synchronizing circuit;
 a load current varying means (44 and 45) for varying an electric current flowing through the load in accordance with an output from said second vertical synchronizing signal separation means;
 a load electric current detecting means (40 and 42) for detecting the electric current flowing through the load; and
 a reset signal generating means (21) for generating a reset signal which resets said frequency dividing means according to an output from said load electric current detecting means.
2. The vertical synchronizing pulse generator as claimed in claim 1 further comprising:
 a bias means (30, 31, 32, 33, 51, and 52) for biasing said output means; and
 a bias switching means (50) for switching the bias of said bias means according to an output generated when said frequency dividing means performs a predetermined frequency dividing operation,



on will no influence the electric current flowing through the output transistor 24. Furthermore, by adjusting the variable resistor 64, it is possible to manually adjust the timing for resetting the frequency divider 8. For example, if the variable resistor 64 is set to take a large resistance, the capacitor 62 will discharge in accordance with a curve with less change, so that the frequency divider 8 may be reset before 279H. On the contrary, if the variable resistor 64 is set to take a small resistance, the capacitor 62 will discharge rapidly, so that the frequency divider 8 may be reset after 279H. Accordingly, an operator may adjust, while he is viewing the television screen to obtain a position which can acquire the synchronization rapidly with a high stability.

As have been described above, the present embodiment makes it possible to form the vertical synchronizing separation circuit in an integrated circuit and also to decrease the number of pins. Furthermore, even when the ghost interferences occur to fail the detection of the vertical synchronizing signal from the video signal, frequency divider 8 can be reset by itself or by a quasi vertical synchronizing signal provided from the outside the integrated circuit. Therefore, a vertical drive pulse can be obtained with a high stability even in the case of a vertical deflection circuit of countdown system.

Still furthermore, by adjusting the variable resistor in the external circuit, the timing when to produce the quasi vertical synchronizing signal can be adjusted, so that the operator may quickly adjust, while he is viewing the television screen, to obtain a position which can acquire the stable vertical synchronized condition.

An Explanation of the numerals and the lettering on the Drawings

VS : a vertical synchronizing separation circuit,
 3 : a composite synchronizing separation circuit,
 8 : frequency dividing means, 9 : signal-generating means,
 13 to 16, and 21 : transistors,
 16, and 19 : a constant current source,
 21 : reset-signal-generating means, 22 : a condenser,
 23 : a comparing circuit, 28 : an outer load,
 24, 25, and 29 : output means,
 14 to 19, 26, and 27 : sensitivity-controlling means,
 40, and 42 : load-electric-current-detecting means,
 43 : the second vertical synchronizing signal separation means,
 44, and 45 : variable-load-electric-current

Claims

1. A vertical synchronizing pulse generator comprising: a first vertical synchronizing signal separation means (VS) for separating a vertical synchronizing signal included in a composite video signal;
 a signal generating means (9) for generating a signal having a frequency which is a predetermined number times as many as the frequency of a horizontal synchronizing signal included in the composite video signal;
 a frequency dividing means (8), which receives an output signal from said first vertical synchronizing signal separation means as a reset signal and also receives said signal from said signal generating means as a clock signal, for dividing said clock signal;
 characterized by an output means (25, 24 and 29) for supplying an output signal to a load according to an output from said frequency dividing means; and
 a sensitivity controlling means (26, 27, and 14 to 19) for controlling a separation sensitivity of said first vertical synchronizing signal separation means according to the electric current flowing through the load by controlling charging and discharging currents of a capacitor (22) of the first vertical synchronizing signal separation circuit via said output means;
 a second vertical synchronizing signal separation means (43) which is connected to said load and having a separation sensitivity which is superior to that of said first vertical synchronizing circuit;
 a load current varying means (44 and 45) for varying an electric current flowing through the load in accordance with an output from said second vertical synchronizing signal separation means;
 a load electric current detecting means (40 and 42) for detecting the electric current flowing through the load; and
 a reset signal generating means (21) for generating a reset signal which resets said frequency dividing means according to an output from said load electric current detecting means.
2. The vertical synchronizing pulse generator as claimed in claim 1 further comprising:
 a bias means (30, 31, 32, 33, 51, and 52) for biasing said output means; and
 a bias switching means (50) for switching the bias of said bias means according to an output generated when said frequency dividing means performs a predetermined frequency dividing operation,

whereby a signal indicative of the frequency-dividing condition whether or not a frequency divider is operating properly is produced at a load terminal as a voltage signal.

3. The vertical synchronizing pulse generator as claimed in claim 2 further comprising:
a reset signal generating means (60 to 65, 40, 42, and 21) for generating a voltage corresponding to an electric current flowing through the load, and for generating a reset signal when said voltage exceeds a predetermined level.

Patentansprüche

1. Vertikalsynchronpuls-Generator mit:
einer ersten Vertikalsynchronsignal-Trenneinrichtung (VS) zur Abtrennung eines Vertikalsynchronsignals, das in einem zusammengesetzten Videosignal enthalten ist;
einer Signalgeneratoreinrichtung (9) zur Erzeugung eines Signals mit einer Frequenz, die ein vorgegebenes Vielfaches der Frequenz eines Horizontalsynchronsignals aufweist, das im zusammengesetzten Videosignal enthalten ist;
einer Frequenzteiler-Einrichtung (8), die ein Ausgangssignal von der ersten Vertikalsynchronsignal-Trenneinrichtung als Rückstellsignal erhält und ferner das Signal von der Signalgenerator-Einrichtung als Taktsignal erhält, zur Teilung des Taktsignals;
gekennzeichnet durch eine Ausgangseinrichtung (25, 24 und 29) zum Zuführen eines Ausgangssignals an eine Last entsprechend einem Ausgangssignal von der Frequenzteiler-Einrichtung; und eine Empfindlichkeits-Steuereinrichtung (26, 27 und 14 bis 19) zum Steuern der Trennempfindlichkeit der ersten Vertikalsynchronsignal-Trenneinrichtung entsprechend eines elektrischen Stroms, der durch die Last fließt, durch Steuern der Lade- und Entladeströme eines Kondensators (22) der ersten Vertikalsynchronsignal-Trennschaltung über die Ausgangseinrichtung;
eine zweite Vertikalsynchronsignal-Trenneinrichtung (43), die mit der Last verbunden ist und eine Trennempfindlichkeit aufweist, die größer ist als die der ersten Vertikalsynchronschaltung;
einer Laststrom-Änderungseinrichtung (44 und 45) zum Ändern eines elektrischen Stroms, der durch die Last fließt, in Abhängigkeit von einem Ausgangssignal der zweiten Vertikalsynchron-Trenneinrichtung;
eine Laststrom-Detektoreinrichtung (40 und 42) zur Erfassung des elektrischen Stroms, der durch die Last fließt;

und eine Rückstellsignal-Erzeugungseinrichtung (21) zur Erzeugung eines Rückstellsignals, das die Frequenzteiler-Einrichtung gemäß einem Ausgangssignal von der Laststrom-Erfassungseinrichtung rückstellt.

2. Vertikalsynchronpuls-Generator nach Anspruch 1 mit ferner:
einer Vorspanneinrichtung (30, 31, 32, 33, 51 und 52) zum Vorspannen der Ausgangseinrichtung; und
einer Vorspann-Umschalteneinrichtung (50) zum Schalten der Vorspannung der Vorspanneinrichtung gemäß einem Ausgangssignal, das erzeugt wird, wenn die Frequenzteiler-Einrichtung einen vorgegebenen Frequenzteiler-Betrieb durchführt, wobei ein Signal bezüglich eines Frequenzteiler-Zustandes, das angibt, ob ein Frequenzteiler ordnungsgemäß arbeitet, an einem Lastanschluß als Spannungssignal erzeugt wird.
3. Vertikalsynchronpuls-Generator nach Anspruch 2, mit ferner:
einer Rückstellsignal-Erzeugereinrichtung (60 bis 65, 40, 42 und 21) zur Erzeugung einer Spannung entsprechend einem durch die Last fließenden elektrischen Strom und zur Erzeugung eines Rückstellsignals, wenn diese Spannung einen vorgegebenen Pegel überschreitet.

Revendications

1. Générateur d'impulsions de synchronisation verticale comprenant :
- un premier moyen de séparation de signal de synchronisation verticale (VS) pour séparer un signal de synchronisation verticale compris dans un signal vidéo composite;
 - un moyen de génération de signal (9) pour générer un signal possédant une fréquence qui est un multiple prédéterminé de la fréquence d'un signal de synchronisation horizontale compris dans le signal vidéo composite;
 - un moyen de division de fréquence (8) recevant un signal de sortie dudit premier moyen de séparation de signal de synchronisation verticale comme signal de réinitialisation et recevant de même ledit signal dudit moyen de génération de signal comme signal de synchronisation pour diviser ledit signal de synchronisation;
- générateur caractérisé par un moyen de sortie (25, 24 et 29) pour fournir un signal de sortie à une charge selon la



sortie dudit moyen de division de fréquence et un moyen de commande de la sensibilité (26, 27 et 14 à 19) pour commander une sensibilité de séparation dudit premier moyen de séparation de signal de synchronisation verticale selon le courant électrique traversant la charge à l'aide d'une commande des courants de charge et de décharge d'un condensateur (22) du premier circuit de séparation du signal de synchronisation verticale via ledit moyen de circuit;

- un second moyen de séparation du signal de synchronisation verticale (43) qui est raccordé à ladite charge et possédant une sensibilité de séparation qui est supérieure à celle dudit premier circuit de synchronisation verticale;
- un moyen de variation du courant de charge (44 et 45) pour modifier un courant électrique traversant la charge selon une sortie dudit second moyen de séparation du signal de synchronisation verticale;
- un moyen de détection du courant électrique de charge (40 et 42) pour la détection du courant électrique traversant la charge; et
- un moyen de génération de signal de réinitialisation (21) pour générer un signal de réinitialisation dudit moyen de division de fréquence selon une sortie dudit moyen de détection du courant électrique de charge.

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2. Générateur d'impulsions de synchronisation verticale selon la revendication 1, comprenant, de plus :

- un moyen de polarisation (30, 31, 32, 33, 51 et 52) pour polariser ledit moyen de sortie; et
- un moyen de commutation de polarisation (50) pour commuter la polarisation dudit moyen de polarisation selon une sortie générée lorsque ledit moyen de division de la fréquence effectue une opération prédéterminée de division de la fréquence, un signal indiquant la condition de division de fréquence selon laquelle un diviseur de fréquence fonctionne correctement ou pas, étant ainsi produit sur une borne de charge comme signal de tension.

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3. Générateur d'impulsions de synchronisation verticale selon la revendication 2, comprenant de plus un moyen de génération de signal de réinitialisation (60 à 65, 40, 42 et 21) pour

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générer une tension correspondant à un courant électrique traversant la charge et pour générer un signal de réinitialisation lorsque ladite tension dépasse un niveau prédéterminé.

