HIGH BANDWIDTH DRAM WITH LOW OPERATING POWER MODES

ABSTRACT

A high bandwidth DRAM (60) is provided with two separate bus networks connecting the DRAM (60) to a processor (50). One bus network (63) is a high speed (e.g., 500 MHZ) 8:1 or 16:1 multiplexed I/O bus and the second (62) is a slower (e.g., 64-bit) bus. The high-speed bus (63) is used for example for graphic intensive applications which require fast access to large numbers of bits in the DRAM (60) memory array. This of course results in higher power requirements. Since, not all applications require such large amounts of data to be transferred between the DRAM (60) and the processor (50), the slower bus (62) is provided for these less demanding applications such as word processors, spreadsheets, and the like. The slower bus (62) requires less power to operate and therefore results in a power saving mode which, among other things, facilitates longer battery life.

FIG. 2