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SEMICONDUCTOR INTEGRATED CIRCUIT TESTING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a semiconductor integrated circuit testing apparatus for testing semiconductor devices constructed by a semiconductor integrated circuit, and more particularly to a semiconductor integrated circuit testing apparatus capable of testing semiconductor integrated circuits in which

10 memory sections and logic circuit sections are formed together as a semiconductor integrated circuit in the same single chip.

2. Description of the Related Art

Many of semiconductor integrated circuit testing apparatus for

15 measuring the electrical characteristics of semiconductor integrated circuits by applying a test signal having a predetermined pattern to the integrated circuits being tested have an IC transporting and handling (processing) apparatus (which will be referred to as handler hereinafter) connected therewith for transporting the

20 semiconductor integrated circuits (which will be referred to as IC hereinafter) to be tested to a test or testing section where an IC is brought into electrical contact with a socket on a test head or tester head of the aforesaid testing apparatus, followed after the testing by carrying the tested ICs out of the test section and sorting out them

25 into conforming (defectless or pass) articles and non-conforming (defective or failure) articles on the basis of the test results. The testing apparatus for measuring the electrical characteristics of ICs

by applying a test signal of a predetermined pattern to the ICs, including the IC testing apparatus (IC tester) having the handler of the type described above connected therewith is herein generally termed "IC testing apparatus" or "IC tester".

5 ICs have heretofore been generally classified into two types, one called memory ICs each of which is constructed mainly of a memory section and the other called logic ICs each of which is constructed mainly of a logic circuit section (which will be referred to as logic section). The memory IC has the number of pins (terminals) held to
10 the order of not more than several tens (20 to 40 pins) despite the recent trend towards an increase in memory capacity. In contrast, the logic IC has an enormous number of pins often as many as several hundreds pins (the order of 500 pins).

 Due to the marked difference in number of pins between the
15 memory IC and the logic IC as discussed above as well as the complete difference between the testing methods for the memory IC and the logic IC, it has conventionally been a practice to provide separately the IC testing apparatus for memory ICs (memory testing system) and the IC testing apparatus for logic ICs (logic testing
20 system) and conduct test on memory ICs and logic ICs using completely differently constructed IC testing apparatuses, respectively (particularly the construction of the handlers being different).

 It should be noted here that the recent tendency is toward
25 manufacturing composite ICs (commonly called system LSI) in each of which a memory section of relatively large capacity was built in a logic IC. In order to test such composite ICs, it is naturally desirable

to carry out the overall testing in a form combining the logic and memory sections. Such approach, however, would involve an enormous number of test patterns required for testing, making it difficult to take shape. In addition, it would also necessitate a much longer period of time for testing, keeping the expensive testing system in use for a long time with the undesirable result that the cost required for testing would be excessively high.

In view of the foregoing, generally the manner of extension of the pins (terminals) of composite ICs is contrived so as to permit the memory sections and logic sections to be separately tested, so that it is currently a common practice to test the memory sections and logic sections using by the separate memory IC testing apparatus and logic IC testing apparatus, respectively.

The differences between the IC testing apparatus for memory ICs and the IC testing apparatus for logic ICs both of which have been conventionally in use will now be described in more details.

The memory IC having a relatively small number of pins on the order of 20 to 40 pins permits the use of an IC testing apparatus which is configured to be capable of testing many ICs at a time. As is well known in the art, the IC tester includes a section called test head adapted to write a test signal of a predetermined pattern on ICs under test and to read the written test signal, the test head being constructed separately from the IC tester main frame and disposed in the test section of the handler. Mounted on the test head is a performance board on which there are mounted sockets adapted to electrically contact the pins (terminals) of the ICs under test. The number of contacts that can be formed in this test head is limited (of

the order of 500 to 600), which in turn limits the number of sockets that can be mounted on the test head.

Consequently, in the memory IC tester the test head is equipped with an appropriate number of sockets depending on the number of pins of ICs to be tested, say 16 sockets for the IC with 40 pins so as to enable testing of 16 ICs at one time, 32 sockets for the IC with 20 pins so as to enable testing of 32 ICs at one time, and 64 sockets for the IC with 10 pins so as to enable testing of 64 ICs at one time. In this manner, the number of ICs that can be tested at a time is determined depending on the number of pins of ICs to be tested.

In recent years the one-way trend towards an increase in IC memory capacity tends to extend the length of time required for testing. In view of this, for the memory IC tester, an attempt has been made to shorten the test time and hence reduce the cost required for testing by subjecting many ICs to testing at one time.

In contrast, the logic IC tester is greatly limited as to the number of ICs that can be tested at a time by the number of pins as many as several hundreds pins involved with the logic IC. It is the logic IC tester configured to test one to several ICs at a time that is generally in practical use.

Next, the general construction of the handler used with the prior art IC tester for testing memory ICs will be described with reference to Figs. 4-10.

Fig. 4 is a schematic plan view illustrating one example of the conventional handler for use in transporting and handling memory ICs, with the chamber section shown in a perspective-like view while Fig. 5 is a schematic perspective view of the handler shown in

Fig. 4. The illustrated handler comprises a chamber section 100 for testing ICs (semiconductor memories) which have been brought in as loaded on a test tray TST, an IC storage section 200 for storing ICs to be tested (ICs under test) and ICs already tested and sorted, a loader
5 section 300 where ICs to be tested which a user has beforehand loaded on universal trays (customer trays) KST are transferred and reloaded onto a test tray TST capable of withstanding high/low temperatures, and an unloader section 400 where the tested ICs which have been carried on the test tray TST out of the chamber
10 section 100 subsequently to undergoing a test therein are transferred from the test tray TST to the universal trays KST to be reloaded on the latter. The unloader section 400 is generally configured to sort out tested ICs based on the data of the test results and load them on the corresponding universal trays.

15 The chamber section 100 comprises a constant temperature chamber 101 for imposing temperature stresses of either a designed high or low temperature on ICs under test loaded on a test tray TST, a test chamber 102 for conducting electrical tests on the ICs under the temperature stress imposed in the constant temperature
20 chamber 101, and a heat-removal/cold-removal chamber 103 for removing the temperature stress imposed in the constant temperature chamber 101 from the ICs having undergone the tests in the test chamber 102. The test chamber 102 contains therein the test head 104 for memory testing of the IC tester, the memory
25 testing test head 104 serving to apply various testing electric signals to the ICs electrically contacted with the IC sockets mounted on the memory testing test head 104 and to receive response signals from

the ICs and transmit same to the IC tester.

The test tray TST is moved in a circulating manner from and back to the loader section 300 sequentially through the constant temperature chamber 101 of the chamber section 100, the test
5 chamber 102 of the chamber section 100 and the heat-removal /cold-removal chamber 103 of the chamber section 100, and the unloader section 400. The constant temperature chamber 101 and the heat-removal/cold-removal chamber 103 are taller than the test chamber 102 and have upper portions protruding beyond the top of
10 the latter, as is apparent from Fig. 5. Spanning between these protruding upper portions of the constant temperature and heat-removal/cold-removal chambers 101 and 103 is a base plate 105 as shown in Fig. 5 on which there is mounted a test tray transport 108 by which test trays TST are transported from the heat-removal
15 /cold-removal chamber 103 side toward the constant temperature chamber 101.

If ICs have had a high temperature of, say, about 125°C applied thereto in the constant temperature chamber 101, the heat-removal /cold-removal chamber 103 cools the ICs with forced air down to
20 the room temperature prior to delivering them out to the unloader section 400. If ICs have had a low temperature of, say, about -30°C applied thereto in the constant temperature chamber 101, they are heated with heated air or a heater up to a temperature at which no dewfall or condensation occurs prior to delivering them out to the
25 unloader section 400.

A test tray TST, loaded with ICs to be tested in the loader section 300, is conveyed from the loader section 300 to the constant

temperature chamber 101 of the chamber section 100 which is equipped with a vertical transport configured to support a plurality of (say, nine) test trays TST in the form of a stack. In the illustrated example, a test tray newly received from the loader section 300 is supported on the top of the stack while the lowermost test tray is delivered out to the test chamber 102. ICs to be tested are loaded with either a predetermined high or low temperature stress as the associated test tray TST is moved sequentially from the top to the bottom of the stack by the vertically downward movement of the vertical transport and during a waiting period until the test chamber 102 is emptied. In the center of the test chamber 102 there is located the test head 104. The test tray TST which has been carried one by one out of the constant temperature chamber 101 is placed onto the test head 104 where a predetermined number of ICs out of the ICs under test loaded on the test tray are brought into electrical contact with IC sockets (not shown) disposed on the test head 104, as will be discussed hereinbelow. Upon completion of the test on all of the ICs placed on one test tray through the test head 104, the test tray TST is conveyed to the heat-removal/cold-removal chamber 103 where the tested ICs are relieved of heat or cold to be restored to the room temperature prior to being delivered to the unloader section 400.

Like the constant temperature chamber 101 as described above, the heat-removal/cold-removal chamber 103 is also equipped with a vertical transport adapted to support a plurality of (say, nine) test trays TST stacked one on another. In the illustrated example, a test tray newly received from the test chamber 102 is supported at the

bottom of the stack while the uppermost test tray is discharged to the unloader section 400. The tested ICs are relieved of heat or cold to be restored to the outside temperature (room temperature) as the associated test tray TST is moved successively from the bottom to the top of the stack by the vertically upward movement of the vertical transport.

The tested ICs as carried on the test tray TST are passed to the unloader section 400 where they are sorted out by categories based on the test results and transferred onto and stored in the corresponding universal trays KST. The test tray TST emptied in the unloader section 400 is delivered back to the loader section 300 where it is again loaded with ICs to be tested from the universal tray KST to repeat the same steps of operation.

As shown in Fig. 5, the IC transport for transferring ICs from the universal tray KST to the test tray TST in the loader section 300 may be in the form of X and Y direction transport 304 comprising a pair of opposed parallel rails 301 mounted on the base plate 105 over the loader section 300 and extending in the forward-rearward direction of the handler (referred to as Y direction herein), a movable arm 302 spanning and movably mounted at opposite ends on the pair of rails 301, and a movable head 303 mounted on the movable arm 302 for movement therealong longitudinally of the arm, that is, in the right to left direction of the handler (referred to as X direction herein). With this construction, the movable head 303 is movable in the Y direction between the universal tray KST and the test tray TST as well as in the X direction along the movable arm 302.

The movable head 303 has at least one device grasping head vertically movably mounted on its bottom surface. The movement of the movable head 303 in the X and Y directions and the downward movement of the grasping head bring the grasping head
5 into abutment with an IC placed on the universal tray KST to attract and grasp it by vacuum suction, for instance, for transfer from the universal tray KST to the test tray TST. The movable head 303 may be provided with a plurality of, say, eight grasping heads so that eight ICs at a time may be transported from the universal tray KST
10 to the test tray TST.

It is to be noted here that a position correcting device 305 for correcting the orientation or position of an IC called "preciser" is located between the stop positions for the universal tray KST and test tray TST. The IC position correcting device or preciser 305
15 includes relatively deep recesses into which ICs as being attracted against the grasping heads are released to fall prior to being transferred to the test tray TST. The recesses are each bounded by vertical tapered side walls which prescribe for the depth to which the ICs drop into the recesses by virtue of the tapering. Once eight
20 ICs have been positioned relative to each other by the position correcting device 305, those accurately positioned ICs are again attracted against the grasping heads and transferred to the test tray TST. The universal tray KST is provided with recesses for holding ICs which are oversized as compared to the size of ICs, resulting in
25 wide variations in positions of ICs stored in the universal tray KST. Consequently, if the ICs as such were grasped by the grasping heads and transferred directly to the test tray TST, there might be some of

them which could not be successfully deposited into the IC storage
recesses in the test tray TST. This is the reason for requiring the
position correcting device 305 as described above, which acts to
array ICs as accurately as the array of the IC storage recesses in the
5 test tray TST.

The unloader section 400 is equipped with two sets of X and Y
direction transports 404 which are identical in construction to the X
and Y direction transport 304 provided for the loader section 300.
The X and Y direction transports 404 perform to transship the tested
10 ICs from the test tray TST delivered to the unloader section 400 onto
the universal tray KST. Each set of X and Y direction transport 404
comprises a pair of opposed parallel rails 401 extending in the
forward-rearward direction of the handler (Y direction), a movable
arm 402 spanning and movably mounted at opposite ends on the
15 pair of rails 401, and a movable head 403 mounted on the movable
arm 402 for movement therealong longitudinally of the arm, that is,
in the right to left direction of the handler (X direction).

Fig. 6 shows the construction of one example of the test tray
TST. The illustrated test tray TST comprises a rectangular frame 12
20 having a plurality of equally spaced apart parallel cleats 13 between
the opposed side frame members 12a and 12b of the frame, each of
the cleats 13 having a plurality of equally spaced apart mounting
lugs 14 protruding therefrom on both sides thereof and each of the
side frame members 12a, 12b opposing the adjacent cleats having
25 similar mounting lugs 14 protruding therefrom. The mounting lugs
14 protruding from the opposed sides of each of the cleats 13 are
arranged such that each of the mounting lugs 14 protruding from

one side of the cleat 13 is positioned intermediate two adjacent mounting lugs 14 protruding from the opposite side of the cleat. Similarly, each of the mounting lugs 14 protruding from each of the side frame members 12a and 12b is positioned intermediate two adjacent mounting lugs 14 protruding from the opposed cleat.

Formed between each pair of opposed cleats 13 and between each of the side frame members 12a and 12b and the opposed cleats are spaces for accommodating a multiplicity of IC carriers 16 in juxtaposition. More specifically, each IC carrier 16 is accommodated in one of an array of rectangular carrier compartments 15 defined in each of aforesaid spaces, each compartment 15 including two staggered, obliquely opposed mounting lugs 14 located at the diagonally opposed corners of the compartment. In the illustrated example wherein each cleat 13 has sixteen mounting lugs 14 on either side thereof, there are sixteen carrier compartments 15 formed in each of aforesaid spaces, in which sixteen IC carriers 16 are mounted. Since there are four of the spaces in the illustrated example, 16×4 , that is, 64 IC carriers in total can be mounted in one test tray TST. Each of the IC carriers 16 is attached to two of the mounting lugs 14 in a floating (movable) state by fasteners 17.

Each of the IC carriers 16 is of identical shape and size in its outer contour and has an IC pocket 19 formed in the center for accommodating an IC device therein. The shape of the IC pocket 19 of each IC carrier 16 is determined depending on that of the IC device to be accommodated therein. In the illustrated example, the IC pocket 19 is in the shape of a generally square recess. The outer dimensions of the IC carrier 16 are sized so as to be loosely fitted in

the space defined between the opposed mounting lugs 14 in the carrier compartment 15. The IC carrier 16 has flanges at its opposed ends adapted to rest on the corresponding mounting lugs 14, these flanges being formed therethrough with mounting holes 21 for
5 receiving fasteners 17 therethrough and holes 22 for passing locating pins therethrough.

In case the IC to be tested is of the type having terminal pins (leads) from four sides of either a square or a rectangular thin package as is the case with the QFP (Quad Flat Package), the IC
10 carrier 16 may have the bottom of the IC pocket 19 formed along the four sides thereof with windows (openings) 23 as shown in Fig. 7 so as to expose the terminal pins 18 of the IC through the windows 23 from the bottom toward the backside of the IC carrier 16 so that the exposed terminal pins 18 may be put into contact with the
15 contacts (socket terminals) 24 of the IC sockets mounted on the test head 104 (specifically performance board mounted on the test head 104) as shown in Fig. 8 to effect testing. In order to insure electrical contact between the terminal pins 18 and the contacts 24, on the top of the test head 104 there is mounted a pusher 20 for pushing down
20 on an IC accommodated in each IC carrier 16 to urge the terminal pins 18 against the contacts 24.

As discussed above, the number of ICs which may be tested at a time depends on the number of IC sockets mounted on the test head 104. By way of example, where sixty-four ICs are carried in an
25 array of 4 rows $\times$ 16 columns on a test tray TST as shown in Fig. 9, 4 $\times$ 4, that is, 16 IC sockets are arranged and mounted on the test head 104 such that the ICs (shown as cross-hatched) in every fourth

column in each of the rows may be tested all at once. More specifically, in the first testing run the examination is conducted on sixteen ICs located in the first, fifth, ninth and thirteenth columns in each row, the second testing run is effected on another sixteen ICs
5 located in the second, sixth, tenth and fourteenth columns in each row by shifting the test tray TST by a distance corresponding to one column of ICs, and the third and fourth testing runs are carried out in the similar manner until all of the ICs are tested. The test results are stored in a memory with the addresses determined by the serial
10 numbers (serial numbers in one lot) assigned to the ICs, the identification number affixed to the test tray TST and the numbers assigned to the IC pockets 19 in the test tray TST. It is to be appreciated that where thirty-two IC sockets are mounted on the test head 104, only two testing runs are required to examine all
15 sixty-four ICs arranged in an array of 4 rows x 16 columns.

The IC storage section 200 comprises an IC-to-be-tested storage rack or stocker 201 for accommodating universal trays KST loaded with ICs to be tested and a tested IC storage rack or stocker 202 for accommodating universal trays KST loaded with tested ICs sorted
20 out by categories on the basis of the test results. The IC-to-be-tested storage rack 201 and the tested IC storage rack 202 are configured to accommodate universal trays in the form of a stack. The universal trays KST with ICs to be tested thereon stored in the form of a stack in the IC-to-be-tested storage rack 201 are
25 transported successively from the top of the stack to the loader section 300 where the ICs to be tested are transferred from the universal tray KST onto the test tray TST on standby in the loader

section 300.

The IC-to-be-tested storage rack 201 and the tested IC storage rack 202, one of which is shown in Fig. 10, may be of identical construction and comprise a tray supporting frame 203 open at the top and having an opening at the bottom, and an elevator 204 disposed below the frame 203 so as to be vertically movable through the bottom opening. In the tray supporting frame 203 there are stored and supported a plurality of universal trays KST stacked one on another which are vertically moved by the elevator 204 acting through the bottom opening of the frame 203.

In the example illustrated in Figs. 4 and 5, eight racks STK-1, STK-2, . . . , STK-8 are provided as tested IC storage racks 202 so as to be able to store tested ICs which may be sorted out into eight categories at a maximum according to the test results. This is because in some applications tested ICs may not only be classified into categories of "conforming article" and "non-conforming article" but also be subclassified into those having high, medium and low operation speeds among the "conforming" articles and those required to be re-tested among the "non-conforming" articles, and others. Even if the number of classifiable categories is up to eight, the unloader section 400 in the illustrated example is capable of accommodating only four universal trays KST. For this reason, if there occur some among the tested ICs which should be classified into a category other than categories assigned to the four universal trays KST arranged in the unloader section 400, the procedures taken are to return one of the universal trays KST from the unloader section 400 to the tested IC storage section 200 and in replacement

transfer a universal tray KST for storing the ICs belonging to the new additional category from the tested IC storage section 200 to the unloader section 400 where those ICs are stored in the new tray.

Referring to Fig. 5, a tray transport 205 is disposed above the
5 IC-to-be-tested storage rack 201 and the tested IC storage racks 202 and below the base plate 105 for movement over the entire extent of the storage racks 201 and 202 in the direction of arrangement of the racks (in the right to left direction of the testing apparatus). The tray transport 205 is provided on its bottom surface with a grasping
10 device (not shown) for grasping a universal tray KST. The tray transport 205 is moved to a position over the tray supporting frame 203 of the IC-to-be-tested storage rack 201 whereupon the elevator 204 is actuated to lift the universal trays KST stacked in the tray supporting frame 203, so that the uppermost universal tray KST
15 may be engaged and grasped by the grasping device of the tray transport 205.

Once the uppermost universal tray KST loaded with ICs being tested has been transferred to the tray transport 205, the elevator 204 is lowered to its original position. At the same time, the tray
20 transport 205 is horizontally moved along a guide (not shown) to and stopped at a predetermined position in the loader section 300 by means of a driving device such as chains or wires where the tray transport 205 has its grasping device release the universal tray KST to unload it onto an immediately underlying tray receiver (not
25 shown). The tray transport 205 having the universal tray KST unloaded therefrom is again moved horizontally along the guide by the driving device and stopped at a position away from the loader

section 300.

In this condition, the elevator 204 is moved upward from below the tray receiver to lift up the universal tray KST loaded with ICs to be tested so that the universal tray KST is held with its upper
5 surface facing a window 106 formed in the base plate 105 (with the upper surface of the universal tray KST exposed through the window). More specifically, a grasping device (not shown) for grasping a universal tray KST is mounted on the undersurface of the base plate 105 around the window 106, so that the universal tray
10 KST is held in the aforesaid condition by the grasping device engaging with the universal trays KST loaded with ICs to be tested. In this condition, the ICs to be tested are loaded from the universal tray KST through the window 106 onto the test tray TST.

The base plate 105 is also formed in the area overlying the
15 unloader section 400 with similar windows 106. In this example, each of the windows 106 is sized to allow the upper surfaces of two universal trays to face the window. Hence, the arrangement is such that tested ICs may be stored through the two windows 106 of the unloader section 400 into four empty universal trays. Grasping
20 devices (not shown) for grasping universal trays KST are also mounted on the undersurface of the base plate 105 around the windows 106 of the unloader section 400, so that universal trays KST may be grasped by the grasping devices. Tested ICs are sorted and stored in these empty universal trays KST according to the
25 categories assigned to the respective trays.

Although not shown, as with the loader section 300, the unloader section 400 is also provided with tray receivers and

associated elevators for temporarily keeping (supporting thereon) universal trays KST. Once one universal tray KST has been fully filled, the associated elevator is moved up to support the tray whereupon the tray is released from the engagement with the grasping device. Then, as the elevator is moved down, the universal tray KST is lowered from the level below the window 116 to be temporarily placed on the tray receiver, and is subsequently stored in the tray storage position assigned to that particular tray by the tray transport 205.

10 Indicated by the numeral 206 in Figs. 4 and 5 is an empty tray storage rack for accommodating empty universal trays KST. From this empty tray storage rack 206, empty universal trays are transported to the respective windows 106 by the tray transport 205 and held thereat by the associated elevators 204 to be ready for receiving tested ICs.

15 Next, the general construction of the handler used with the prior art IC tester for testing logic ICs will be described with reference to Fig. 11.

20 Fig. 11 is a schematic plan view illustrating the general arrangement of the conventional handler for use in transporting and handling logic ICs. This handler comprises a base 111, a feeding tray 116 located on the base 111 on the upper left side portion thereof as viewed in the drawing and having ICs 115 under test placed thereon, a receiving tray 117 located on the base 111 below the feeding tray 116 for receiving tested ICs 117 thereon, and an X-Y transport 130 adapted to transfer ICs 115 to be tested from the feeding tray 116 to a test head 112 for testing logic ICs and to

transfer tested ICs from this test head 112 for testing logic ICs to the receiving tray 117.

The test head 112 for testing logic ICs is mounted on the base 111 on the center right portion thereof as viewed in the drawing and is electrically connected with the main frame 113 of the logic IC testing apparatus by cables 114. The test head 112 is equipped with one socket in this example. An IC 115 to be tested is electrically connected with the contacts of the socket through which a test signal of a predetermined pattern is supplied to the IC 115 under test for testing the logic sections of the ICs under test.

The X-Y transport 130 comprises a pair of opposed parallel rails 131 mounted on the base 111 and extending along the upper and lower lateral edges of the base 111 in the left to right direction (referred to as X direction herein), a movable arm 132 spanning and movably mounted at opposite ends on the pair of rails 131, and a movable head 133 mounted on the movable arm 132 for movement therealong in the forward-rearward direction of the base 111 (referred to as Y direction herein). With this construction, the movable head 133 is reciprocally movable in the X direction with movement of the movable arm 132 in the X direction as well as being movable in the Y direction along the movable arm 132.

The movable head 133 has an IC grasping head 134 vertically movably mounted on its bottom surface. The IC grasping head 134 in this example is a vacuum pick-up head for attracting and grasping ICs by vacuum suction and is configured to be moved downwardly by the driving power of a drive source such as an air cylinder and to be moved back to its original position by a normally upwardly

biasing member when the drive source is deactivated to remove the driving power.

The movement of the movable head 133 in the X and Y directions and the downward movement of the IC grasping head 134 bring the grasping head 134 into abutment with the IC 115 to be tested placed on the feeding tray 116 to attract and grasp it by vacuum suction for transfer from the feeding tray 116 to the test head 112. Upon completion of the test by the test head 112, the grasping head 134 picks up and grasp the tested IC from the test head 112 and transport it to the receiving tray 117. The illustrated example shows the case in which the movable head 133 is provided with a single vacuum pick-up head 134 so that one IC at a time may be suction attracted and held for transporting.

The receiving tray 117 is provided with a storage device (memory) for each of the IC holding compartments on the tray so that the results of decision on the quality (conforming/non-conforming) of tested ICs accommodated in corresponding compartments may be stored in the corresponding storage devices, respectively.

In the case of testing composite ICs containing memory sections and logic sections, assuming that the testing sequence is to test the logic sections following the testing of memory sections, only those of the ICs that have been determined as conforming articles through the testing of the memory sections will be subjected to testing of the logic sections. Consequently, ICs placed on the feeding tray 116 of the handler for use in transporting and handling logic ICs are those of equal quality which have been determined as conforming articles through the testing of the memory sections and which have been

classified as belonging to ones having high, medium and low operation speeds, for example. In other words, it is ICs uniform in quality that are stored in the feeding tray 116.

When transferring ICs from the memory IC tester to the logic IC
5 tester, generally the operator transmits the test results obtained in the memory IC tester to the logic IC tester by utilizing a storage medium such as a floppy disk whereby the logic IC tester is informed of the qualities (the test results of the memory sections) of the ICs on the feeding tray 116. It will be thus appreciated that the
10 results of testing of the logic sections which will be effected from now as well as the transmitted test results of the memory sections will be stored as the ultimate results of decision on the qualities of the composite ICs.

Since the IC tester for memory ICs and the IC tester for logic ICs
15 use the handlers of entirely different construction or structure as indicated hereinbefore, in the case of testing composite ICs containing memory sections and logic sections, it has been required for the operator to operate separately the handler for use with memory ICs as described with reference to Figs. 4 to 10 and the
20 handler for use with logic ICs as described with reference to Fig. 11 and to carry the composite ICs already tested for either their memory sections or their logic sections from one handler having finished with the testing to the other handler which will now proceed with the testing and load the ICs on an appropriate tray
25 associated with the latter handler.

Such operations not only requires much human effort but also disadvantageously prevents the automation of the IC tester. In

addition, notwithstanding the fact that the test results are stored according to the order of delivery of trays delivered out of one of the IC testers, an accidental change in the order of delivery of trays as occasioned by intermediation of human operations would lead to an inconsistency between the test results transmitted to the succeeding IC tester and the order of delivery of trays, resulting in the inconvenience of consequentially causing erroneous sorting of the tested ICs.

10 SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor integrated circuit testing apparatus which is capable of automatically testing the memory sections and logic sections successively of composite ICs.

15 In order to accomplish the aforesaid object, the present invention provides a semiconductor integrated circuit testing apparatus in which a test tray is moved in a circulating manner along a predetermined path of movement so as to test ICs to be tested placed on the test tray by a test head disposed in the path of movement of the test tray, the testing apparatus being characterized in that: a memory testing test head and a logic testing test head are disposed in the path of movement of the test tray, and ICs to be tested placed on one test tray, each having a memory section and a logic section, are tested by the respective test heads while the ICs are placed on the one same test tray.

In a preferred embodiment, the ICs to be tested placed on one test tray have their memory sections first tested by the memory

testing test head, followed by having their logic sections tested by said logic testing test head. In addition, an X-Y moving mechanism for moving and indexing one test tray by predetermined increments in X and Y directions and Z-axis drive means for moving one test
5 tray vertically may be provided, and the ICs to be tested placed on one test tray are successively brought into contact with a testing socket of the logic testing test head by the X-Y moving mechanism and the Z-axis drive means while the ICs are placed on the one same test tray.

10 Moreover, only those of the ICs to be tested, which have been determined as non-defective in respect of their memory sections as a result of testing by the memory testing test head, have their logic sections further tested by the logic testing test head, whereby the testing time may be substantially reduced.

15 With the construction as described above, it is possible to automatically test the memory sections of the ICs and the logic sections successively while remaining loaded on the same test tray TST, thereby eliminating the need for the human operations of transshipping ICs from one handler to the other handler to reload
20 the ICs on the corresponding tray between the testing of the memory sections and the testing of the logic sections so that the testing may be carried out in a reduced time. In addition, the present invention provides the advantage of enabling both the testing of the memory sections and the testing of the logic sections
25 without the need for human operations to thereby provide for constructing a highly reliable composite testing system.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic plan view illustrating the general construction of a handler used with one embodiment of the IC testing apparatus according to the present invention, with the chamber section shown in a perspective-like view;

Fig. 2 is a side view illustrating the configuration of the X-Y moving mechanism used with the handler of the IC testing apparatus shown in Fig. 1;

Fig. 3 is a plan view of the drawing of Fig. 2;

Fig. 4 is a schematic plan view illustrating one example of the handler for use with the conventional memory IC testing apparatus, with the chamber section shown in a perspective-like view;

Fig. 5 is a schematic perspective view of the handler shown in Fig. 4;

Fig. 6 is an exploded perspective view illustrating an example of the test tray for use with the handler shown in Figs. 4 and 5;

Fig. 7 is a plan view illustrating the construction of the IC carrier useful with the test tray shown in Fig. 6;

Fig. 8 is a cross-sectional view taken along the line 8-8 in Fig. 7 and seen in the direction indicated by the arrows;

Fig. 9 is a plan view illustrating the sequence in which ICs under test stored in the test tray shown in Fig. 6 are subjected to testing;

Fig. 10 is a perspective view illustrating the construction of a IC-to-be-tested storage rack or a tested IC storage rack for use with the handler shown in Figs. 4 and 5; and

Fig. 11 is a plan view illustrating the general construction of one example of the handler for use with the conventional logic IC testing

apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One embodiment of the present invention will be described in
5 details with reference to Figs. 1-3.

Fig. 1 is a schematic plan view illustrating the general
construction of a handler used with one embodiment of the IC
testing apparatus according to the present invention. This handler,
like the conventional handler shown in Figs. 4 and 5, comprises a
10 chamber section 100 for testing ICs) which have been brought in as
loaded on a test tray TST, an IC storage section 200 for storing ICs to
be tested (ICs under test) and ICs already tested and sorted, a loader
section 300 where ICs being tested which a user has beforehand
loaded on universal trays (customer trays) KST are transferred and
15 reloaded onto test trays TST capable of withstanding high/low
temperatures, and an unloader section 400 where the tested ICs
which have been carried on the test trays TST out of the chamber
section 100 subsequently to undergoing a test therein are
transferred from the test trays TST to the universal trays KST to be
20 reloaded on the latter.

The chamber section 100 comprises a constant temperature
chamber 101 for imposing thermal stresses of either a designed high
or low temperature on ICs under test loaded on a test tray TST, a
test chamber 102 for conducting electrical tests on the ICs under the
25 thermal stress imposed in the constant temperature chamber 101,
and a heat-removal/cold-removal chamber 103 for removing the
thermal stress imposed in the constant temperature chamber 101

from the ICs having undergone the tests in the test chamber 102.
The test tray TST is moved in a circulating manner from and back to
the loader section 300 sequentially through the constant
temperature chamber 101 of the chamber section 100, the test
5 chamber 102 of the chamber section 100 and the heat-removal
/cold-removal chamber 103 of the chamber section 100, and the
unloader section 400. In Fig. 1, those parts and elements
corresponding to the parts and elements shown in Figs. 4 and 5 are
designated by like reference numbers, and will not be further
10 described unless necessary.

In an IC testing apparatus configured such that a test tray TST
is moved in a circulating manner along a predetermined path of
movement as set forth above to bring an IC under test placed on the
test tray TST while remaining thereon into electrical contact with a
15 socket on a test head of the IC testing apparatus to subject the IC
under test to testing, according to the present invention, a test head
104A for testing memory sections and a test head 104B for testing
logic sections are disposed in the path or route of movement of the
test tray TST, the arrangement being such that both the memory
20 sections and the logic sections of the IC (composite IC) under test are
subjected to testing while the IC is placed on the same test tray TST.

In the embodiment shown in Fig. 1, the memory testing test
head 104A and the logic testing test head 104B are disposed in the
interior of the test chamber 102 for conducting tests on ICs under
25 test while maintaining the temperature of the ICs loaded with a
predetermined thermal stress in the constant temperature chamber
101 at a predetermined level. Specifically, the memory testing test

head 104A and the logic testing test head 104B are located in the test chamber 102 toward the entrance and the exit, respectively thereof. It will thus be appreciated that they are positioned such that the test tray in its path of movement first arrives at the
5 memory testing test head 104A and then is routed to the logic testing test head 104B.

By way of example, where ICs under test are placed in an array of 4 rows $\times$ 16 columns on a test tray TST, 4×4 , that is, 16 IC sockets are arranged and mounted on the memory testing test head
10 104A so that the ICs (shown as cross-hatched in Fig. 9) in every fourth column in each of the rows may be tested all at once. More specifically, as already explained with reference to Fig. 9, in the first testing run the examination is conducted on sixteen ICs located in the first, fifth, ninth and thirteenth columns in each row, the second
15 testing run is effected on another sixteen ICs located in the second, sixth, tenth and fourteenth columns in each row by shifting the test tray TST by a distance corresponding to one column of ICs, and the third and fourth testing runs are carried out in the similar manner until all of the ICs are tested.

20 The test results are stored in the addresses of a storage device (memory) determined by the identification number affixed to the particular test tray TST and the numbers assigned to the IC-placed locations in the test tray TST. It will be evident that if thirty-two IC sockets are mounted on the memory testing test head 104A, only
25 two testing runs are required to examine all sixty-four ICs arranged in an array of 4 rows $\times$ 16 columns.

Stored in the storage device are, not to mention the data of

qualities (non-defective/defective) of the memory sections of the tested ICs, the quality data and other data concerning ones having the high, medium and low operation speeds among the "conforming" articles and ones required to be re-tested among the "non-conforming" articles.

The test tray TST having gone through the testing by the memory testing test head 104A is then passed to the location of the logic testing test head 104B. Mounted over the location of the logic testing test head 104B is an X-Y moving mechanism 140 for receiving the incoming test tray TST and indexing it by predetermined increments (pitch) in X and Y directions (bi-axial directions in a horizontal plane).

Figs. 2 and 3 are side and plan views, respectively, illustrating the construction of the X-Y moving mechanism 140 used with the handler shown in Fig. 1. The X-Y moving mechanism may comprise opposed X-axis screw shaft 141 and X-axis guide shaft 142 extending parallel to the direction of movement of the test tray TST (which is referred to as X direction) along the opposite sides of the logic testing test head 104B, two spaced apart X-axis ball screws 143 threaded on the X-axis screw shaft 141, two X-axis sliders 144 slidably engaged on the X-axis guide shaft 142, two Y-axis rails 145 spanning between the X-axis screw shaft 141 and X-axis guide shaft 142 and extending in the Y direction perpendicular to the X direction, each of the rails secured at one end to one of the X-axis ball screws 143 and at the other end to the corresponding one of the X-axis sliders 144, a Y-axis screw shaft 146 extending along one of the Y-axis rails 145, Y-axis guide shaft 146 extending along the

other Y-axis rails 145, two spaced apart Y-axis ball screws 148 threaded on the Y-axis screw shaft 146, two Y-axis sliders 149 slidably engaged on the Y-axis guide shaft 147, Z-axis drive units 150 one mounted on each of the Y-axis ball screws 148 and the Y-axis sliders 149, and a support frame 151 suspended from the four Z-axis drive units 150 so as to be moved in the Z-axis direction (vertically) by the drive units 150.

As is best shown in Fig. 3, the rectangular support frame 151 is supported at two points spaced apart a predetermined distance along each of the opposed X-direction sides thereof by the Z-axis drive units 150. In this example, the Z-axis drive units 150 each comprise an air cylinder mounted to the corresponding Y-axis ball screw 148 or Y-axis slider 149 in a downwardly facing orientation. The outer ends of the piston rods of these air cylinders are attached to the respective X-direction sides of the support frame 151 such that the support frame 151 is moved in the Z-axis direction by simultaneous actuation of the four Z-axis drive units 150.

An X-axis drive pulse motor 154 rotatively drives the X-axis screw shaft 141 the rotation of which in turn moves the two X-axis ball screws 143 together reciprocally in the X direction. The reciprocal movement of the two X-axis ball screws 143 in the X direction causes the simultaneous reciprocal movement of the two Y-axis rails 145 in the X direction. Similarly, a Y-axis drive pulse motor 155 rotatively drives the Y-axis screw shaft 146 the rotation of which in turn moves the two Y-axis ball screws 146 together reciprocally in the Y direction. The reciprocal movement of the two Y-axis ball screws 148 in the Y direction directly causes the

simultaneous reciprocal movement of the two Z-axis drive units 150 mounted to the Y-axis ball screws 148 and also causes, through the support frame 151, the simultaneous reciprocal movement of the other two Z-axis drive units 150 mounted to the Y-axis sliders 149 in the Y direction.

It is to thus be appreciated that activation of the X-axis drive pulse motor 154 and the Y-axis drive pulse motor 155 causes movement of the support frame 151 in the X and Y directions and that simultaneous activation of the four Z-axis drive units 150 causes movement of the support frame 151 in the Z direction.

Since the support frame 151 is designed to receive the incoming test tray TST and carry it thereon as such, the spacing between the two Y-axis ball screws 148 (specifically the spacing between the two Z-axis drive units 150 mounted to these Y-axis ball screws 148) must be greater than the width (the dimension in the Y direction) of the test tray TST. Likewise, the spacing between the X-axis screw shaft 141 and the X-axis guide shaft 142 must be greater than the width of the test tray TST.

The test tray TST loaded with composite ICs after finishing with the testing for the memory sections is delivered in the X direction by a transport composed of rollers 152 to a position overlying the support frame 151 which is at this point of time supported at the lower limit position (bottom dead center) of the stroke of the Z-axis drive units 150 shown in Fig. 2. Upon the test tray TST being placed on the support frame 151, the Z-axis drive units 150 are activated to lift the support frame 151 with the test tray TST placed thereon up usually to the upper limit position of the stroke of the Z-axis drive

units 150. Alternatively, the arrangement may be such that when the drive source for the Z-axis drive units 150 is turned off, the piston rods of the Z-axis drive units 150 are moved up to the upper limit position of the stroke by biasing means for normally biasing the piston rods to the upper limit position. Thereafter, the support frame 151 and the test tray TST are conveyed to a predetermined position overlying the logic testing test head 104B by the X-Y moving mechanism 140.

The logic testing test head 104B has two, in this example, testing sockets 153 mounted thereon. ICs placed on the test tray TST are successively two by two brought into the two testing sockets 153 to carry out the testing for the logic sections. It is to be noted that the testing for the logic sections is conducted on only those ICs which have been determined as non-defective in the testing for the memory sections while the logic section testing is omitted for the defective ICs, whereby the testing time is reduced to enhance the testing efficiency.

Since the operations of moving the support frame 151 and the test tray TST placed thereon in the X and Y directions by activation of the X-axis drive pulse motor 154 and putting the ICs placed on the test tray TST successively two by two brought into the two testing sockets 153 on the logic testing test head 104B by activation of the Z-axis drive units 150 are obvious to those skilled in the art, the detailed description thereof is omitted herein.

Once the testing for the logic sections have been completed on those ICs which have been determined as non-defective in the testing for the memory sections, the test tray TST is removed from

the support frame 151 and delivered to the heat-removal/cold-removal chamber 103 shown in Fig. 1 where the tested ICs are relieved of heat or cold to be restored to the room temperature prior to being passed to the unloader section 400. The tested ICs on the test tray TST delivered to the unloader section 400 are sorted out by categories based on the test results and transferred from the test tray TST onto and stored in the corresponding universal trays KST. The test tray TST emptied in the unloader section 400 is delivered back to the loader section 300 where it is again loaded with ICs to be tested from the universal tray KST to repeat the same steps of operation.

In the illustrated handler, eight storage racks STK-1, STK-2, . . . , STK-8 as tested IC storage racks 202 so that tested ICs may be classified into a maximum of 8 storage racks and stored in the corresponding storage racks. This is because it may be desired not only to sort tested ICs into conforming articles and non-conforming articles but also to subclassify them into those having high, medium and low operation speeds among the conforming articles and those required to be re-tested among the non-conforming articles, and others. Even if the sortable categories are eight at maximum, the number of universal trays KST which can be disposed in the unloader section 400 is limited to four in the illustrated example. For this reason, if there occur some tested ICs which are to be sorted into categories other than the categories assigned to the universal trays KST disposed in the unloader section 400, the procedures taken are to return one of the universal trays KST from the unloader section 400 to the IC storage section 200 and in replacement

transfer a universal tray KST for storing the IC belonging to the newly occurring category from the IC storage section 200 the unloader section 400 for storage of the IC.

As discussed hereinabove, according to the present invention, once ICs have been loaded on a test tray TST in the loader section, it is possible to automatically test the memory sections and logic sections successively of the ICs while remaining loaded on that test tray TST, thereby eliminating the need for the human operations of transshipping ICs between the testing of the memory sections and the testing of the logic sections. It will thus be appreciated that the present invention provides the marked advantage of enabling both the testing of the memory sections and the testing of the logic sections in a short time.

In addition, the complete elimination of the need for human operations eliminates possible occurrence of an accidental change in the order of delivery of trays from one of the IC testers. It is thus to be understood that the present invention provides for constructing a highly reliable IC tester.

While the present invention has been described in the illustrated embodiment with reference to the case where the invention is applied to the handler of the construction in which the test tray is circulated in a three-dimensional path, it will readily be appreciated that the present invention is also applicable with equal functional effects to the handler of the type as shown in Fig. 11 in which the test tray is circulated in a planar path.



WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit testing apparatus in which a test tray is moved in a circulating manner along a predetermined path of movement so as to test ICs to be tested placed on the test tray by a test head disposed in the path of movement of the test tray, said testing apparatus being characterized in that:

a memory testing test head and a logic testing test head are disposed in the path of movement of the test tray, and ICs to be tested placed on one test tray, each having a memory section and a logic section, are tested by said respective test heads while the ICs are placed on said one same test tray.

2. The semiconductor integrated circuit testing apparatus according to claim 1, wherein the ICs to be tested placed on one test tray have their memory sections first tested by said memory testing test head, followed by having their logic sections tested by said logic testing test head.

3. The semiconductor integrated circuit testing apparatus according to claim 1 or 2, further including an X-Y moving mechanism for moving and indexing one test tray by predetermined increments in X and Y directions, and wherein the ICs to be tested placed on one test tray are successively brought into contact with a testing socket of said logic testing test head by said X-Y moving mechanism while the ICs are placed on said one same test tray.



4. The semiconductor integrated circuit testing apparatus according to claim 2, wherein only those of the ICs to be tested, which have been determined as non-defective in respect of their memory sections as a result of testing by said memory testing test head, have their logic sections further tested by said logic testing test head.

5. The semiconductor integrated circuit testing apparatus according to claim 3, wherein said X-Y moving mechanism have mounted thereon Z-axis drive means for moving one test tray vertically so as to successively bring the ICs to be tested placed on one test tray into contact with the testing socket of said logic testing test head while the ICs are placed on said one same test tray.

6. A semiconductor integrated circuit testing apparatus in which a test tray is moved in a circulating manner along a predetermined path of movement so as to test ICs to be tested placed on a test tray by a test head disposed in the path of movement of the test tray while the ICs are placed on said one same test tray and the test results are managed according to addresses determined by identification number affixed to the test tray and the numbers assigned to the IC-placed locations in the test tray, said testing apparatus being characterized in that:

a memory testing test head and a logic testing test head are disposed in the path of movement of the test tray, and ICs to be tested placed on one test tray, each having a memory section and a



logic section, are tested by said respective test heads while the ICs are placed on said one same test tray.

7. The semiconductor integrated circuit testing apparatus according to claim 6, wherein the ICs to be tested placed on one test tray have their memory sections first tested by said memory testing test head, followed by having their logic sections tested by said logic testing test head.

8. The semiconductor integrated circuit testing apparatus according to claim 6 or 7, further including an X-Y moving mechanism for moving and indexing one test tray by predetermined increments in X and Y directions provided at a predetermined position over said logic testing test head, and wherein the ICs to be tested placed on one test tray are successively brought into contact with a testing socket of said logic testing test head by said X-Y moving mechanism while the ICs are placed on said one same test tray.

9. The semiconductor integrated circuit testing apparatus according to claim 7, wherein only those of the ICs to be tested, which have been determined as non-defective in respect of their memory sections as a result of testing by said memory testing test head, have their logic sections further tested by said logic testing test head.

10. The semiconductor integrated circuit testing apparatus



according to claim 8, wherein said X-Y moving mechanism have mounted thereon Z-axis drive means for moving one test tray vertically so as to successively bring the ICs to be tested placed on one test tray into contact with the testing socket of said logic testing test head while the ICs are placed on said one same test tray.