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"CONVERTER".

The present invention relates to a converter which is constructed of a plurality of insulated-gate field effect transistors (hereinafter referred to as "FETs") formed in a semiconductor integrated circuit device, and more particularly to a converter
5 which is used as a digital-to-analog converter (hereinafter referred to as a "DAC") or an analog-to-digital converter (hereinafter referred to as a "ADC").

A converter which employs FETs as voltage
10 switching elements is known from the disclosure in Japanese laid-open patent publication No. 28851/77.

In this known converter, a plurality of P-channel type FETs (hereinafter referred to as "P-type FETs") formed on a single semiconductor substrate
15 are connected in the shape of a fir-tree between a plurality of input points and one output point and are controlled "on" and "off" by a digital signal having a plurality of bits.

By means of the switching control of the

plurality of P-type FETs, one of the plurality of input points which corresponds to the state of the digital signal is coupled to the output point. The respective input points are supplied with voltages of levels
4 different from one another from a resistive voltage divider which divides a reference voltage. Therefore, a voltage of a level corresponding to the state of the digital signal is provided at the output point.

10 However, the level of the voltage to be delivered to the output point is limited as will be explained below.

A FET must have its gate potential raised greater than its threshold voltage (hereinafter, referred to as " V_{th} ") with respect to its source potential
15 in order to bring it into the "on" state. Accordingly, in the case where P-type FETs are used in the converter described above, the upper limit of the selectable voltages is restricted by the V_{th} as well as the level of the digital signal to be applied to the gate of the
20 P-type FET.

The respective P-type FETs formed on the single semiconductor substrate as described above have a bias voltage (hereinafter referred to as "back gate bias voltage") applied from the semiconductor substrate
25 which serves as a common substrate gate. As a result, the V_{th} of each P-type FET has its level increased by the known substrate effect.

In such a case where the semiconductor

substrate is maintained at earth potential, the back gate bias voltage is formed of the potentials of the source, drain and channel of the P-type FET. Therefore, the P-type FET for switching a voltage of a high level in absolute value receives a back gate bias voltage of a high level corresponding thereto and accordingly has its V_{th} made high. Usually, a FET of large V_{th} exhibits a comparatively large drain - source resistance under a constant gate bias voltage.

Thus, the voltage which can be delivered to the output point has its level limited, not only by the V_{th} of the FET and the digital signal level as stated previously, but also by the attenuation induced by the increased drain - source resistance of the FET. In other words, it is difficult with such a converter to deliver a voltage of a desirable level corresponding to the digital signal.

In order to eliminate the limitations to the output voltage level as described above, the digital signal level for controlling the plurality of P-type FETs "on" and "off" can be increased by employing, for example, a voltage booster circuit. This necessitates additional circuit elements in order to construct the voltage booster circuit.

It is an object of the present invention to provide a converter which will deliver a large voltage signal even when the level of a digital signal is comparatively low.

According to the present invention there is provided a converter including:

a voltage selector which comprises a plurality of input points supplied with voltages all having different levels from one another, a single common output point, and a plurality of insulated-gate field effect transistors with their source - drain paths connected between said plurality of input points and said common output point, each of said plurality of insulated-gate field effect transistors having a conductivity type which is determined so that each transistor can be brought into the "on" state by a level of a binary signal which affords a greater level difference relative to the voltage to be switched by each transistor; and

a driving circuit which provides binary signals of a plurality of bits for controlling the "on" and "off" states of said plurality of insulated-gate field effect transistors.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a circuit diagram of one preferred form of a converter;

Figure 2 is a sectional view of a semiconductor substrate on which a P-type FET and an N-type FET are formed;

Figure 3 is a block diagram of a digital-to-

analog converter embodying the converter shown in Figure 1;

Figure 4 is a block diagram of an analog-to-digital converter embodying the converter shown in Figure 1;

5 Figure 5 is a logic circuit diagram showing the control circuit 28 of Figure 4 in greater detail;

Figure 6 is a block diagram of an electronic sound generator to which a converter of the present invention can be applied;

10 Figure 7A is a graph showing the characteristic curve of the circuit 60 in Figure 6, whilst Figure 7B is an equivalent circuit diagram of the circuit 60.

15 Figures 8, 9 and 10 are waveform diagrams showing the waveforms of signal voltages supplied to DACs and output voltages provided therefrom.

The converter shown in Figure 1, includes a reference voltage circuit 1; a voltage selector 2; and a driving circuit 3. The reference voltage circuit 1 receives a reference voltage (hereinafter referred to as " $-V_s$ ") supplied to a terminal $-V_s$, in order to deliver voltages of levels different from one another to its output points V_1 to V_8 . The reference voltage circuit 1 is constructed as a voltage divider and comprises eight resistors R_1 to R_8 connected in series. The resistors R_1 to R_8 have values of resistance which are equal to one another. The reference voltage $-V_s$ has a value of -3 volts. Accordingly, a voltage drop

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of $-3/8$ volt develops across each of the resistors R_1 to R_8 , and the voltages (hereinafter, written " V_1 ", " V_2 " etc.) to be delivered to the output points V_1 to V_8 are correspondingly determined. By way of example, the voltage V_5 becomes
5 $-3/2$ volts, i.e. -1.5 volts.

The voltage selector 2 has input points N_1 to N_8 respectively coupled to the output points V_1 to V_8 of the reference voltage circuit 1, a common output point N_0 , and control input points C_1 to C_5 .

10 The control input point C_1 is supplied with a binary signal $\bar{a}$ from the driving circuit 3. The control input point C_2 is supplied with a binary signal $\bar{b}$, and the control input point C_3 is supplied with a binary signal b complementary to the binary signal $\bar{b}$. Likewise, the control input
15 points C_4 and C_5 are respectively supplied with binary signals $\bar{c}$ and c .

The voltage selector 2 includes P-type FETs T_1 to T_7 and N-type FETs Q_1 to Q_7 which are connected in the configuration of a fir-tree between the input points N_1 to N_8 and
20 the common output point N_0 . By "fir-tree" configuration, we mean that the number of FETs in each subsequent stage of the voltage selector 2 reduces by a factor of 2.

The respective FETs to be coupled to branches B_1 to B_7 in the fir-tree configuration have their channel conductivity types determined so as to be turned "on" by binary
25 signal levels which afford difference voltages greater in the absolute value than voltages V_N to be thereby switched. The earth level of the binary signals which are delivered from the driving circuit 3 is denoted by V_0 , and the supply

voltage level by V_s .

In this embodiment, the level of the binary signal which is delivered from the driving circuit 3 is made either the reference voltage $-V_s$ having a negative potential (logic value "1") or the earth potential (logic value "0") as will be apparent from later description.

In contrast, the voltage V_5 amongst the voltages which are delivered from the reference voltage circuit 1 is equal to half of $-V_s$. As a result, the voltages V_6 , V_7 and V_8 are all negative with respect to the voltage V_5 , and the voltages V_4 , V_3 , V_2 and V_1 are all positive with respect to the voltage V_5 .

Accordingly, the level difference between each of the output voltages V_1 to V_4 of the reference voltage circuit 1 and the "1" level (reference voltage $-V_s$) of the binary signal becomes greater in the absolute value than the level difference between each of the output voltages V_1 to V_4 and the "0" level (earth) of the binary signal. Likewise, the level difference between each of the output voltages V_6 to V_8 of the reference voltage circuit 1 and the "0" level of the binary signal is greater than the level difference between each of the voltages V_6 to V_8 and the "1" level of the binary signal.

Regarding the voltage V_5 , the level differences are equal for both the "1" level (reference voltage $-V_s$) and the "0" level (earth) of the binary

signal.

Accordingly, the FETs T_1 to T_4 for coupling the input points N_1 to N_4 to branches B_6 and B_7 are of the P-channel type. The FETs T_5 and T_6 for coupling the branches B_6 and B_7 to the branch B_3 and the FET T_7 for coupling the branch B_3 to the branch B_1 are similarly of the P-channel type.

Likewise, the FETs Q_1 to Q_3 for coupling the input points N_6 to N_8 to the branches B_4 and B_5 , the FETs Q_5 and Q_6 for coupling the branches B_4 and B_5 to the branch B_2 and the FET Q_7 for coupling the branch B_2 to the branch B_1 are of the N-channel type.

In this embodiment, the FET Q_4 for coupling the input point N_5 to the branch B_5 may be either of the N-channel type or of the P-channel type because the voltage supplied to the input point N_5 has the level of $V_s/2$. In the embodiment shown it is of the N-channel type.

In the voltage selector 2, the FETs Q_7 and T_7 coupled to the branch B_1 of the fir-tree have their gate electrodes coupled to the input point C_1 so as to be complementarily controlled "on" and "off". The FETs Q_5 and Q_6 coupled to the branch B_2 have their gate electrodes respectively coupled to the input points C_2 and C_3 so as to be complementarily controlled "on" and "off" in similar manner. Also the FETs T_6 and T_5 coupled to the branch B_3 have their gate electrodes respectively coupled to the input points C_2 and C_3 .

Likewise, the FETs coupled to the respective branches B_4 to B_7 have their gate electrodes coupled to the appropriate control input points C_4 or C_5 so as to be complementarily controlled "on" and "off" as shown according to circuit connections.

Although not shown, the substrate gate electrodes of the respective P-type FETs T_1 to T_7 are coupled to earth and those of the respective N-type FETs Q_1 to Q_7 are coupled to the terminal $-V_s$.

The driving circuit 3 provides the binary signals $\bar{a}$, $\bar{b}$, $\bar{c}$ and c for driving the voltage selector 2, from 3-bit binary signals A to C supplied thereto. The binary signal A is made the binary signal of the most significant bit amongst the 3-bit binary signals, and the binary signal C the binary signal of the least significant bit.

The driving circuit 3 includes complementary type inverters IN_1 to IN_5 each of which comprises a P-type FET T_8 and an N-type FET Q_8 and complementary type inverters IN_6 and IN_7 . The driving circuit 3 is supplied with the voltage $-V_s$ as its supply voltage. The complementary type inverters IN_6 and IN_7 are constructed in similar manner to the inverters IN_1 to IN_5 .

The operation of the circuit arrangement shown in Figure 1 is such that one of the input points N_1 to N_8 of the voltage selector 2, which is determined by the combination of the 3-bit binary signals A to C, is

coupled to the output point N_0 . In other words, a voltage which is determined by the combination of the 3-bit binary signals A to C is supplied to the output point N_0 .

5 More specifically, when the 3-bit binary signals A, B and C applied to the driving circuit 3 are "0", "0" and "0", the driving circuit 3 provides in response thereto the binary signals $\bar{a}$, $\bar{b}$ and $\bar{c}$ respectively being "1" (reference voltage $-V_g$) and the
10 binary signals b and c respectively being "0" (earth). In response to these binary signals, the P-type FETs T_4 , T_6 and T_7 in the voltage selector 2 are switched to the "on" state. As a result, the voltage V_1 of the input point N_1 is supplied to the common output point N_0
15 through the FETs T_4 , T_6 and T_7 . The voltage at the output point N_0 is output from the voltage selector through a lead 26.

When the 3-bit binary signals A, B and C are "1", "1" and "1", the driving circuit 3 responds
20 thereto to provide the binary signals $\bar{a}$, $\bar{b}$ and $\bar{c}$ respectively being "0" and the binary signals b and c respectively being "1". In response to these binary signals, the N-type FETs Q_1 , Q_5 and Q_7 in the voltage selector 2 are switched to the "on" state. As a result,
25 the voltage V_8 of the input point N_8 is derived through the common output point N_0 and the lead 26.

In the same manner, the output point N_0 is supplied with the voltage V_7 when the 3-bit binary

signals A, B and C are "1", "1" and "0", with the voltage V_6 when they are "1", "0" and "1", with the voltage V_5 when they are "1", "0" and "0", with the voltage V_4 when they are "0", "1" and "1", with the voltage V_3 when they are "0", "1" and "0", and with the voltage V_2 when they are "0", "0" and "1".

The N-type FETs Q_1 to Q_8 and the P-type FETs T_1 to T_8 are respectively formed on the single semiconductor substrate by well-known semiconductor integrated circuit techniques.

Referring now to Figure 2, the semiconductor substrate in which the N-type FET Q_3 and the P-type FET T_2 are formed in the shape of a semiconductor integrated circuit, includes an N-type semiconductor substrate 10 which is connected to earth and a P-type well region 11 which is formed in the surface of the N-type semiconductor substrate 10 and which is supplied with the reference voltage $-V_s$. The P-type FET T_2 is constituted by a P-type source region 15 and drain region 14 which are formed in the surface of the semiconductor substrate 10, and a gate electrode 20 which is formed through a gate oxide film 19 on the part of the semiconductor substrate between the source region 15 and the drain region 14. The N-type FET Q_3 is constituted by a P-type source region 13 and drain region 12 which are formed in the surface of the P-type well region 11, and a gate electrode 18 which is formed through a gate oxide film 17 on the part of the P-type well region 11 between the source region 13

and the drain region 12. A field oxide film 16 is formed on the surface of the semiconductor substrate 10 and is relatively thick.

5 The respective resistors R_1 to R_8 constituting the reference voltage circuit 1 are constituted by P-type polycrystalline silicon films formed on the thick oxide film 16 overlying the N-type semiconductor substrate 10 though not shown. The output voltages V_1 to V_8 of the reference voltage circuit
10 1 can be determined comparatively precisely because deviations in relative characteristics among resistance elements in a semiconductor integrated circuit are, in general, small. In the case where the polycrystalline silicon film is used as the resistor, its resistivity
15 can be made sufficiently great, so that the occupying area of the resistor in the semiconductor substrate can be made smaller than in the case where the resistor is formed as a semiconductor resistor which is formed by doping a semiconductor substrate with an impurity having
20 the opposite conductivity type to the substrate. In addition, since the resistors can have comparatively high values of resistance, the power dissipation of the circuit can be made low.

In the converter described above, the
25 voltage to be provided at the output point N_0 is not essentially limited by the threshold voltages of the FETs in the voltage selector 2 and the levels of the digital signals applied to the FETs.

By appropriately determining the conductivity types of the FETs in the voltage selector 2 as stated above, switching control signals of sufficient levels can be given between the gates and sources of the FETs to be switched into the "on" states, so that the "on" resistances of the FETs can be sufficiently lowered.

As a result, in the above described converter, digital signals of small level amplitudes can be used to provide a voltage responding to the digital signal at high speed and having an accurate level.

The above described converter does not need any booster circuit as in converters of the prior art referred to earlier. Moreover, the converter can be operated with the single potential source which has the level of the reference voltage $-V_s$ relative to earth.

Furthermore, in the voltage selector 2, the P-type FET and N-type FET which receive voltages different from each other from the reference voltage circuit 1, for example, the FETs T_7 and Q_7 may be controlled by the common binary signal $\bar{a}$ from the driving circuit 3.

As a result, the types of binary signals to be delivered from the driving circuit 3 and the number of output control signals corresponding thereto can be reduced.

In a modified form, the input digital signals can have an even larger number of bits, and the intervals of the multi-valued voltages to be delivered from the

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reference voltage circuit can be varied as desired.

Referring now to the digital-to-analog converter shown in Figure 3, the system shown includes a register which stores binary signals of 3 bits A, B and C applied through a plurality of lines 25 and which transmits them to a converter 21 through a plurality of lines 24.

The converter 21 has the same construction as the converter shown in Figure 1. That is, the converter 21 comprises the reference voltage circuit, the voltage selector and the driving circuit, and it supplies a buffer amplifier 22 through a line 26 with a voltage which is determined on the basis of the 3-bit binary signals A, B and C transmitted from the register 23.

The buffer amplifier 22 has a high input impedance characteristic in order to prevent current from flowing to the common output point N_0 of the converter 21. Thus, a voltage of an accurate analog value corresponding to the input digital signals is supplied from the converter 21 to the buffer amplifier 22.

Whilst, in the DAC shown in Figure 3, the driving circuit is included in the converter 21, it is possible to directly drive the voltage selector circuit with the outputs of the register 23. In this way, the driving circuit need not be arranged in the converter 21.

Referring now to the analog-to-digital converter shown in Figure 4, the ADC system converts an

input analog voltage V_x into binary signals of 3 bits A, B and C. The DAC converter 21 is constructed in similar manner to the converter shown in Figure 1.

On the basis of the 3-bit binary signals A, B and C supplied through respective lines 34, 35 and 36 from a control circuit 28 to be described later, the DAC 21 outputs an analog voltage on a line 26, this analog voltage corresponding to the 3-bit binary signals A, B and C.

A comparator 29 receives on one of its inputs the voltage delivered from the DAC 21, and on its other input an input analog voltage V_x to be converted into a digital signal through a line 33. The comparator 29 compares the voltage from the DAC 21 and the input voltage V_x , and transmits a binary signal C_D based on the result of the comparison to the control circuit 28 through a line 30.

The control circuit 28 is shown in greater detail in Figure 5, and comprises latch circuits 100, 108, 109 and 110, a counter 101, AND gates 102, 103, 104, 105 and 106, and OR gates 111, 112 and 113. A start signal S is applied through a line 31 to the reset terminal (hereinbelow, termed "R terminal") of each of these latch circuit 100, 108, 109, 110 and 101.

The AND gate 102 receives the output $\bar{Q}$ of the latch circuit 100 on one of its input terminals and receives a clock pulse C_n on the other input terminal through a line 32, thereby supplying a clock pulse to the

counter 101.

The counter 101 counts the clock pulses supplied from the AND gate 102, and supplies binary signals to its output lines 115 to 118, these binary signals having weights of "1", "2", "3" and "4" respectively. The binary signals output from the counter 101 on the lines 115, 116 and 117 are supplied to one input terminal of the respective AND gates 104, 105 and 106 and also to one input terminal of the respective OR gates 111, 112 and 113.

The binary signal C_D delivered from the comparator 29 shown in Figure 4 is applied to one input terminal of the AND gate 103 through a line 30. The clock pulse C_n is applied to the other input terminal of the AND gate 103 through an inverter 107. The output of the AND gate 103 is applied to the other input terminal of each of the AND gates 104, 105 and 106.

The outputs of the respective AND gates 104, 105 and 106 are applied to the set terminals (hereinafter referred to as "S terminals") of the latch circuits 108, 109 and 110. The output Q of each of these latch circuits 108, 109 and 110 is applied to the other input terminal of the respective OR gates 111, 112 and 113.

Signals supplied from the OR gates 111, 112 and 113 to lines 34, 35 and 36 respectively are used as the binary signals A, B and C to be supplied to the DAC 21 shown in Figure 4.

When the fourth clock pulse is applied to

the input terminal of the counter 101 through the AND gate 102, the counter 101 delivers an output signal to the set terminal S of the latch circuit 100 through a line 118.

5 The operation of the ADC shown in Figures 4 and 5 will now be described in greater detail.

First of all, the start signal S which is, for example, the binary signal "1" is supplied on the line 31 from an ADC operation controller not shown.

10 Thus, the latch circuits 100, 108, 109 and 110 and the counter 101 are respectively reset.

When the first clock pulse (binary signal "1") after the resetting of the latch circuits 100, 108, 109 and 110 is applied to the line 32, this clock pulse is supplied to the counter 101 through the AND-gate 102.

As a result, the binary signal "1" is delivered from the counter 101 to the line 115. At this time, the lines 116 and 117 are supplied with the binary signals "0". The binary signals delivered from the counter 101 to the lines 115, 116 and 117 are respectively transmitted to the lines 34, 35 and 36 through the OR gates 111, 112 and 113. Accordingly, the line 34 is supplied with the binary signal "1", and the lines 35 and 36 are supplied with the binary signals "0". That is, the 3-bit binary signals A, B and C are respectively made levels "1", "0" and "0".

The DAC 21 receives the 3-bit binary signals "1", "0" and "0" and thus has all its N-type FETs

Q₄, Q₆ and Q₇ (Figure 1) switched to the "on" states, so that it provides the line 26 with the voltage V₅ of the level equal to -V_s/2.

5 The voltage V₅ provided from the DAC 21 is compared with the input voltage V_x by means of the comparator 29.

In the case where the input voltage V_x is higher than the voltage V₅, the binary signal C_D of the "0" level is provided from the comparator 29.

10 Conversely, in the case where the input voltage V_x is lower than the voltage V₅, the binary signal C_D of the level "1" is provided from the comparator 29.

In the case where the binary signal C_D is at the "1" level because the input voltage V_x is lower than the voltage V₅ delivered from the DAC 21 as described above, the AND gate 103 is enabled by this signal. The AND gates 104, 105 and 106 are enabled when the "1" level signal is provided from the AND gate 103 by the "0" level of the clock pulse C_n.

20 Accordingly, the latch circuit 108 is set by the signal of "1" level supplied from the counter 101 through the line 115. The setting of the latch circuit 108 determines the "1" level of the binary signal A to be delivered to the line 34.

25 On the other hand, in the case where the binary signal C_D is at the "0" level because the input voltage V_x is higher than the voltage V₅, the AND gate 103 is held in the disabled state by this signal C_D.

Since a "1" level signal is not provided from the AND gate 103, the AND gates 104 to 106 are held in the disabled state. Accordingly, none of the latch circuits 108 to 110 is set.

5 When the second clock pulse C_n is applied to the line 32, the data in the counter 101 is thereby updated. As a result, the line 116 is supplied with a "1" level signal, and the lines 115 and 117 with "0" level signals. If the latch circuit 108 is brought into the
10 set state beforehand as described above, the signals A, B and C to be delivered to the lines 34, 35 and 36 become "1", "1" and "0" levels in response to the signals supplied from the latch circuit 108 and the lines 116 and 117, respectively. Unless the latch circuit 108 is brought
15 into the set state beforehand, the signals A, B and C become "0", "1" and "0" levels, respectively.

 In the case where the signals A, B and C are at the "1", "1" and "0" levels, the DAC 21 responds thereto to provide the voltage V_g supplied to the
20 terminal N_g in Figure 1, i.e., the voltage equal to $-(7/8) \times V_s$ volts. This voltage V_g is compared with the input voltage V_x by the comparator 29.

 In the case where the binary signal C_D of the "0" level is provided from the comparator 29 because
25 the input voltage V_x is higher than the voltage V_g , the AND gate 103 is held in the disabled state in similar manner as described previously. Accordingly, no set input is applied to the latch circuits 108 to 110.

In the case where the binary signal C_D of "1" level is provided from the comparator 29 because the input voltage V_x is lower than the voltage V_g , the AND gate 103 is enabled. Accordingly, when the second
5 clock pulse C_n is returned to the "0" level, a "1" level signal is provided from the AND gate 103 to enable the AND gates 104 to 106. The second latch circuit 109 is brought into the set state by the "1" level signal supplied through the AND gate 105. The "1" level output of the
10 latch circuit 109 determines the "1" level of the signal B to be supplied to the line 35.

In the case where the signals A, B and C are at the "0", "1" and "0" levels upon the application of the second clock pulse C_n as described above, the
15 DAC 21 provides the voltage V_3 , i.e., the voltage of $-(2/8) \times V_g$ volt. Also in this case, similar to that described above, the input voltage V_x and the voltage V_3 are compared by the comparator 29, and a determination is made as to whether or not the set signal is to be
20 supplied to the latch circuit 108. In other words, the level of the signal B is determined.

Likewise, the level of the binary signal C of the lowest bit is determined on the basis of the third clock signal C_n .

25 When, after the 3-bit binary signals A, B and C have been determined as stated above, the fourth clock pulse (at the level "1") is supplied to the control circuit 28, and a signal of the "1" level is supplied

from the counter 101 to the set terminal S of the latch circuit 100 through the line 118. In response to this signal, the latch circuit 100 is set. Furthermore, the set state of the latch circuit 100 enables the AND gate 102. As a result, the clock pulse is inhibited from being applied to the counter 101.

Thus by arranging the DAC as described above, the booster circuit may be dispensed with as stated previously, so that the whole circuit can be miniaturized.

Since the amplitudes of the binary signals, in other words, the "1" level and "0" level of the binary signals can be respectively made, for example, the level of the reference voltage $-V_s$ and earth potential as described above, the control circuit, DAC circuit, comparator can be operated by a power supply which has the level of the reference voltage $-V_s$. Thus, the respective circuits can be operated by the use of the single power supply, and an additional power supply such as a booster circuit is not required.

Furthermore, since the amplitude level of the binary signals can be made small as described above, the rate of change from one level to the other level of the signal can be made great. Therefore, the ADC can be put into a high-speed operation.

Figure 6 is a block diagram of an embodiment of an electronic sound generator employing a DAC.

The electronic sound generator includes an

oscillator circuit 50 which produces a low frequency signal of audio-frequency. The output signal of the oscillator 50 is supplied to a mixing circuit 60 through a line 56'.

5 The circuit also includes a counter which provides a line 54 with three kinds of signals. For the sake of clarity the single line 54 is illustrated as lines for transmitting the three sorts of signals.

10 The three kinds of signals consist of a first signal which has, for example, a reference frequency, a second signal which is obtained by dividing the frequency of the first signal by 2, and a third signal which is obtained by dividing the frequency of the first signal by 4.

15 By way of example, the first signal corresponds to the binary signal C of the lowest bit in each of the foregoing embodiments, the third signal to the binary signal A of the highest bit, and the second signal to the binary signal B of the intermediate
20 bit.

 The three kinds of signals delivered to the line 54 are supplied to DACs 21 and 21', each having the same construction as the DAC shown in Figure 1, directly and through an inverter 59 respectively.

25 An output signal from the DAC 21 is an envelope signal, which is supplied to the mixing circuit 60 through a line 55.

 Similarly, an output signal from the DAC 21'

is an envelope signal, which is supplied to the mixing circuit 60 through a line 55'.

The mixing circuit 60 receives the signal from the oscillator 50 and the envelope signal from the DACs 21 and 21', thereby providing a signal V_o with these signals mixed. The output signal V_o is supplied to a low-pass filter circuit 52 (hereinafter referred to as a "LPF") through a line 51.

The LPF 52 is provided to remove higher harmonic components included in the signal delivered by the mixing circuit 60. An output signal from the LPF 52 is supplied to a loudspeaker 53 through a line 58.

The loudspeaker 53 converts the signal supplied from the LPF 52 in acoustic energy.

The mixing circuit 60 comprises P-type FETs T_9 and T_{10} , N-type FETs Q_9 and Q_{10} and resistors R_9 to R_{12} .

In the mixing circuit 60, the P-type FET T_{10} and the N-type FET Q_{10} whose drain electrodes are connected in common and whose gate electrodes are also connected in common constitute a complementary type amplifier circuit.

The resistor R_{11} which is connected between the common drain electrodes and the common gate electrodes of the P-type FET T_{10} and N-type FET Q_{10} , and the resistor R_{12} which is connected between the common gate electrodes and an output terminal of the oscillator 50 constitute a feedback circuit for the amplifier circuit.

The P-type FET T_9 and the resistor R_9 which are connected in parallel between the source electrode of the P-type FET T_{10} and earth constitute a variable resistance circuit R_x . More specifically, the
5 resistance between terminals R_{x1} and R_{x2} of the variable resistance circuit R_x is varied in such a manner that the source - drain resistance of the P-type FET T_9 is varied by an analog voltage applied to its gate electrode.

Likewise, the N-type FET Q_9 and the
10 resistor R_{10} which are connected in parallel between the source electrode of the N-type FET Q_{10} and a power supply terminal V_9 constitute a variable resistance circuit R_x' .

As referred to above, the output signal
15 of the counter 56 is supplied to the DAC 21 directly and to the DAC 21' through the inverter 59. Accordingly, the signal delivered from the DAC 21 to the line 55 and the signal delivered from the DAC 21' to the line 55' are complementarily changed in response to the change
20 of the output signal of the counter 56.

In response to the changes of the delivered signals, the source - drain resistance of the P-type FET T_9 in the variable resistance circuit R_x and the source - drain resistance of the N-type FET Q_9 in
25 the variable resistance circuit R_x' are changed in an identical direction. That is, the terminal resistance of the variable resistance circuit R_x and that of the variable resistance circuit R_x' are varied in the identical

direction in response to the change of the output signal of the counter 56.

Accordingly, the level of the voltage V_0 to be provided from the mixing circuit 60 is controlled by the output signal of the counter 56.

This will be better understood from the following explanation.

In order to assist the explanation, it is assumed that the N-type FET Q_{10} is held substantially in the "off" state by the output voltage of the oscillator 50.

Figure 7B shows an equivalent circuit which is constituted by the P-type FET T_{10} , the resistors R_{12} and R_{11} and the variable resistance circuit R_x . In Figure 7B, R' denotes the terminal resistance of the variable resistance circuit R_x , i denotes current which flows through the resistors R_{12} , R_{11} and R_x , and g_m denotes the mutual conductance of the P-type FET T_{10} . V_{in} denotes the voltage which is supplied from the oscillator 50. Furthermore, V_{01} denotes a voltage which is developed at the junction between the resistors R_{12} and R_{11} , and V_{02} denotes a voltage which is developed across the variable resistance circuit R_x .

The following relationships can be deduced from the equivalent circuit of Figure 7B:

$$\begin{aligned} i &= (V_{in} - V_{01})/R_{12} = (V_{01} - V_0)/R_{11} \\ &= V_{02}/R' = (V_{01} - V_{02}) g_m \end{aligned} \quad (1)$$

$$V_{in} - V_{01} = \frac{R_{12}}{R'} V_{02}, \quad V_{01} - V_0 = \frac{R_{11}}{R'} V_{02} \quad (2)$$

Equations (3) to (5) can be deduced from the above equations (1) and (2):

$$V_{in} = \left\{ 1 + \frac{R_{12} \cdot R' \cdot g_m}{R' (1 + R' \cdot g_m)} \right\} V_{O1} \quad (3)$$

$$V_O = \left\{ 1 - \frac{R_{11} \cdot R' \cdot g_m}{R' (1 + R' \cdot g_m)} \right\} V_{O1} \quad (4)$$

$$\frac{V_O}{V_{in}} = \frac{1 - \frac{R_{11} \cdot R' \cdot g_m}{R' (1 + R' \cdot g_m)}}{1 + \frac{R_{12} \cdot R' \cdot g_m}{R' (1 + R' \cdot g_m)}} \quad (5)$$

When the mutual conductance g_m of the P-type FET T_{10} is comparatively large, equation (5) can be simplified and expressed as follows:

$$\frac{V_O}{V_{in}} = - \frac{R_{11} - R'}{R_{12} + R'} \quad (6)$$

As will be apparent from equations (5) and (6), the ratio V_O/V_{in} is varied by the value R' of the terminal resistance of the variable resistance circuit R_x . Figure 7A is a graph showing the characteristic of the ratio (V_O/V_{in}) plotted to a base of terminal resistance (R') .

Similarly, the ratio V_O/V_{in} at the time when the N-type FET Q_{10} is held substantially in the "on" state and the P-type FET T_{10} is held substantially in the "off"

state by the output voltage V_{in} of the oscillator 50 can be evaluated.

As stated above, the terminal resistances of the variable resistance circuits R_x and R_x' can be varied by the combinations of the three kinds of signals supplied from the counter 56. Therefore, the signal V_0 whose frequency is coincident with the oscillation frequency of the oscillator 50 and whose level corresponds to the output digital signal of the counter 56 can be provided from the mixing circuit 60.

When the three kinds of signals A, B and C supplied from the counter 56 are those shown in Figure 8, the DAC 21 responds thereto to provide voltages as shown by the waveform having a broken line in Figure 9.

On the other hand, the DAC 21' provides voltages as shown by the waveform having a solid line in Figure 9.

Figures 10A to 10D illustrate the respective waveforms of the output of the oscillator 50, the output of the DAC 21', the output of the DAC 21 and the output of the mixing circuit 60 in the case where the signals as shown in Figure 8 are provided from the counter 56.

The voltages provided from the DACs 21 and 21' are varied approximately in a linear manner with respect to time t as shown in Figures 10B and 10C, whereas the envelope of the signal output of the mixing circuit 60 as shown in Figure 10D does not vary linearly with respect to time t . This is based on the facts that the

values of the terminal resistances of the variable resistance circuits R_x and R_x' are not proportional to the variations of the voltages delivered from the DACs 21 and 21', and that the value of the ratio V_O/V_{in} is not proportional to the variation of the value of the resistance R' as illustrated in Figure 7A.

The electronic sound generator described above can be miniaturized because any booster circuit is not required for the DACs employed therein.

In a modified form of the electronic sound generator, a second oscillator is provided in order to apply an output to the gate of the P-type FET T_{10} within the mixing circuit 60 through a resistor. Thus, the output of the further oscillator and the output of the oscillator 50 are combined. As a result, sounds of various tones can be generated from the mixing circuit 60. Furthermore, the electronic sound generator may include a plurality of such further oscillators.

The two DACs are used for varying the envelope of the audio signal to be supplied from the mixing circuit 60. By arranging both the DACs in the same construction, the design of the electronic sound generator is greatly facilitated.

Furthermore, it is also possible to vary the envelope of the audio signal with a single DAC. In this case, a new envelope signal can be obtained by, for example, inverting with an inverting amplifier an envelope signal delivered from the single DAC. This

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will enable the electronic sound generator to be miniaturized still further.

5 In the circuit shown in Figure 6, the signal of the counter 56 is supplied to the DAC 21' through the inverter 59. However, the inverter 59 can be omitted in which case the counter 56 is constructed so as to also provide inverted signals of the respective output signals.



CLAIMS.

1. A converter including:-

a voltage selector which comprises a plurality of input points supplied with voltages all having different levels from one another, a single common output point, and a plurality of insulated-gate field effect transistors with their source - drain paths connected between said plurality of input points and said common output point, each of said plurality of insulated-gate field effect transistors having a conductivity type which is determined so that each transistor can be brought into the "on" state by a level of a binary signal which affords a greater level difference relative to the voltage to be switched by each transistor; and

a driving circuit which provides binary signals of a plurality of bits for controlling the "on" and "off" states of said plurality of insulated-gate field effect transistors.

2. A converter according to Claim 1, wherein the gate electrodes of at least one P-channel type insulated-gate field effect transistor and one N-channel type insulated-gate field effect transistor in said voltage selector are connected in common so as to receive an identical binary signal.

3. A converter according to Claim 1, wherein said plurality of insulated-gate field effect transistors in said voltage selector are formed on a single semiconductor substrate.



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4. A converter according to any one of the preceding claims, wherein said transistors in the voltage selector are arranged in fir-tree configuration as hereinbefore defined.

5. An analog-to-digital converter including:
a converter according to any one of the preceding claims;

a comparator having a first input supplied with an input signal to be converted and a second input supplied with the voltage provided from said voltage selector; and

a control circuit supplied from the output of said comparator and controlled in order to provide binary signals of a plurality of bits for controlling the "on" and "off" states of said plurality of insulated-gate field effect transistors.

6. A digital-to-analog converter including:
a converter according to any one of the preceding claims 1 to 4;

a register which stores binary signals of three bits and transmits them to the converter on a plurality of lines; and

a buffer amplifier connected in the output line from the converter.

7. A digital-to-analog converter according to Claim 6, wherein said buffer amplifier has a high input impedance.



8. An electronic sound generator including;
first and second converters according to any one of the
preceding Claims 1 to 4;

a low frequency oscillator circuit;
a counter providing three kinds of signals;
a mixing circuit receiving inputs from the
first and second converters and the oscillator;

a low pass filter and a loudspeaker connected
in series with the output of the mixing circuit, the
counter supplying inverted and non-inverted signals to
the respective second and first converters.

9. An electronic sound generator according
to Claim 8, wherein the mixing circuit includes first and
second variable resistance circuits respectively
controlled by the outputs of the first and second
converters.

10. An electronic sound generator according to
Claim 8 or 9, wherein the counter includes frequency
dividing means to divide a first square-wave signal into
a second signal having half the frequency and a third
signal having a quarter of the frequency of the first
signal, the three sets of square-wave signals being
supplied directly to the first converter and through
an inverter to the second converter.

11. A converter constructed substantially as
herein described with reference to and as illustrated
in Figures 1 and 2 of the accompanying drawings.



12. A digital-to-analog converter constructed substantially as herein described with reference to and as illustrated in Figure 3 of the accompanying drawings.

13. An analog-to-digital converter constructed substantially as herein described with reference to and as illustrated in Figures 4 and 5 of the accompanying drawings.

14. An electronic sound generator constructed substantially as herein described with reference to and as illustrated in Figure 6 of the accompanying drawings.