What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

~~a plurality of memory cells that is provided on~~ a semiconductor substrate;

a trench extending in a first direction, and dividing the semiconductor substrate into active areas adjacent to each other in a second direction crossing to the first direction;

control gate electrodes extending to the second direction;

a select gate electrode extending to the second direction and adjacent to one of the control gate electrodes, and a length of the select gate electrode in the second direction is longer than that of the control gate electrodes in the second direction;

~~and includes a~~ charge storage layers disposed between the control gate electrodes and the active areas;

an insulating film disposed directly under the select gate electrode in the trench;

a first air gap provided between the charge storage layers adjacent in the second~~a word line~~ direction, and formed under the control gate electrode in the trench; and

a second air gap provided between charge storage

layers adjacent in the first~~a bit line~~ direction, wherein

the second air gap is present at a position higher than an upper surface of the charge storage layer, and the first air gap continuously extends from the insulating film.

2. The nonvolatile semiconductor memory device according to claim 1, wherein the first air gap is present at a position lower than a lower surface of the charge storage layer.

3. The nonvolatile semiconductor memory device according to claim 1,

wherein an isolation insulating film is disposed in the ~~first air gap penetrates a~~ trench ~~that separates active areas of the memory cells and is provided in the semiconductor substrate~~.

4. The nonvolatile semiconductor memory device according to claim 1, wherein the second air gap is vertically asymmetric and an upper end of the second air gap is spire-shaped.

5. The nonvolatile semiconductor memory device according

to claim 1, further comprising:

a third air gap provided between the one of the control electrodes and the select gate electrode and extending in the second direction, and

~~wherein~~ the first air gap and the third air gap are connected at an intersection of the first air gap and the third air gap~~is formed continuously in the trench across memory cells adjacent in the bit line direction~~.

6. The nonvolatile semiconductor memory device according to claim 1~~5~~, wherein

the second air gap ~~is formed~~ continuously extends~~across memory cells adjacent~~ in the second~~word line~~ direction between the charge storage layers adjacent in the first direction, and

the first air gap and the second air gap are connected at an intersection of the first air gap and the second air gap.

7. The nonvolatile semiconductor memory device according to claim 1~~5~~, ~~further comprising a select gate transistor that includes a select gate electrode and is formed by being connected to an active area of a memory cell,~~ wherein

~~the~~ the first air gap is present under the select gate

electrode along the trench.

8. The nonvolatile semiconductor memory device according to claim 1~~6~~, further comprising~~wherein the first air gap penetrates under the select gate electrode along the trench~~:

a peripheral transistor disposed in a peripheral circuit portion around a memory cell array in which the charge storage layers are provided; and

a fourth air gap formed under a gate electrode of the peripheral transistor.

9. A nonvolatile semiconductor memory device comprising:

~~a plurality of memory cells in which a tunnel dielectric film, a charge storage layer, an inter-electrode dielectric film, and a control gate electrode are sequentially stacked on~~ a semiconductor substrate;

a trench extending in a first direction, and dividing~~that is provided in~~ the semiconductor substrate into~~and separates~~ active areas adjacent to each other in a second direction crossing to the first direction~~of the memory cells~~;

control gate electrodes extending to the second direction;

a select gate electrode extending to the second direction and adjacent to one of the control gate electrodes, and a length of the select gate electrode in the second direction is longer than that of the control gate electrodes in the second direction;

charge storage layers disposed between the control gate electrodes and the active areas; and

an insulating film disposed directly under the select gate electrode in the trench;

an air gap ~~that is~~ provided between the charge storage layers adjacent in the second~~a word line~~ direction~~,~~ and formed under the control gate electrode in~~penetrates to a bottom of~~ the trench, wherein~~and is configured such that~~ the air gap continuously extends from the insulating~~inter-electrode dielectric~~ film~~ reaches a sidewall of the charge storage layer~~.

10. The nonvolatile semiconductor memory device according to claim 9, further comprising:

a sidewall dielectric film formed on a sidewall of the trench.

11. The nonvolatile semiconductor memory device according to claim 10,

wherein the air gap is formed continuously in the trench across adjacent memory cells.

~~12. The nonvolatile semiconductor memory device according to claim 11, further comprising a select gate transistor that includes a select gate electrode and is formed by being connected to an active area of a memory cell, wherein the air gap is present under the select gate electrode along the trench.~~

~~13. The nonvolatile semiconductor memory device according to claim 12, wherein the air gap penetrates under the select gate electrode along the trench.~~

12~~14~~. The nonvolatile semiconductor memory device according to claim 10, further comprising:

a peripheral transistor formed in a peripheral circuit portion around a memory cell array in which the memory cells are provided; and

an air gap formed in a trench under a gate electrode of the peripheral transistor.

13~~15~~. A method of manufacturing a nonvolatile semiconductor memory device comprising:

forming a charge storage material on a semiconductor substrate via a tunnel dielectric film;

forming a trench in the semiconductor substrate in a bit line direction via the charge storage material and the tunnel dielectric film;

forming an embedded dielectric film in the trench;

forming an inter-electrode dielectric film on the embedded dielectric film and the charge storage material;

forming a control gate electrode material on the inter-electrode dielectric film;

forming floating gate electrodes separated for each memory cell by patterning the control gate electrode material, the inter-electrode dielectric film, and the charge storage material, and forming control gate electrodes arranged on charge storage layers in a word line direction;

forming a first air gap between charge storage layers adjacent in the word line direction by removing at least part of the embedded dielectric film embedded in the trench; and

forming a second air gap between charge storage layers adjacent in the bit line direction by forming a cover dielectric film that extends between the control gate electrodes, wherein

the second air gap is present at a position higher than an upper surface of the charge storage layer, wherein

an inside of the trench that separates active areas of the memory cells is filled partway with a flowable embedded dielectric film that is solidified by cross-linking, and

an inside of the trench used for isolation of a peripheral circuit is filled with the flowable embedded dielectric film and a nonflowable embedded dielectric film.

14~~16~~. The method according to claim 13~~15~~, further comprising:

forming a sacrifice film on the semiconductor substrate so that the first air gap and a space between the floating gate electrodes are filled, after removing at least part of the embedded dielectric film embedded in the trench;

forming an inter-layer dielectric film on the sacrifice film;

planarizing the inter-layer dielectric film; and

removing the sacrifice film after planarizing the inter-layer dielectric film.

~~17. The method according to claim 15, wherein~~

~~an inside of a trench that separates active areas of~~

~~the memory cells is filled partway with a flowable embedded dielectric film that is solidified by cross-linking, and~~

~~an inside of a trench used for isolation of a peripheral circuit is filled with the flowable embedded dielectric film and a nonflowable embedded dielectric film.~~

15~~18~~. The method according to claim 13~~15~~, further comprising:

forming a sidewall dielectric film on a sidewall of the tunnel dielectric film and a sidewall of the trench,

wherein the embedded dielectric film formed in the trench is formed on the first sidewall protection film.

16~~19~~. The method according to claim 15~~18~~, further comprising forming a gate sidewall protection film on a sidewall of the inter-electrode dielectric film before removing part of the embedded dielectric film in the trench.