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(71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): GROCHOWSKI, Ed [US/US]; 5565 Yale Drive, San Jose, CA 95118 (US). SHARMA, Vinod [IN/IN]; 954 Hibiscus Lane, San Jose, CA 95117 (US). BHUSHAN, Bharat [IN/IN]; 21301 Milford Drive, Cupertino, CA 95014 (US). CRAWFORD, John [US/US]; 20128 Chateau Drive, Saratoga, CA 95070 (US).

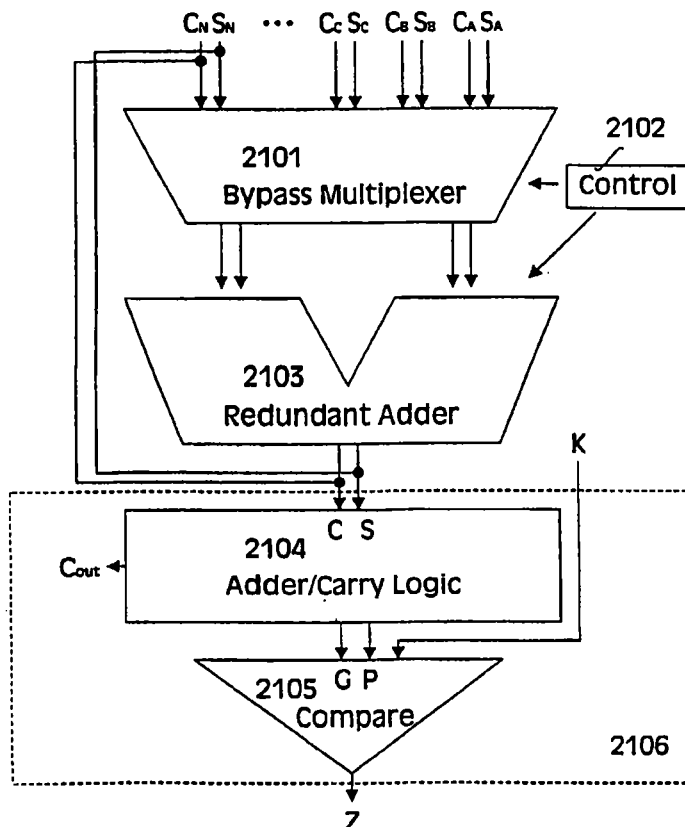
(74) Agents: MALLIE, Michael, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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(54) Title: METHOD AND APPARATUS FOR PERFORMING SINGLE-CYCLE ADDITION OR SUBTRACTION AND COMPARISON IN REDUNDANT FORM ARITHMETIC

WO 01/46795 A3



(57) Abstract: A method and apparatus is disclosed that uses an arithmetic circuit for adding numbers represented in a redundant form to also subtract numbers received in redundant form, including numbers received from a bypass circuit. A non-propagative comparator circuit is then used to compare a given value with a result from the arithmetic circuit to determine if the result is equal to the given value. All of the operations described above can be accomplished without propagating carry signals throughout the circuitry. The method includes generating a complemented redundant form of at least one number supplied to the arithmetic circuit in redundant form. It also includes providing adjustment input to the arithmetic circuit to augment a result produced through the arithmetic circuit. This adjustment causes the arithmetic circuit to generate a valid outcome in redundant form as a result of a subtraction operation if the arithmetic operation is subtraction. Then the result is compared to a given value using a non-propagative comparator to determine equality or inequality of the result to the given value.



ACTION

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