

METHOD FOR FORMING CONDUCTIVE INTERCONNECTION STRUCTURE

TECHNICAL FIELD

5 [0001] The present disclosure belongs to the field of semiconductor manufacturing technologies, and specifically relates to a method for forming a conductive interconnect structure.

BACKGROUND

10 [0002] In a semiconductor manufacturing process, metal interconnect structures are formed through a back end of line (BEOL) process to provide wiring for integrated circuits. Generally, a metal interconnect structure includes a plurality of metal interconnect layers, and an electrical connection between different metal interconnect layers is implemented through a conductive via.

15 [0003] With the progressive reduction in the pitch and line width of conductive lines in the integrated circuit, there is an urgent need to provide a method for forming a conductive via capable of establishing a reliable electrical connection between metal interconnect layers.

20 SUMMARY

[0004] Embodiments of the present disclosure disclose a method for forming a conductive interconnect structure, which aims to at least solve the problem that it is difficult to form a conductive via capable of establishing a reliable electrical connection in the related art.

25 [0005] To at least solve the above technical problem, an embodiment of the present disclosure provides a method for forming a conductive interconnect structure, including:

forming a predetermined mask pattern on a conductive layer;

doping a first mask pattern to form a doped region having a predetermined depth in the first mask pattern, wherein the first mask pattern is the predetermined mask pattern
30 that has been doped, and a second mask pattern is the predetermined mask pattern that is

undoped; and wherein the doped region has a higher etch rate than an undoped region;
and

etching the conductive layer by the first mask pattern and the second mask pattern
to form the conductive interconnect structure; wherein a conductive line in a region
5 corresponding to the second mask pattern has a greater height than a conductive line in a
region corresponding to the first mask pattern, and the conductive line in the region
corresponding to the second mask pattern is formed as a conductive via.

[0006] In some embodiments, etching the conductive layer by the first mask pattern and
the second mask pattern includes:

10 etching the first mask pattern and the second mask pattern while etching the
conductive layer by the first mask pattern and the second mask pattern;

wherein an etch selectivity between the conductive layer and an undoped region in
the predetermined mask pattern is less than a predetermined value.

[0007] In some embodiments, the step of etching the first mask pattern and the second
15 mask pattern while etching the conductive layer by the first mask pattern and the second
mask pattern includes stages of:

when the doped region in the first mask pattern is etched and removed, partially
etching the second mask pattern while partially etching the conductive layer not covered
by the predetermined mask pattern;

20 when the first mask pattern is completely removed, etching the second mask pattern
correspondingly while further etching the conductive layer not covered by the
predetermined mask pattern; and

when the second mask pattern is completely removed, completely removing the
conductive layer not covered by the predetermined mask pattern to form a plurality of
25 conductive lines, and partially etching the conductive layer in the region corresponding to
the first mask pattern, such that the conductive line in the region corresponding to the
second mask pattern has a greater height than the conductive line in the region
corresponding to the first mask pattern, and the conductive line in the region
corresponding to the second mask pattern is used as the conductive via.

30 [0008] In some embodiments, etching the conductive layer by the first mask pattern and
the second mask pattern includes:

removing the doped region in the first mask pattern;

etching the remaining first mask pattern and the second mask pattern to completely
remove the first mask pattern; and

partially removing the conductive layer in the region corresponding to the first mask pattern while removing the remaining second mask pattern, to form the conductive via in the conductive line in the region corresponding to the second mask pattern.

[0009] In some embodiments, the conductive layer not covered by the predetermined mask pattern is etched while the first mask pattern and the second mask pattern are etched and removed.

[0010] In some embodiments, before removing the doped region in the first mask pattern, the method further includes:

etching the conductive layer by the first mask pattern and the second mask pattern to form the conductive line; or

after removing the doped region in the first mask pattern, the method further includes:

etching the conductive layer by the remaining first mask pattern and the second mask pattern to form the conductive line.

[0011] In some embodiments, forming the predetermined mask pattern on the conductive layer includes:

forming a mandrel on the conductive layer; and

forming a spacer as the predetermined mask pattern on a sidewall of the mandrel.

[0012] In some embodiments, doping the first mask pattern includes:

doping a first spacer to form a doped region having a predetermined depth in the first spacer, wherein the first spacer is the spacer that has been doped, and a second spacer is the spacer that is undoped.

[0013] In some embodiments, doping the first spacer includes:

forming a planarization layer on the conductive layer to fill a region between spacers;

performing a planarization process on the planarization layer to expose the mandrel and the spacer;

forming a mask layer on a surface of the planarization layer to block the second spacer; and

performing ion implantation on the first spacer that is unblocked.

[0014] In some embodiments, the planarization layer includes an SOC material; or an element for the ion implantation is Ge.

[0015] In some embodiments, the method further includes:

removing the mandrel and the planarization layer.

[0016] In some embodiments, the doped region of the first spacer is removed while the mandrel and/or the planarization layer are removed.

[0017] In some embodiments, a hard mask layer is further provided between the conductive layer, and the mandrel and the planarization layer, and removing the mandrel and the planarization layer includes:

removing the mandrel and the planarization layer by taking the hard mask layer as an etch stop layer.

[0018] In some embodiments, etching the conductive layer by the first mask pattern and the second mask pattern includes:

removing the hard mask layer and the conductive layer which are not covered by the first spacer and the second spacer by taking the first spacer and the second spacer as masks.

[0019] In some embodiments, a liner is further provided below the conductive layer, and removing the hard mask layer and the conductive layer which are not covered by the first spacer and the second spacer by taking the first spacer and the second spacer as masks further includes:

removing the liner not covered by the first spacer and the second spacer.

[0020] In some embodiments, the liner includes at least one of TiN, TaN, Al, Cu, Ni, Co, Ru, Ti and Ta.

[0021] In some embodiments, the conductive layer is a metal conductive layer; or the conductive layer includes at least one of Ru, Co, Mo, W, Al and Rh.

[0022] In some embodiments, forming the predetermined mask pattern on the conductive layer includes:

forming the predetermined mask pattern by self-aligned multi-patterning.

[0023] In the method for forming a conductive interconnect structure provided in the embodiments of the present disclosure, a predetermined mask pattern is doped so that the doped region in the predetermined mask pattern has a higher etch rate than an undoped region, thereby forming conductive lines of different heights through a subsequent etching process, and the conductive line in the region corresponding to the second mask pattern has a greater height than the conductive line in the region corresponding to the first mask pattern, thereby forming a conductive via. The conductive via is formed by a self-aligned process, which will not cause the problem of alignment deviation between the conductive via and the conductive line that may be otherwise caused by a damascene process in the related art, while involving fewer process steps without a precise mask pattern, compared

with a subtractive etching process in the related art.

BRIEF DESCRIPTION OF DRAWINGS

[0024] FIG. 1 is a schematic diagram of a method for forming a metal interconnect structure in the related art;

[0025] FIG. 2 is a schematic diagram of another method for forming a metal interconnect structure in the related art;

[0026] FIGs. 3 to 11 respectively show schematic diagrams of semiconductor structures corresponding to respective steps in a method for forming a conductive interconnect structure according to an embodiment of the present disclosure; and

[0027] FIGs. 12 to 20 respectively show schematic diagrams of semiconductor structures corresponding to respective steps in a method for forming a conductive interconnect structure according to another embodiment of the present disclosure.

DETAIL DESCRIPTION OF EMBODIMENTS

[0028] To clarify the objects, technical solutions and advantages of the present disclosure, the technical solutions in the embodiments of the present disclosure will be clearly and completely described below with reference to the accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are some, not all, of the embodiments of the present disclosure. All other embodiments obtained by the ordinarily skilled in the art based on the embodiments of the present disclosure without paying any creative effort shall be included in the protection scope of the present disclosure.

[0029] It should be understood by those skilled in the art that the embodiments of the present disclosure are merely illustration of the structures and methods of the present disclosure that may be embodied in various forms. Furthermore, each example given in connection with the various embodiments is intended to be illustrative, and not restrictive. Furthermore, the figures are not necessarily drawn to scale, where some features may be exaggerated to show details of particular components. Therefore, specific structural and functional details in the embodiments of the present disclosure are not to be interpreted as being restrictive, but merely as a representative basis for teaching one skilled in the art

to variously employ the embodiments of the present disclosure. It should also be noted that like and corresponding elements are indicated by like reference numerals.

[0030] In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, to provide an understanding of various embodiments of the present disclosure. However, it should be understood by those skilled in the art that various embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail to avoid obscuring the present disclosure.

[0031] For purposes of the description hereinafter, the terms "upper", "right", "left", "vertical", "horizontal", "top", "bottom", and derivatives thereof shall relate to the orientations of the structures and methods disclosed in the accompanying drawings. It will be understood that when an element as a layer, region or substrate is referred to as being "on" another element, it may be directly on the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly on" another element, there is no intervening element between the two. It will also be understood that when an element is referred to as being "under" another element, it may be directly under the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly under" another element, there is no intervening element between the two.

[0032] In the related art, there is provided a method for forming a metal interconnect structure as shown in FIG. 1, in which an insulation layer is formed on a metal interconnect line 11 by a damascene process, a via hole is formed in the insulation layer, and then a metal is filled into the via hole to form a conductive via 12 configured to electrically connect the current metal interconnect line 11 with an upper metal interconnect line. However, on the one hand, this method has the problem that the via hole is difficult to be aligned with the underlying metal interconnect line 11 while the via hole is formed, especially in the case of a very narrow conductive line; and on the other hand, line wiggling of the metal interconnect line may exist, causing an alignment deviation between the conductive via 12 and the metal interconnect line 11, and thereby increasing the impedance of the metal interconnect structure.

[0033] In the related art, there is further provided a method for forming a metal interconnect structure as shown in FIG. 2, which adopts a subtractive etching process to form a mask pattern 13 at a position where a conductive via is to be formed, and then etch

a metal interconnect line, where an unetched part is higher than the etched part, and the unetched part serves as the conductive via. However, this method requires the formation of a precise mask pattern 13 in the case of a very close pitch of conductive lines, and if there is a deviation in the mask pattern 13, an undesired conductive via may be formed at a position where a conductive via is not desired.

[0034] The technical solutions provided in the embodiments of the present disclosure will be described in detail below with reference to the accompanying drawings.

[0035] To at least solve the above technical problem, an embodiment of the present disclosure provides a method for forming a conductive interconnect structure, which may include the following steps S11 to S11 to S13.

[0036] At S11, a predetermined mask pattern is formed on a conductive layer.

[0037] As shown in FIG. 3, a semiconductor structure includes a substrate 100, a liner 110 formed on the substrate 100, a conductive layer 120 formed on the liner 110, a hard mask layer 130 formed on the conductive layer 120, and a predetermined mask pattern 140 formed on the hard mask layer 130.

[0038] The substrate 100 may be composed of a silicon-containing material. The silicon-containing material includes, but is not limited to, any one or combination of silicon, monocrystalline silicon, polycrystalline silicon, SiGe, monocrystalline SiGe, polycrystalline SiGe or carbon-doped silicon (Si: C), amorphous silicon, or the like, and the substrate 100 may have a single-layer or multi-layer structure. The substrate 100 may also be composed of other semiconductor materials, such as Ge, and a compound semiconductor substrate which may be, for example, a III-V type semiconductor substrate, such as GaAs and the like.

[0039] The liner 110 may be formed by sputtering, chemical vapor deposition (CVD), atomic layer deposition (ALD), and the like, and the liner 110 may include a conductive material such as TiN or TaN. In some embodiments, the liner 110 may also be composed of other conductive materials, such as Al, Cu, Ni, Co, Ru, Ti, Ta, or a combination thereof.

[0040] The conductive layer 120 may be a metal conductive layer or a non-metal conductive layer. In some implementations of embodiments of the present disclosure, the conductive layer 120 is a metal conductive layer, and may include Ru, Co, Mo, W, Al or Rh, or an alloy thereof. The conductive layer 120 may be formed by, for example, CVD, plasma enhance CVD (PECVD), physical vapor deposition (PVD), or other deposition processes.

[0041] The hard mask layer 130 is a material used as an etching mask in the

semiconductor process, and may be configured to protect the conductive layer 120 from being etched when a predetermined mask pattern 140 is subsequently etched, for example. The hard mask layer 130 may be composed of a metal or a dielectric material, such as silicon nitride, silicon oxide, or a combination of silicon nitride and silicon oxide, and
5 may be formed by a process such as low pressure CVD (LPCVD) and the like.

[0042] The predetermined mask pattern 140 may be composed of any dielectric material, such as a dielectric oxide, a dielectric nitride, and/or a dielectric oxynitride. In some embodiments, the mask pattern 140 may be composed of a non-conductive low capacitance dielectric material, such as silicon dioxide. To obtain a finer mask pattern 140,
10 the mask pattern 140 may be formed in a self-aligned multi-patterning method, such as self-aligned double patterning or self-aligned quadruple patterning.

[0043] It should be understood by those skilled in the art that in the above description, the substrate 100, the liner 110, and the hard mask layer 130 are optional, and in some implementations of embodiments of the present disclosure, one or more of the substrate
15 100, the liner 110, and the hard mask layer 130 may be omitted.

[0044] It should be noted that, in the example of FIG. 3, other layers may be present between the substrate 100 and the conductive layer 120, and the embodiments of the present disclosure do not limit the metal interconnect layer where the conductive layer 120 is located to be a lowermost metal interconnect layer, and instead, it may be any one
20 of the interconnect layers. In other words, there may be other metal interconnect layers in direct contact with the conductive layer 120.

[0045] At S12, a first mask pattern is doped to form a doped region having a predetermined depth in the first mask pattern, where the first mask pattern is the predetermined mask pattern that has been doped, and a second mask pattern is the
25 predetermined mask pattern that is undoped.

[0046] As shown in FIG. 4, some of a plurality of predetermined mask patterns are formed with a doped region having a predetermined depth (indicated by the hatched portion in FIG. 4), which are all referred to as first mask patterns; while the remaining predetermined mask patterns without a doped region (i.e., without a hatched portion) are
30 referred to as second mask patterns.

[0047] In some embodiments, the first mask pattern 141 may be doped by ion implantation or the like. For example, Ge may be implanted into the first mask pattern 141, and an implantation depth of the ion implantation may be precisely controlled by controlling the implantation energy and implantation dose of the ion implantation. As will

be seen below, the implantation depth is associated with a height of the conductive via to be subsequently formed. In the subsequent etching process, the region subjected to the ion implantation has a higher etch rate than the region without ion implantation, that is, the doped region has a higher etch rate than an undoped region.

5 [0048] When the doping process is performed, photoresist (not shown) may be used to shield a region that does not need to be doped, so that the first mask pattern 141 and the second mask pattern 142 can be obtained.

[0049] At S13, the conductive layer is etched by the first mask pattern and the second mask pattern to form the conductive interconnect structure; where a conductive line in a region corresponding to the second mask pattern has a greater height than a conductive line in a region corresponding to the first mask pattern, and the conductive line in the region corresponding to the second mask pattern is formed as a conductive via.

10 [0050] In other words, a height of the conductive line in the region corresponding to the second mask pattern is higher than a height of the conductive line in the region corresponding to the first mask pattern, thereby forming a conductive via.

[0051] It will be readily appreciated that in the above process of etching the conductive layer, a part of the hard mask layer 130 that is not covered by the first mask pattern and the second mask pattern is completely etched.

15 [0052] The above step S13 may be implemented in a one-step etching manner or in a step-by-step etching manner. For clarity, the step-by-step etching manner is described in detail first herein.

[0053] In some implementations of embodiments of the present disclosure, the step S13 may include the following steps S131 to S134.

[0054] At S131, the doped region in the first mask pattern is removed.

25 [0055] As shown in FIG. 5, the doped region in the first mask pattern 141 may be removed by an etching process. Since a partial region of the first mask pattern 141 is doped, the doped region has a higher etch rate than an undoped region in the etching process, so that the doped region can be removed. In some implementations, the conductive layer not covered by the predetermined mask pattern 140 is etched while the doped region of the first mask pattern 141 is etched and removed, thereby reducing the process steps.

[0056] At S132, the conductive layer is etched by the remaining first mask pattern and the second mask pattern to form the conductive line.

[0057] As shown in FIG. 6, after this step of etching, a plurality of conductive lines 121

are formed in the semiconductor structure. It should be noted that the embodiments of the present disclosure are not limited thereto, and before step S131, the conductive layer 120 may be etched by the first mask pattern 141 and the second mask pattern 142 to form the conductive line 121. The doped regions are not removed from the first mask pattern 141 and the second mask pattern 142 here.

[0058] It should be understood by those skilled in the art that step S132 is optional, and in some implementations, the conductive layer 120 not covered by the predetermined mask pattern may be etched while the first mask pattern 141 and the second mask pattern 142 are etched and removed, so that a separate step of etching to form the conductive line 121 is omitted, thereby reducing the process steps.

[0059] At S133, the remaining first mask pattern and the second mask pattern are etched to completely remove the first mask pattern.

[0060] As shown in FIG. 7, since the second mask pattern 142 has a height greater than the remaining first mask pattern 141, the second mask pattern 142 partially remains after the first mask pattern 141 is completely removed.

[0061] At S134, the conductive layer in the region corresponding to the first mask pattern is partially removed while removing the remaining second mask pattern, to form a conductive via in the conductive line in the region corresponding to the second mask pattern.

[0062] After step S133, the semiconductor structure is further etched. In this etching process, an etching gas enabling a relatively low etch selectivity between the conductive line 121 and the second mask pattern 142 is selected so that the conductive line 121 exposed after the first mask pattern 141 is completely removed is also etched while the remaining second mask pattern 142 is etched. Therefore, after the remaining second mask pattern 142 is completely removed, the conductive line in the region where the first mask pattern 141 is located is also partially removed, thereby forming conductive lines 121 of different heights. The conductive line in the region corresponding to the first mask pattern 141 has a smaller height, while the conductive line in the region corresponding to the second mask pattern 142 has a greater height and thus forms a conductive via 123, as shown in FIGs. 8 and 9.

[0063] As can be seen from the above description, a main concept of the embodiments of the present disclosure lies in that a predetermined mask pattern is doped so that the doped region in the predetermined mask pattern has a higher etch rate than an undoped region, thereby forming conductive lines of different heights through a subsequent etching

process. The conductive line in the region corresponding to the first mask pattern 141 has a smaller height, while the conductive line in the region corresponding to the second mask pattern 142 has a greater height and thus forms a conductive via 123. Based on this concept and to further reduce the manufacturing processes of the conductive interconnect structure, step S13 may be further implemented by a one-step etching manner, so as to reduce the manufacturing cost of the conductive interconnect structure. In some implementations of embodiments of the present disclosure, the above step S13 may include:

etching the first mask pattern 141 and the second mask pattern 142 while etching the conductive layer 120 by the first mask pattern 141 and the second mask pattern 142;

where an etch selectivity between the conductive layer 120 and an undoped region in the predetermined mask pattern 140 is less than a predetermined value. In other words, the etch selectivity between the conductive layer 120 and the undoped region in the predetermined mask pattern 140 is relatively small, and the predetermined mask pattern 140 is also etched while the conductive layer 120 is removed. By selecting a suitable etching gas, the conductive layer 120 not covered by the predetermined mask pattern 140 is also completely removed when the etching of the second mask pattern 142 is completed, thereby forming the plurality of conductive lines 121.

[0064] The one-step etching will be described in detail below in stages.

[0065] In a stage 1, during etching of the semiconductor structure shown in FIG. 4, when the doped region in the first mask pattern 141 is etched and removed, since the doped region in the predetermined mask pattern 140 has a higher etch rate than an undoped region, the second mask pattern 142 is partially etched, for example, by a very small amount, and the conductive layer 120 not covered by the predetermined mask pattern 140 is also etched to some extent. In other words, a part of the conductive layer 120 not covered by the predetermined mask pattern 140 is also partially etched to form a plurality of grooves 122, as shown in FIG. 10.

[0066] In a stage 2, the semiconductor structure shown in FIG. 10 is further etched, and when the first mask pattern 141 is completely removed, since the remaining undoped first mask pattern 141 has the same etch rate as the second mask pattern 142, the second mask pattern 142 is also etched correspondingly, resulting in a reduced height. Meanwhile, since the etch selectivity between the conductive layer 120 and the undoped region in the predetermined mask pattern 140 is less than the predetermined value, the conductive layer 120 not covered by the predetermined mask pattern 140 is also further etched, resulting in an increased depth of the grooves 122, as shown in FIG. 11.

[0067] In a stage 3, the semiconductor structure shown in FIG. 11 is further etched, and when the second mask pattern 142 is completely removed, the conductive layer 120 not covered by the predetermined mask pattern 140 is also completely removed, thereby forming a plurality of conductive lines 121 of different heights. Meanwhile, the conductive layer 120 in the region corresponding to the first mask pattern 141 is partially etched, so that the conductive line in the region corresponding to the first mask pattern 141 has a smaller height, while the conductive line in the region corresponding to the second mask pattern 142 has a greater height than the conductive line in the region corresponding to the first mask pattern 141, and the conductive line in the region corresponding to the second mask pattern 142 serves as a conductive via 123, as shown in FIGs. 8 and 9.

[0068] In the method for forming a conductive interconnect structure provided in the embodiments of the present disclosure, a predetermined mask pattern is doped so that the doped region in the predetermined mask pattern has a higher etch rate than an undoped region, thereby forming conductive lines of different heights through a subsequent etching process, and the conductive line in the region corresponding to the second mask pattern 142 has a greater height than the conductive line in the region corresponding to the first mask pattern 141, so that the conductive line in the region corresponding to the second mask pattern 142 is formed as a conductive via 123. The conductive via 123 is formed by a self-aligned process, which means that only an exposed portion of a corresponding film layer not covered by an upper film layer is etched during the etching process. Therefore, automatic alignment of the etching position is achieved, which will not cause the problem of alignment deviation between the conductive via and the conductive line that may be otherwise caused by a damascene process in the related art, while involving fewer process steps without a precise mask pattern, compared with a subtractive etching process in the related art.

[0069] Hereinafter, a method for forming a conductive interconnect structure provided in the embodiments of the present disclosure will be described in more detail, and the method may include the following steps S101 to S109.

[0070] At S101, a mandrel is formed on the conductive layer.

[0071] As shown in FIG. 12, detailed descriptions of the substrate 100, the liner 110, the conductive layer 120, and the hard mask layer 130 may refer to the corresponding descriptions above, and are not repeated here.

[0072] The mandrel 150 may be composed of, for example, SiN, SiCN, SiOCN, SiBCN,

or any other insulating material known in the art. Specifically, the mandrel 150 may be formed by depositing an insulation layer on the conductive layer 120, and then etching the insulation layer. The etching may be dry etching or laser ablation, or any process known in the art for selective removal, which is not limited in any way here.

5 [0073] At S102, a spacer is formed as the predetermined mask pattern on a sidewall of the mandrel.

[0074] As shown in FIG. 13, the spacer, i.e., the predetermined mask pattern 140 described above, may be composed of any dielectric material, such as a dielectric oxide, a dielectric nitride, and/or a dielectric oxynitride. In some embodiments, the spacer (i.e.,
10 the predetermined mask pattern 140) may be composed of a non-conductive low capacitance dielectric material, such as silicon dioxide. The process of forming the spacer (i.e., the predetermined mask pattern 140) may include depositing an insulating material, such as silicon nitride, on exposed surfaces of the mandrel 150 and the hard mask layer 130 by, for example, CVD, plasma enhanced chemical vapor deposition (PECVD),
15 physical vapor deposition (PVD), or any other deposition process. Then, an anisotropic etching process with a forward etch rate greater than a lateral etch rate may be used to etch and remove a horizontal part of the deposited insulating material to form the spacer (i.e., the predetermined mask pattern 140) on the sidewall of the mandrel 150. While the process of forming the spacer as the predetermined mask pattern 140 by self-aligned
20 double patterning is described above, it should be understood by those skilled in the art that finer predetermined mask pattern 140 may be formed by self-aligned quadruple patterning or more patterning, which is not described in detail here.

[0075] At S103, a planarization layer is formed on the conductive layer to fill a region between spacers.

25 [0076] At S104, a planarization process is performed on the planarization layer to expose the mandrel and the spacer.

[0077] As shown in FIG. 14, the planarization layer 160 may be composed of, for example, a spin-on carbon (SOC) material, and may be formed on the conductive layer 120 by deposition, such as chemical vapor deposition. When the planarization layer 160
30 is deposited, a surface of the mandrel 150 is covered by the planarization layer 160, and in this case, the planarization process is performed to expose the surface of the mandrel 150, and a region between spacers (i.e., predetermined mask patterns 140) is filled up to obtain a planar surface to facilitate subsequent process steps.

[0078] At S105, a mask layer is formed on a surface of the planarization layer to block a

second spacer.

[0079] As shown in FIG. 15, a mask layer 170 is formed on a surface of the planarization layer 160 to block the second spacer (serving as the second mask pattern 142). A region corresponding to the mask layer 170 is a region where a conductive via is to be formed.

5 [0080] At S106, ion implantation is performed on an unblocked first spacer (serving as the first mask pattern 141).

[0081] As shown in FIG. 16, after the ion implantation, a doped region having a predetermined depth is formed in the first spacer. In the related art shown in FIG. 2, the mask pattern 13 is a mask for etching and needs to be precisely formed at a corresponding
10 position, and when a pitch of conductive lines is as low as a nanometer level, it is difficult to achieve a corresponding precision of the mask pattern for etching. Unlike this, the mask layer 170 in this embodiment is a mask for ion implantation and has a lower requirement for the precision in mask position, and even if the position of the mask layer 170 is slightly shifted, the ion implantation into the first spacer will not be affected. For example, the
15 position shift of the mask layer 170 may be overcome by slightly adjusting an ion implantation angle, and the like.

[0082] The mask layer 170 may be, for example, photoresist, and when the ion implantation is completed, the mask layer 170 may be removed by a photoresist removal process.

20 [0083] At S107, the planarization layer and the mandrel are removed.

[0084] The semiconductor structure after removal of the mandrel 150 and the planarization layer 160 is shown in FIG. 17. In step S107, the mandrel 150 and the planarization layer 160 may be removed by taking the hard mask layer 130 as an etch stop layer.

25 [0085] In some implementations of embodiments of the present disclosure, the mandrel 150 and the planarization layer 160 may be removed simultaneously or in separate steps.

[0086] In some other implementations of embodiments of the present disclosure, the doped region of the first spacer (serving as the first mask pattern 141) may be removed while the mandrel 150 and/or the planarization layer 160 are removed.

30 [0087] At S108, the hard mask layer 130 and the conductive layer 120 which are not covered by the first spacer (serving as the first mask pattern 141) and the second spacer (serving as the second mask pattern 142) are removed by taking the first spacer and the second spacer as masks.

[0088] In this step, the etching of the hard mask layer 130 and the conductive layer 120

may be completed in a one-step etching process. Apparently, the etching of the hard mask layer 130 and the conductive layer 120 may be complemented in separate steps, thereby forming a plurality of conductive lines 121.

[0089] In some implementations of embodiments of the present disclosure, the liner 110 not covered by the first spacer and the second spacer is also removed while the hard mask layer 130 and the conductive layer 120 which are not covered by the first spacer and the second spacer are removed, as shown in FIG. 18.

[0090] It should be noted that, in the example of FIG. 18, other layers may be present between the substrate 100 and the liner 110 or the conductive line 121, and the embodiments of the present disclosure do not limit the metal interconnect layer where the conductive line 121 is located to be a lowermost metal interconnect layer, and instead, it may be any one of the interconnect layers.

[0091] At S109, the remaining first mask pattern and the second mask pattern are etched to completely remove the first mask pattern, and form a conductive via in the conductive line in the region corresponding to the second mask pattern.

[0092] In this step, since the second mask pattern 142 (i.e., the second spacer) has a height greater than the remaining first mask pattern 141 (i.e., the first spacer), the second mask pattern 142 partially remains after the first mask pattern 141 is completely removed. In the subsequent etching process, since the etch selectivity between the conductive line 121 and the second mask pattern 142 is relatively low, the conductive line 121 exposed after the first mask pattern 141 is completely removed is also etched while the remaining second mask pattern 142 is etched. Therefore, after the remaining second mask pattern 142 is completely removed, the conductive line in the region where the first mask pattern 141 is located is also partially removed, thereby forming conductive lines 121 of different heights. The conductive line in the region corresponding to the first mask pattern 141 has a smaller height, while the conductive line in the region corresponding to the second mask pattern 142 has a greater height, and the conductive line in the region corresponding to the second mask pattern 142 is formed as a conductive via 123, as shown in FIG. 19.

[0093] In this step, the remaining hard mask layer 130 on the conductive line 121 is also removed.

[0094] At S110, an interlayer insulation layer covering the conductive interconnect structure is formed, and a planarization process is performed to expose the conductive via.

[0095] As shown in FIG. 20, an interlayer insulation layer 180 is formed on the substrate 100 to cover the entire conductive interconnect structure, and a planarization process is

performed, so that an upper conductive interconnect structure may be formed on the interlayer insulation layer 180, where the upper conductive interconnect structure may be electrically connected to the current conductive interconnect structure through the conductive via 123.

5 [0096] In the method for forming a conductive interconnect structure provided in the embodiments of the present disclosure, a predetermined mask pattern is doped so that the doped region in the predetermined mask pattern has a higher etch rate than an undoped region, thereby forming conductive lines of different heights through a subsequent etching process, and the conductive line in the region corresponding to the second mask pattern
10 142 has a greater height than the conductive line in the region corresponding to the first mask pattern 141, so that the conductive line in the region corresponding to the second mask pattern 142 is formed as a conductive via 123. The conductive via 123 is formed by a self-aligned process, which will not cause the problem of alignment deviation between the conductive via and the conductive line that may be otherwise caused by a damascene
15 process in the related art, while involving fewer process steps without a precise mask pattern, compared with a subtractive etching process in the related art.

[0097] The above embodiments of the present disclosure emphasize the differences between various embodiments, and different optimization features between the embodiments can be combined to form a better embodiment as long as they are not
20 contradictory, and further description is omitted here in view of brevity of the text.

[0098] The above are only embodiments of the present disclosure and are not intended to limit the present disclosure. Those skilled in the art knows well that various modifications and changes may be made to the present disclosure. Any amendments, equivalent substitutions, improvements, and the like within the spirit and principle of the
25 present disclosure are included in the scope of protection defined by the appended claims of the present disclosure.

What is claimed is:

1. A method for forming a conductive interconnect structure, comprising:
forming a predetermined mask pattern on a conductive layer;

5 doping a first mask pattern to form a doped region having a predetermined depth
in the first mask pattern, wherein the first mask pattern is the predetermined mask
pattern that has been doped, and a second mask pattern is the predetermined mask
pattern that is undoped; and wherein the doped region has a higher etch rate than an
undoped region; and
10 etching the conductive layer by the first mask pattern and the second mask
pattern to form the conductive interconnect structure; wherein a conductive line in a
region corresponding to the second mask pattern has a greater height than a conductive
line in a region corresponding to the first mask pattern, and the conductive line in the
region corresponding to the second mask pattern is formed as a conductive via.

15 2. The method according to claim 1, wherein etching the conductive layer by the
first mask pattern and the second mask pattern comprises:

etching the first mask pattern and the second mask pattern while etching the
conductive layer by the first mask pattern and the second mask pattern;

20 wherein an etch selectivity between the conductive layer and an undoped region
in the predetermined mask pattern is less than a predetermined value.

3. The method according to claim 2, wherein the step of etching the first mask
pattern and the second mask pattern while etching the conductive layer by the first
25 mask pattern and the second mask pattern comprises stages of:

when the doped region in the first mask pattern is etched and removed, partially
etching the second mask pattern while partially etching the conductive layer not
covered by the predetermined mask pattern;

30 when the first mask pattern is completely removed, etching the second mask
pattern correspondingly while further etching the conductive layer not covered by the
predetermined mask pattern; and

when the second mask pattern is completely removed, completely removing the
conductive layer not covered by the predetermined mask pattern to form a plurality of
conductive lines, and partially etching the conductive layer in the region corresponding

to the first mask pattern, such that the conductive line in the region corresponding to the second mask pattern has a greater height than the conductive line in the region corresponding to the first mask pattern, and the conductive line in the region corresponding to the second mask pattern is used as the conductive via.

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4. The method according to claim 1, wherein etching the conductive layer by the first mask pattern and the second mask pattern comprises:

removing the doped region in the first mask pattern;

10 etching the remaining first mask pattern and the second mask pattern to completely remove the first mask pattern; and

partially removing the conductive layer in the region corresponding to the first mask pattern while removing the remaining second mask pattern, to form the conductive via in the conductive line in the region corresponding to the second mask pattern.

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5. The method according to claim 4, wherein the conductive layer not covered by the predetermined mask pattern is etched while the first mask pattern and the second mask pattern are etched and removed.

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6. The method according to claim 4, wherein before removing the doped region in the first mask pattern, the method further comprises:

etching the conductive layer by the first mask pattern and the second mask pattern to form the conductive line; or

25 after removing the doped region in the first mask pattern, the method further comprises:

etching the conductive layer by the remaining first mask pattern and the second mask pattern to form the conductive line.

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7. The method according to claim 1, wherein forming the predetermined mask pattern on the conductive layer comprises:

forming a mandrel on the conductive layer; and

forming a spacer as the predetermined mask pattern on a sidewall of the mandrel.

8. The method according to claim 7, wherein doping the first mask pattern

comprises:

doping a first spacer to form a doped region having a predetermined depth in the first spacer, wherein the first spacer is the spacer that has been doped, and a second spacer is the spacer that is undoped.

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9. The method according to claim 8, wherein doping the first spacer comprises: forming a planarization layer on the conductive layer to fill a region between spacers;

10 performing a planarization process on the planarization layer to expose the mandrel and the spacer;

forming a mask layer on a surface of the planarization layer to block the second spacer; and

performing ion implantation on the first spacer that is unblocked.

15 10. The method according to claim 9, wherein the planarization layer comprises an SOC material; or
an element for the ion implantation is Ge.

20 11. The method according to claim 9, further comprising:
removing the mandrel and the planarization layer.

12. The method according to claim 11, wherein the doped region of the first spacer is removed while the mandrel and/or the planarization layer are removed.

25 13. The method according to claim 11, wherein a hard mask layer is further provided between the conductive layer, and the mandrel and the planarization layer, and removing the mandrel and the planarization layer comprises:

removing the mandrel and the planarization layer by taking the hard mask layer as an etch stop layer.

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14. The method according to claim 13, wherein etching the conductive layer by the first mask pattern and the second mask pattern comprises:

removing the hard mask layer and the conductive layer which are not covered by the first spacer and the second spacer by taking the first spacer and the second

spacer as masks.

15. The method according to claim 14, wherein a liner is further provided below the conductive layer, and removing the hard mask layer and the conductive layer which are not covered by the first spacer and the second spacer by taking the first spacer and the second spacer as masks further comprises:

removing the liner not covered by the first spacer and the second spacer.

16. The method according to claim 15, wherein the liner comprises at least one of TiN, TaN, Al, Cu, Ni, Co, Ru, Ti and Ta.

17. The method according to claim 1, wherein the conductive layer is a metal conductive layer; or

the conductive layer comprises at least one of Ru, Co, Mo, W, Al and Rh.

18. The method according to claim 1, wherein forming the predetermined mask pattern on the conductive layer comprises:

forming the predetermined mask pattern by self-aligned multi-patterning.