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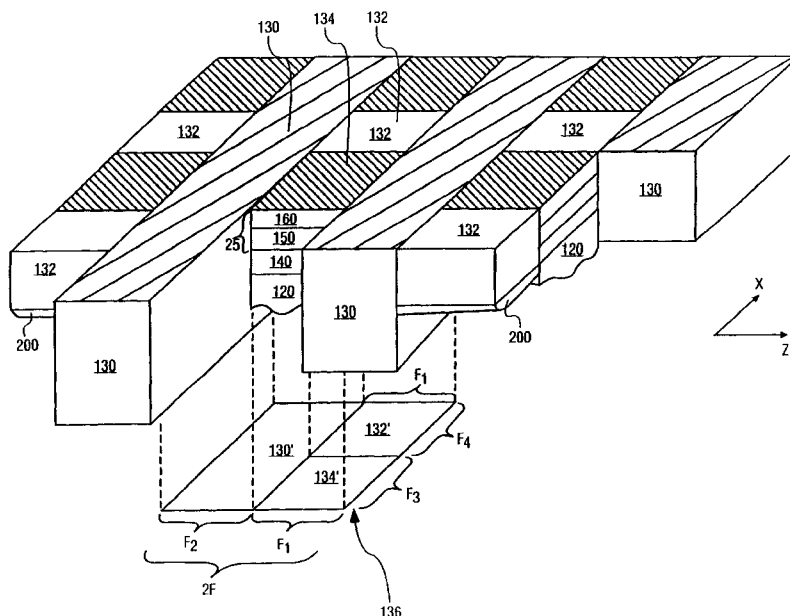
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| <p>(51) International Patent Classification⁷: H01L 27/102, 21/762, 45/00, 27/24, G11C 11/34</p> <p>(21) International Application Number: PCT/US02/05534</p> <p>(22) International Filing Date: 22 February 2002 (22.02.2002)</p> <p>(25) Filing Language: English</p> <p>(26) Publication Language: English</p> <p>(71) Applicants: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). OVONYX, INC. [US/US]; 1675 West Maple Road, Troy, MI 48084 (US).</p> <p>(72) Inventor: XU, Daniel; 930 Rich Avenue, Mountain View, CA 94040 (US).</p> <p>(74) Agents: MALLIE, Michael, J. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).</p> | <p>(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.</p> <p>(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published:
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(54) Title: DUAL TRENCH ISOLATION FOR A PHASE-CHANGE MEMORY CELL AND METHOD OF MAKING SAME



(57) Abstract: The invention relates to a phase-change memory device. The device includes a double-trench isolation structure around the diode stack that communicates to the lower electrode. The present invention also relates to a method of making a phase-change memory device. The method includes forming two orthogonal and intersecting isolation trenches around a memory cell structure diode stack.