Abstract

A variety of applications can include apparatus having a memory device structured with a circuit under array (CuA) architecture. A page buffer region in the CuA can be formed with a periphery region that is horizontally adjacent to the page buffer region. Contacts to gates for transistors in the page buffer region can be formed to land only on these gates, separating and electrically isolating the contacts and associated gates from each other in the page buffer region. Contacts to gates for transistors in the periphery region can be formed to land on conductive regions disposed on gates for transistors in the periphery region.

Figure 12.